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SDRAM

*New part number system for
New millennium business*

2000 Data Book

128Mb/256Mb <<<

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TABLE OF CONTENTS

I. General Information

A. SDRAM Component Product Guide	15
B. SDRAM Module Product Guide	16
C. SDRAM Component Ordering Information : NEW	18
D. SDRAM Component Ordering Information : OLD	19
E. SDRAM Module Ordering Information : NEW	20
F. SDRAM Module Ordering Information : OLD	21
G. Package Dimension	22

II. Component Specifications

A . 128Mb M-die SDRAM Datasheet

K4S280432M	32M x 4 bit	29
K4S280832M	16M x 8 bit	38
K4S281632M	8M x 16 bit	47

B . 128Mb A-die SDRAM Datasheet

K4S280432A	32M x 4 bit	59
K4S280832A	16M x 8 bit	68

C . 128Mb B-die SDRAM Datasheet

K4S280432B	32M x 4 bit	79
K4S280832B	16M x 8 bit	88
K4S281632B	8M x 16 bit	97

D . 256Mb A-die SDRAM Datasheet

K4S560432A	64M x 4 bit	109
K4S560832A	32M x 8 bit	118
K4S561632A	16M x 16 bit	127

E . Device Operation & Timing Diagram

Device Operation	139
Timing Diagram	155

III. Module Specifications

A . PC66 SODIMM Datasheet

128Mb M-die

M466S0924MT0-L10	8M x 64 1 row of	8MX16	181
M466S1723MT2-L10	16M x 64 1 row of	16MX 8	192
M466S1723MT3-L10	16M x 64 1 row of	16MX 8	203
M466S1724MT2-L10	16M x 64 2 row of	8MX16	214

128Mb A-die

M466S1723AT2-L10	16M x 64 1 row of	16MX 8	225
M466S1723AT3-L10	16M x 64 1 row of	16MX 8	236

128Mb B-die

M466S0924BT0-L10,C10	8M x 64 1 row of	8MX16	247
M466S1723BT2-L10,C10	16M x 64 1 row of	16MX 8	258
M466S1723BT3-L10,C10	16M x 64 1 row of	16MX 8	269
M466S1724BT2-L10,C10	16M x 64 2 row of	8MX16	280

B . PC100 SODIMM Datasheet

128Mb M-die

M464S0924MT1-L1H,L1L	8M x 64 1 row of	8MX16	293
M464S1724MT1-L1H,L1L	16M x 64 2 row of	8MX16	304

128Mb B-die

M464S0924BT1-L1H,L1L,C1H,C1L	8M x 64 1 row of	8MX16	315
M464S1724BT1-L1H,L1L,C1H,C1L	16M x 64 2 row of	8MX16	326

C . PC100 Registered DIMM Datasheet

128Mb M-die

M377S1723MT3 -C1H,C1L	16M x 72	1 row of	16MX 8	339
M377S3320MT3 -C1H,C1L	32M x 72	1 row of	32MX 4	351
M377S3323MT0 -C1H,C1L	32M x 72	2 row of	16MX 8	363
M377S6428MT3 -C1H,C1L	64M x 72	2 row of St.	64MX 4	375

128Mb A-die

M377S1723AT3 -C1H,C1L	16M x 72	1 row of	16MX 8	387
M377S3320AT3 -C1H,C1L	32M x 72	1 row of	32MX 4	399
M377S3323AT0 -C1H,C1L	32M x 72	2 row of	16MX 8	411
M377S6428AT3 -C1H,C1L	64M x 72	2 row of St.	64MX 4	423

128Mb B-die

M377S1723BT3 -C1H,C1L	16M x 72	1 row of	16MX 8	435
M377S3320BT3 -C1H,C1L	32M x 72	1 row of	32MX 4	447
M377S3323BT0 -C1H,C1L	32M x 72	2 row of	16MX 8	459
M377S6428BT3 -C1H,C1L	64M x 72	2 row of St.	64MX 4	471

256Mb A-die

M377S3253AT3 -C1H,C1L	32M x 72	1 row of	32MX 8	483
M377S6450AT3 -C1H,C1L	64M x 72	1 row of	64MX 4	495
M377S6453AT0 -C1H,C1L	64M x 72	2 row of	32MX 8	507
M377S2858AT3 -C1H,C1L	128M x 72	2 row of St.	128MX 4	519

D . PC100 Unbuffered DIMM Datasheet

128Mb M-die

M366S0924MTS -C80,C1H,C1L	8M x 64 1 row of	8MX16	533
M366S1724MT0 -C80,C1H,C1L	16M x 64 2 row of	8MX16	544
M366S1723MTS -C80,C1H,C1L	16M x 64 1 row of	16MX 8	555
M374S1723MTS -C80,C1H,C1L	16M x 72 1 row of	16MX 8	566
M366S3323MT0 -C80,C1H,C1L	32M x 64 2 row of	16MX 8	577
M374S3323MT0 -C80,C1H,C1L	32M x 72 2 row of	16MX 8	588

128Mb A-die

M366S1723ATS -C80,C1H,C1L	16M x 64 1 row of	16MX 8	599
M374S1723ATS -C80,C1H,C1L	16M x 72 1 row of	16MX 8	610
M366S3323AT0 -C80,C1H,C1L	32M x 64 2 row of	16MX 8	621
M374S3323AT0 -C80,C1H,C1L	32M x 72 2 row of	16MX 8	632

128Mb B-die

M366S0924BTS -C80,C1H,C1L	8M x 64 1 row of	8MX16	643
M366S1724BT0 -C80,C1H,C1L	16M x 64 2 row of	8MX16	654
M366S1723BTS -C80,C1H,C1L	16M x 64 1 row of	16MX 8	665
M374S1723BTS -C80,C1H,C1L	16M x 72 1 row of	16MX 8	676
M366S3323BT0 -C80,C1H,C1L	32M x 64 2 row of	16MX 8	687
M374S3323BT0 -C80,C1H,C1L	32M x 64 2 row of	16MX 8	698

256Mb A-die

M366S3253ATS -C80,C1H,C1L	32M x 64 1 row of	32MX 8	709
M374S3253ATS -C80,C1H,C1L	32M x 72 1 row of	32MX 8	720
M366S6453AT0 -C80,C1H,C1L	64M x 64 2 row of	32MX 8	731
M374S6453AT0 -C80,C1H,C1L	64M x 72 2 row of	32MX 8	742

E . PC133 SODIMM Datasheet

128Mb B-die

M464S0924BT1 -C75,L75	8M x 64 1 row of	8MX16	755
M464S1724BT1 -C75,L75	16M x 64 2 row of	8MX16	766

F . PC133 Registered DIMM Datasheet

128Mb A-die

M390S1723AT1-C75	 16M x 72 1 row of	16MX 8	 779
M390S3320AT1-C75	 32M x 72 1 row of	32MX 4	 791

128Mb B-die

M390S1723BT1-C75	 16M x 72 1 row of	16MX 8	 803
M390S3320BT1-C75	 32M x 72 1 row of	32MX 4	 815

256Mb A-die

M390S3253AT1-C75	 32M x 72 1 row of	32MX 8	 827
M390S6450AT1-C75	 64M x 72 1 row of	64MX 4	 839
M390S2858AT1-C75	 128M x 72 2 row of St.128MX 4		 851

G . PC133 Unbuffered DIMM Datasheet

128Mb A-die

M366S1723ATS-C75	 16M x 64 1 row of	16MX 8	 865
M374S1723ATS-C75	 16M x 72 1 row of	16MX 8	 876
M366S3323AT0-C75	 32M x 64 2 row of	16MX 8	 887
M374S3323AT0-C75	 32M x 72 2 row of	16MX 8	 898

128Mb B-die

M366S1723BTS-C75	 16M x 64 1 row of	16MX 8	 909
M374S1723BTS-C75	 16M x 72 1 row of	16MX 8	 920
M366S3323BT0-C75	 32M x 64 2 row of	16MX 8	 931
M374S3323BT0-C75	 32M x 72 2 row of	16MX 8	 942

256Mb A-die

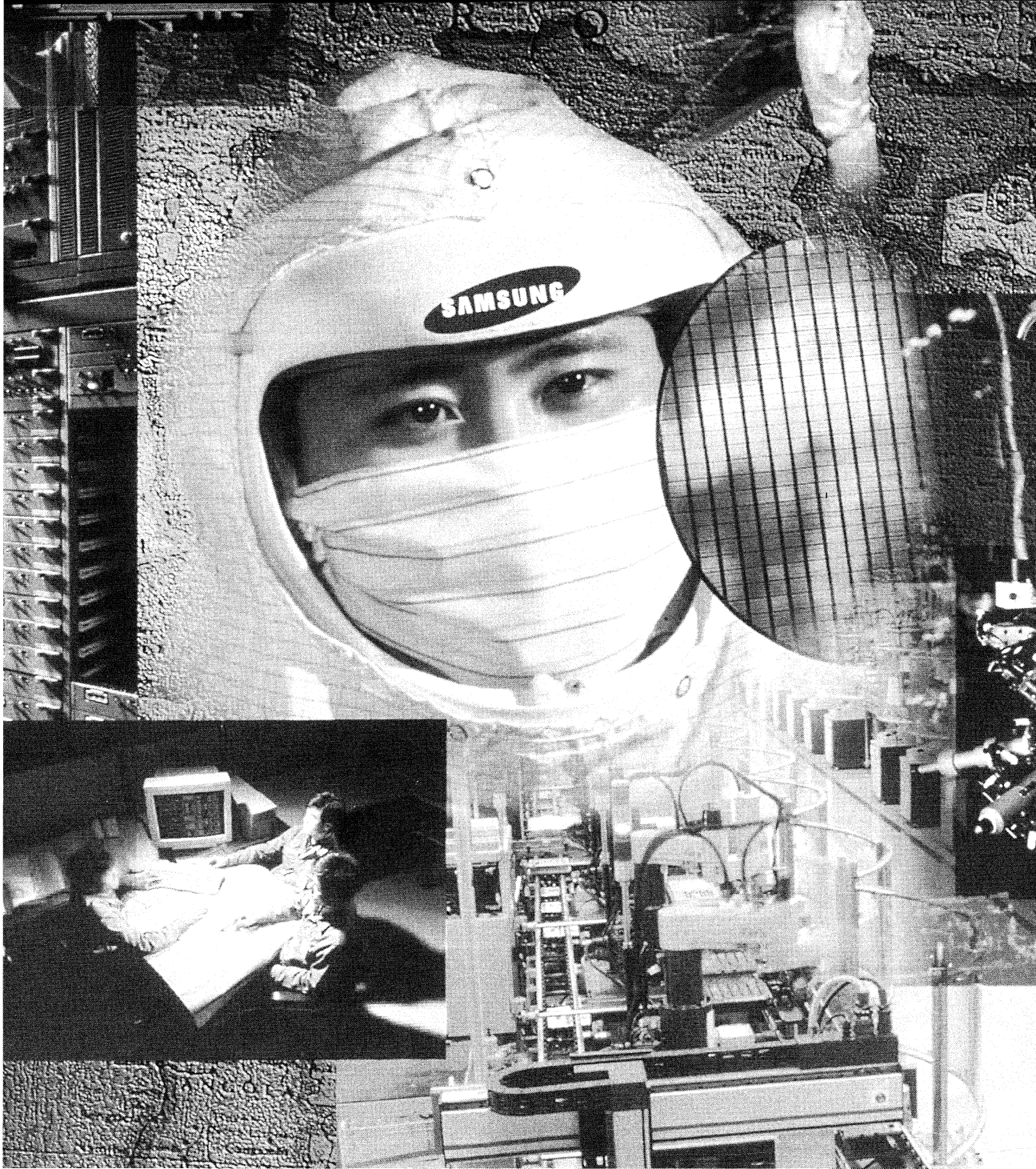
M366S3253ATS-C75	 32M x 64 1 row of	32MX 8	 953
M374S3253ATS-C75	 32M x 72 1 row of	32MX 8	 964
M366S6453AT0-C75	 64M x 64 2 row of	32MX 8	 975
M374S6453AT0-C75	 64M x 72 2 row of	32MX 8	 986

IV . Serial Presence Detect User's Manual 1001

V . Saes Offices and Manufacturer's Representatives 1021

General Information	1
Component Specification	2
128M bit M-die	
128M bit A-die	
128M bit B-die	
256M bit A-die	
Device Operation & Timing Diagram	
Module Specification	3
PC66 SODIMM	
PC100 SODIMM	
PC100 Registered DIMM	
PC100 Unbuffered DIMM	
PC133 SODIMM	
PC133 Registered DIMM	
PC133 Unbuffered DIMM	
Serial Presence Detect User's Manual	4
Sales Offices and Manufacturer's Representation	5

General Information 1



A. SDRAM Component Product Guide

1

Density	Banks	New Part Number	Old Part Number	Power* ¹ (-C/L) & Speed * ³	Org.	Interface	Ref.	Power (V)	Pkg.	Avail
128Mb 1st	4Banks	K4S280432M	KM44S32030	T ² C80/C1H/C1L/C10 TL80/L1H/L1L/L10	32M x 4	LVTTL	4K	3.3 ± 0.3V	TSOP II 54pin	Now
		K4S280832M	KM48S16030		16M x 8					Now
		K4S281632A	KM416S8030A		8M x16					Now
128Mb 2nd	4Banks	K4S280432A	KM44S32030A	TC75/C80/C1H/C1L/C10 TL75/L80/L1H/L1L/L10	32M x 4	LVTTL	4K	3.3 ± 0.3V	TSOP II 54pin	Now
		K4S280832A	KM48S16030A		16M x 8					Now
128Mb 3rd	4Banks	K4S280432B	KM44S32030B	TC75/C80/C1H/C1L/C10 TL75/L80/L1H/L1L/L10	32M x 4	LVTTL	4K	3.3 ± 0.3V	TSOP II 54pin	Now
		K4S280832B	KM48S16030B		16M x 8					Now
		K4S281632B	KM416S8030B		8M x16					Now
256Mb 2nd	4Banks	K4S560432A	KM44S64230A	TC75/C80/C1H/C1L TL75/L80/L1H/L1L	64M x 4	LVTTL	4K	3.3 ± 0.3V	TSOP II 54pin	Now
		K4S560832A	KM48S32230A		32M x 8					Now
		K4S561632A	KM416S16230A		16M x16					Now

Note 1 :

Temperature and Power		
NEW	OLD	Description
C	G	Commercial Temperature, Normal Power
L	F	Commercial Temperature, Low Power

Note 2:
T : TSOP II (400mil)

Note 3:

Speed		
NEW	OLD	Description
75	A	PC133 (@CL=3)
1H	H	PC100 (@CL=2)
1L	L	PC100 (@CL=3)
10	10	PC66 (@CL=2 & CL=3)
80	8	125Mhz(@CL=3)

B. SDRAM Module Product Guide

Org.	New Part No.	Old Part No.	Speed	Composition	Comp. Version	Vtg.	Internal Banks	External Banks	Feature	Avail.
144pin PC66 SODIMM										
8M x 64	M466S0924MT0	KMM466S924T	L10	8Mx16 * 4 pcs	128Mb 1st	3.3V	4	1	DS, 1000mil	Now
	M466S0924BT0	KMM466S924BT	L10, C10	8Mx16 * 4 pcs	128Mb 3rd			1	DS, 1000mil	Now
16Mx64	M466S1723MT2	KMM466S1723T2	L10	16Mx 8 * 8 pcs	128Mb 1st			1	DS, 1150mil	Now
	M466S1723AT2	KMM466S1723AT2	L10, C10	16Mx 8 * 8 pcs	128Mb 2nd			1	DS, 1150mil	Now
	M466S1723BT2	KMM466S1723BT2	L10, C10	16Mx 8 * 8 pcs	128Mb 3rd			1	DS, 1150mil	Now
	M466S1723MT3	KMM466S1723T3	L10	16Mx 8 * 8 pcs	128Mb 1st			1	DS, 1050mil	Now
	M466S1723AT3	KMM466S1723AT3	L10, C10	16Mx 8 * 8 pcs	128Mb 2nd			1	DS, 1050mil	Now
	M466S1723BT3	KMM466S1723BT3	L10, C10	16Mx 8 * 8 pcs	128Mb 3rd			1	DS, 1050mil	Now
	M466S1724MT2	KMM466S1724T2	L10	8Mx16 * 8 pcs	128Mb 1st			2	DS, 1150mil	Now
	M466S1724BT2	KMM466S1724BT2	L10, C10	8Mx16 * 8 pcs	128Mb 3rd			2	DS, 1150mil	Now
144pin PC100 SODIMM										
8M x 64	M464S0924MT1	KMM464S924T1	L1H, L1L	8Mx16 * 4 pcs	128Mb 1st	3.3V	4	1	DS, 1000mil	Now
	M464S0924BT1	KMM464S924BT1	L1H, L1L C1H, C1L	8Mx16 * 4 pcs	128Mb 3rd			1	DS, 1000mil	Now
16M x 64	M464S1724MT1	KMM464S1724T1	L1H, L1L	8Mx16 * 8 pcs	128Mb 1st			2	DS, 1250mil	Now
	M464S1724BT1	KMM464S1724BT1	L1H, L1L C1H, C1L	8Mx16 * 8 pcs	128Mb 3rd			2	DS, 1250mil	Now
	M464S1654AT1	KMM464S1654AT1	L1H, L1L C1H, C1L	16Mx16 * 4 pcs	256Mb 2nd			1	DS, 1000mil	TBD
32M x 64	M464S3254AT1	KMM464S3254AT1	L1H, L1L C1H, C1L	16Mx16 * 8 pcs	256Mb 2nd			2	DS, 1250mil	TBD
168pin PC100 Registered DIMM										
16M x 72	M377S1723MT3	KMM377S1723T3	C1H, C1L	16Mx 8 * 9 pcs	128Mb 1st	3.3V	4	1	DS, 1500mil	Now
	M377S1723AT3	KMM377S1723AT3	C1H, C1L	16Mx 8 * 9 pcs	128Mb 2nd			1	DS, 1500mil	Now
	M377S1723BT3	KMM377S1723BT3	C1H, C1L	16Mx 8 * 9 pcs	128Mb 3rd			1	DS, 1500mil	Now
32Mx72	M377S3320MT3	KMM377S3320T3	C1H, C1L	32Mx 4 * 18 pcs	128Mb 1st			1	DS, 1700mil	Now
	M377S3320AT3	KMM377S3320AT3	C1H, C1L	32Mx 4 * 18 pcs	128Mb 2nd			1	DS, 1700mil	Now
	M377S3320BT3	KMM377S3320BT3	C1H, C1L	32Mx 4 * 18 pcs	128Mb 3rd			1	DS, 1700mil	Now
	M377S3323MT0	KMM377S3323T	C1H, C1L	16Mx 8 * 18 pcs	128Mb 1st			2	DS, 1700mil	Now
	M377S3323AT0	KMM377S3323AT	C1H, C1L	16Mx 8 * 18 pcs	128Mb 2nd			2	DS, 1700mil	Now
	M377S3323BT0	KMM377S3323BT	C1H, C1L	16Mx 8 * 18 pcs	128Mb 3rd			2	DS, 1700mil	Now
	M377S3253AT3	KMM377S3253AT3	C1H, C1L	32Mx 8 * 9 pcs	256Mb 2nd			1	DS, 1500mil	Now
	M377S6428MT3	KMM377S6428T3	C1H, C1L	St. 64Mx 4 * 18 pcs	128Mb 1st			2	DS, 1700mil	Now
64M x 72	M377S6428AT3	KMM377S6428AT3	C1H, C1L	St. 64Mx 4 * 18 pcs	128Mb 2nd			2	DS, 1700mil	Now
	M377S6428BT3	KMM377S6428BT3	C1H, C1L	St. 64Mx 4 * 18 pcs	128Mb 3rd			2	DS, 1700mil	Now
	M377S6450AT3	KMM377S6450AT3	C1H, C1L	64Mx 4 * 18 pcs	256Mb 2nd			1	DS, 1700mil	Now
	M377S6453AT0	KMM377S6453AT	C1H, C1L	32Mx 8 * 18 pcs	256Mb 2nd			2	DS, 1700mil	Now
	M377S2858AT3	KMM377S2858AT3	C1H, C1L	St. 128Mx 4 * 18 pcs	256Mb 2nd			2	DS, 1700mil	Now

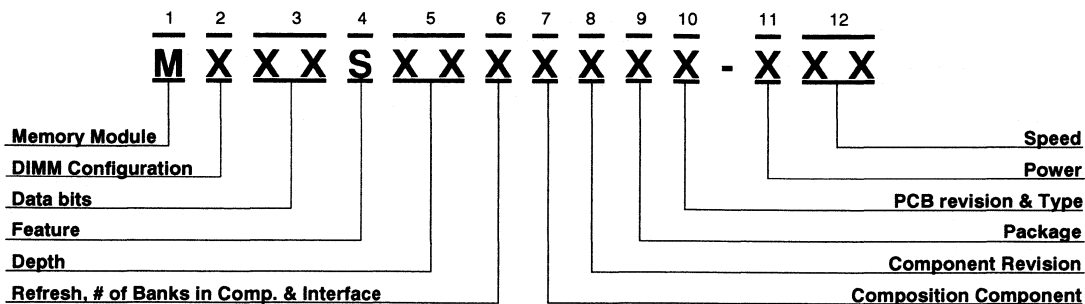
Org.	New Part No.	Old Part No.	Speed	Composition	Comp. Version	Vtg.	Internal Banks	External Banks	Feature	Avail.		
168pin PC100 Unbuffered DIMM												
16Mx64	M366S0924MTS	KMM366S924TS	C80,C1H,C1L	8Mx16 * 4 pcs	128Mb 1st	3.3 V	4	1	SS, 1000mil	Now		
	M366S0924BTS	KMM366S924BTS	C80,C1H,C1L	8Mx16 * 4 pcs	128Mb 3rd			1	SS, 1000mil	Now		
	M366S1723MTS	KMM366S1723TS	C80,C1H,C1L	16Mx 8 * 8 pcs	128Mb 1st			1	SS, 1375mil	Now		
	M366S1723ATS	KMM366S1723ATS	C80,C1H,C1L	16Mx 8 * 8 pcs	128Mb 2nd			1	SS, 1375mil	Now		
	M366S1723BTS	KMM366S1723BTS	C80,C1H,C1L	16Mx 8 * 8 pcs	128Mb 3rd			1	SS, 1375mil	Now		
	M366S1724MT0	KMM366S1724T	C80,C1H,C1L	8Mx16 * 8 pcs	128Mb 1st			2	DS, 1375mil	Now		
16Mx72	M366S1724BT0	KMM366S1724BT	C80,C1H,C1L	8Mx16 * 8 pcs	128Mb 3rd			2	DS, 1375mil	Now		
	M374S1723MTS	KMM374S1723TS	C80,C1H,C1L	16Mx 8 * 9 pcs	128Mb 1st			1	SS, 1375mil	Now		
	M374S1723ATS	KMM374S1723ATS	C80,C1H,C1L	16Mx 8 * 9 pcs	128Mb 2nd			1	SS, 1375mil	Now		
32Mx64	M374S1723BTS	KMM374S1723BTS	C80,C1H,C1L	16Mx 8 * 9 pcs	128Mb 3rd			1	SS, 1375mil	Now		
	M366S3323MT0	KMM366S3323T	C80,C1H,C1L	16Mx 8 * 16 pcs	128Mb 1st			2	DS, 1375mil	Now		
	M366S3323AT0	KMM366S3323AT	C80,C1H,C1L	16Mx 8 * 16 pcs	128Mb 2nd			2	DS, 1375mil	Now		
32Mx72	M366S3323BT0	KMM366S3323BT	C80,C1H,C1L	16Mx 8 * 16 pcs	128Mb 3rd			2	DS, 1375mil	Now		
	M366S3253ATS	KMM366S3253ATS	C80,C1H,C1L	32Mx 8 * 8 pcs	256Mb 2nd			1	SS, 1375mil	Now		
	M374S3323MT0	KMM374S3323T	C80,C1H,C1L	16Mx 8 * 18 pcs	128Mb 1st			2	DS, 1375mil	Now		
	M374S3323AT0	KMM374S3323AT	C80,C1H,C1L	16Mx 8 * 18 pcs	128Mb 2nd			2	DS, 1375mil	Now		
64Mx64	M374S3323BT0	KMM374S3323BT	C80,C1H,C1L	16Mx 8 * 18 pcs	128Mb 3rd			2	DS, 1375mil	Now		
	M374S3253ATS	KMM374S3253ATS	C80,C1H,C1L	32Mx 8 * 9 pcs	256Mb 2nd			1	SS, 1375mil	Now		
	M366S6453AT0	KMM366S6453AT	C80,C1H,C1L	32Mx 8 * 16 pcs	256Mb 2nd			2	DS, 1375mil	Now		
64Mx72	M374S6453AT0	KMM374S6453AT	C80,C1H,C1L	32Mx 8 * 18 pcs	256Mb 2nd			2	DS, 1375mil	Now		
144pin PC133 SODIMM												
8Mx64	M464S0924BT1	KMM464S924BT1	C75,L75	8Mx16 * 4 pcs	128Mb 3rd	3.3 V	4	1	DS, 1000mil	Now		
16Mx64	M464S1724BT1	KMM464S1724BT1	C75,L75	8Mx16 * 8 pcs	128Mb 3rd			2	DS, 1250mil	Now		
168pin PC133 Registered DIMM												
16Mx72	M390S1723AT1	KMM390S1723AT1	C75	16Mx 8 * 9 pcs	128Mb 2nd	3.3 V	4	1	DS, 1500mil	Now		
	M390S1723BT1	KMM390S1723BT1	C75	16Mx 8 * 9 pcs	128Mb 3rd			1	DS, 1500mil	Now		
32Mx72	M390S3320AT1	KMM390S3320AT1	C75	32Mx 4 * 18 pcs	128Mb 2nd			1	DS, 1700mil	Now		
	M390S3320BT1	KMM390S3320BT1	C75	32Mx 4 * 18 pcs	128Mb 3rd			1	DS, 1700mil	Now		
64Mx72	M390S3253AT1	KMM390S3253AT1	C75	32Mx 8 * 9 pcs	256Mb 2nd			1	DS, 1500mil	Now		
	M390S6450AT1	KMM390S6450AT1	C75	64Mx 4 * 18 pcs	256Mb 2nd			1	DS, 1700mil	Now		
128Mx72	M390S2858AT1	KMM390S2858AT1	C75	St. 128Mx 4 * 18 pcs	256Mb 2nd			2	DS, 1700mil	Now		
168pin PC133 Unbuffered DIMM												
16Mx64	M366S1723ATS	KMM366S1723ATS	C75	16Mx 8 * 8 pcs	128Mb 2nd	3.3V	4	1	SS, 1375mil	Now		
	M366S1723BTS	KMM366S1723BTS	C75	16Mx 8 * 8 pcs	128Mb 3rd			1	SS, 1375mil	Now		
16Mx72	M374S1723ATS	KMM374S1723ATS	C75	16Mx 8 * 9 pcs	128Mb 2nd			1	SS, 1375mil	Now		
	M374S1723BTS	KMM374S1723BTS	C75	16Mx 8 * 9 pcs	128Mb 3rd			1	SS, 1375mil	Now		
32Mx64	M366S3323AT0	KMM366S3323AT	C75	16Mx 8 * 16 pcs	128Mb 2nd			2	DS, 1375mil	Now		
	M366S3323BT0	KMM366S3323BT	C75	16Mx 8 * 16 pcs	128Mb 3rd			2	DS, 1375mil	Now		
	M366S3253ATS	KMM366S3253ATS	C75	32Mx 8 * 8 pcs	256Mb 2nd			1	SS, 1375mil	Now		
32Mx72	M374S3323AT0	KMM374S3323AT	C75	16Mx 8 * 18 pcs	128Mb 2nd			2	DS, 1375mil	Now		
	M374S3323BT0	KMM374S3323BT	C75	16Mx 8 * 18 pcs	128Mb 3rd			2	DS, 1375mil	Now		
	M374S3253ATS	KMM374S3253ATS	C75	32Mx 8 * 9 pcs	256Mb 2nd			1	SS, 1375mil	Now		
64Mx64	M366S6453AT0	KMM366S6453AT	C75	32Mx 8 * 16 pcs	256Mb 2nd					2	DS, 1375mil	Now
64Mx72	M374S6453AT0	KMM374S6453AT	C75	32Mx 8 * 18 pcs	256Mb 2nd					2	DS, 1375mil	Now

Diagram showing the pinout of a 16-pin package. Pins 1-8 are labeled K, 4, S, X, X, X, X, X. Pins 9-11 are labeled X, X, X, X. The package is identified as SAMSUNG Memory DRAM. The pinout is: Pin 1: SAMSUNG Memory; Pin 2: DRAM; Pin 3: Product; Pin 4: Density & Refresh; Pin 5: Organization; Pin 6: Interface (VDD, VDDQ); Pin 7: Revision; Pin 8: Package Type; Pin 9: Temperature & Power; Pin 10: Speed; Pin 11: Bank.

75: PC133 (133MHz @ CL=3)
1H: PC100 (100MHz @ CL=2 & CL=3)
1L: PC100 (100MHz @ CL=3)
10: PC66 (66MHz @ CL=2 & CL=3)
80: 8ns (125MHz @ CL=3)

1



E. SDRAM Module Ordering Information : NEW

1. Memory Module : M

2. DIMM Configuration

- 3 : DIMM
4 : SODIMM

3. Data Bits

- 64 : x64 PC100 SODIMM
with SPD for 144pin (Intel/JEDEC)
66 : x64 Unbuffered DIMM
with SPD for 144pin/168pin (Intel/JEDEC)
74 : X72 /ECC Unbuffered DIMM
with SPD for 168pin (Intel/JEDEC)
77 : x72 /ECC PLL + Register DIMM
with SPD for 168pin (Intel PC100)
90 : x72 /ECC PLL + Register DIMM
with SPD for 168pin (JEDEC PC133)

4. Feature

- S : SDRAM

5. Depth

- | | |
|-----------|-----------------------------|
| 01 : 1M | 02 : 2M |
| 04 : 4M | |
| 08 : 8M | 09 : 8M (for 128Mb/512Mb) |
| 16 : 16M | 17 : 16M (for 128Mb/512Mb) |
| 32 : 32M | 33 : 32M (for 128Mb/512Mb) |
| 64 : 64M | 65 : 64M (for 128Mb/512Mb) |
| 28 : 128M | 29 : 128M (for 128Mb/512Mb) |

6. Refresh, # of Banks in comp. & Interface

- 2 : 4K/ 64ms Ref., 4Banks & LVTTL
5 : 8K/ 64ms Ref., 4Banks & LVTTL

7. Composition Component

- 0 : x 4
3 : x 8
4 : x16
5 : x32
8 : x 4 Stack (Flexframe)
9 : x 8 Stack (Flexframe)

8. Component Revision

- | | |
|--------------|--------------|
| M : 1st Gen. | A : 2nd Gen. |
| B : 3rd Gen. | C : 4th Gen. |
| D : 5th Gen. | E : 6th Gen. |

9. Package

- T : TSOP II (400mil)
N : sTSOP II (400mil)

10. PCB Revision & Type

- | | |
|-----------------------|--------------|
| 0 : 1st Rev. | 1 : 2nd Rev. |
| 2 : 3rd Rev. | 3 : 4th Rev. |
| S : PC100 (4 Layer) | |

11. Power

- C : Commercial Normal
L : Commercial Low

12. Speed (Default CL= 3)

- 75 : PC133 (133MHz @ CL=3)
1H : PC100 (100MHz @ CL=2 & CL=3)
1L : PC100 (100MHz @ CL=3)
10 : PC66 (66MHz @ CL=2 & CL=3)
80 : 8ns (125MHz @ CL=3)

1

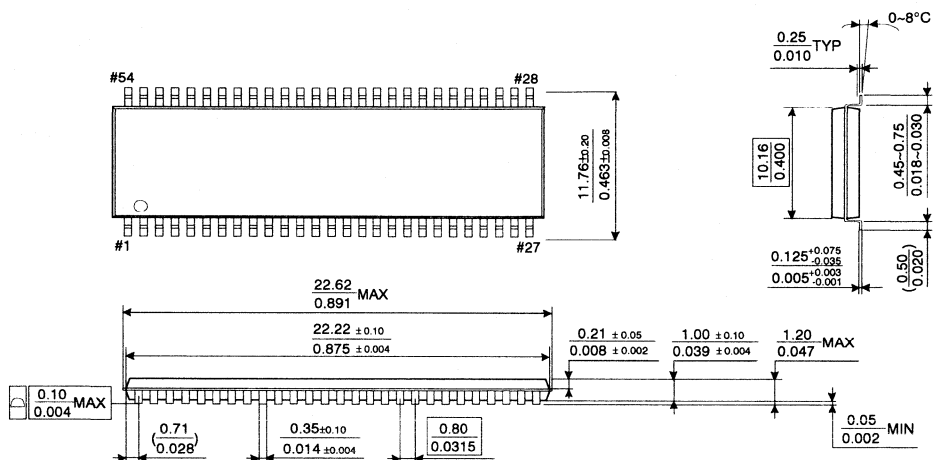


G. Package Dimension

PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE

54-TSOP2-400AF

Unit : Millimeters



SEC changed some symbols and test conditions from 128M bit A-die/B-die.

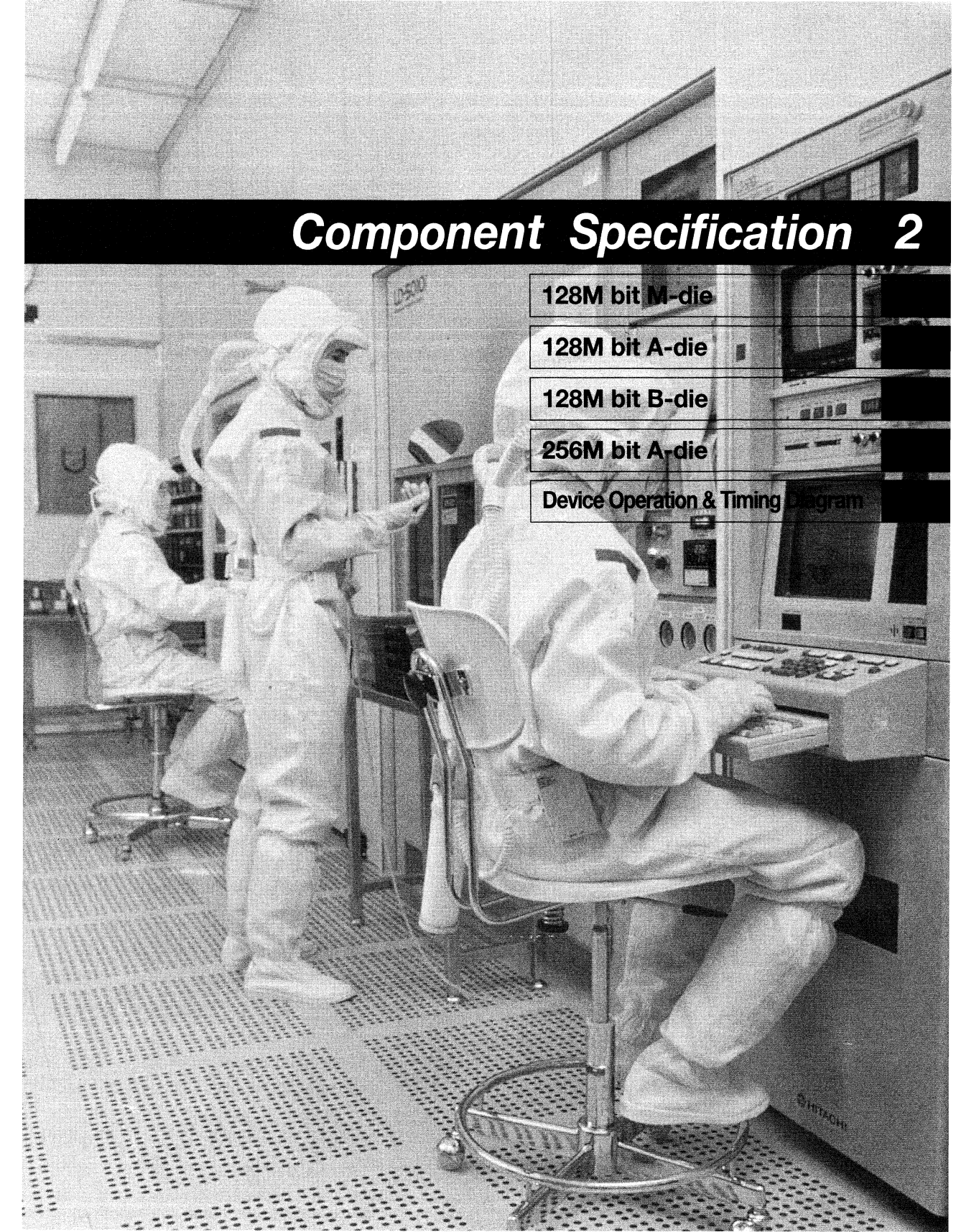
• Symbol Change Notice (128 Mb A-die / B-die)

Before		After	
I_{IL}	Input leakage current (inputs)	I_{LI}	Input leakage current
I_{IL}	Input leakage current (I/O pins)		
I_{OL}	Output open @ DC characteristic table	I_o	Output open @ DC characteristic table

• Test Condition in DC CHARACTERISTIC Change Notice (128 Mb A-die / B-die)

Symbol	Before	After
I_{CC2P}, I_{CC3P}	$CKE \leq V_{IL(max)}, t_{CC} = 15ns$	$CKE \leq V_{IL(max)}, t_{CC} = 10ns$
I_{CC2N}, I_{CC3N}	$CKE \geq V_{IH(min)}, \overline{CS} \geq V_{IH(min)}, t_{CC} = 15ns$ Input signals are changed one time during 30ns	$CKE \geq V_{IH(min)}, \overline{CS} \geq V_{IH(min)}, t_{CC} = 10ns$ Input signals are changed one time during 20ns
I_{CC4}	2 Banks activated	4 Banks activated

NOTES



Component Specification 2

128M bit M-die

128M bit A-die

128M bit B-die

256M bit A-die

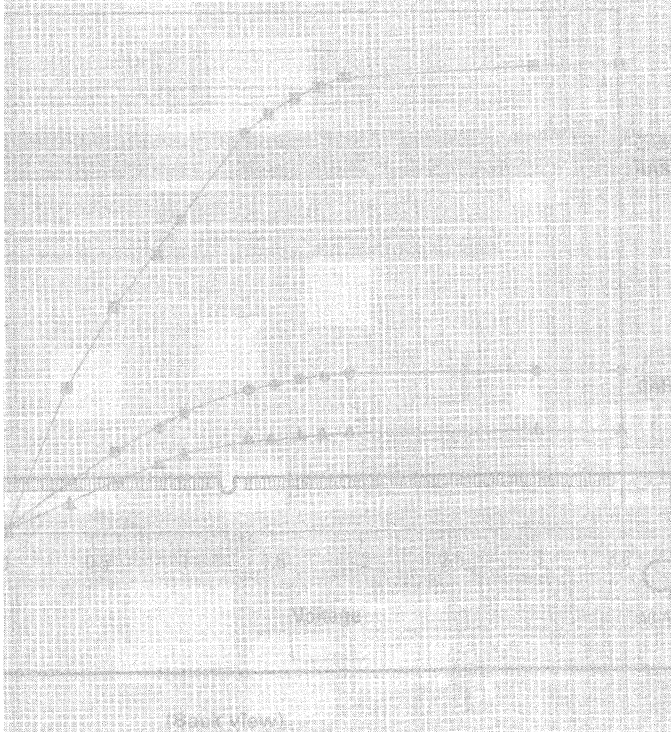
Device Operation & Timing Diagram

Component Specification

2

128M bit M-die

60MHz and 100MHz P/L Low power view



(Peak View)

RAS	001	DO1
RAS	002	DO2
DE W 001	DO3	DO4
RAS	005	DO5
RAS	006	DO6
DE W 001	DO7	DO8
RAS	009	DO9
RAS	010	DO10
DE W 001	DO11	DO12
RAS	013	DO13
RAS	014	DO14
DE W 001	DO15	DO16
RAS	017	DO17
RAS	018	DO18
DE W 001	DO19	DO20
RAS	021	DO21
RAS	022	DO22
DE W 001	DO23	DO24
RAS	025	DO25
RAS	026	DO26
DE W 001	DO27	DO28
RAS	029	DO29
RAS	030	DO30
DE W 001	DO31	DO32
RAS	033	DO33
RAS	034	DO34
DE W 001	DO35	DO36
RAS	037	DO37
RAS	038	DO38
DE W 001	DO39	DO40
RAS	041	DO41
RAS	042	DO42
DE W 001	DO43	DO44
RAS	045	DO45
RAS	046	DO46
DE W 001	DO47	DO48
RAS	049	DO49
RAS	050	DO50
DE W 001	DO51	DO52
RAS	053	DO53
RAS	054	DO54
DE W 001	DO55	DO56
RAS	057	DO57
RAS	058	DO58
DE W 001	DO59	DO60
RAS	061	DO61
RAS	062	DO62
DE W 001	DO63	DO64

DO59 DO60 DO61 DO62 DO63 DO64

8M x 4Bit x 4 Banks Synchronous DRAM**FEATURES**

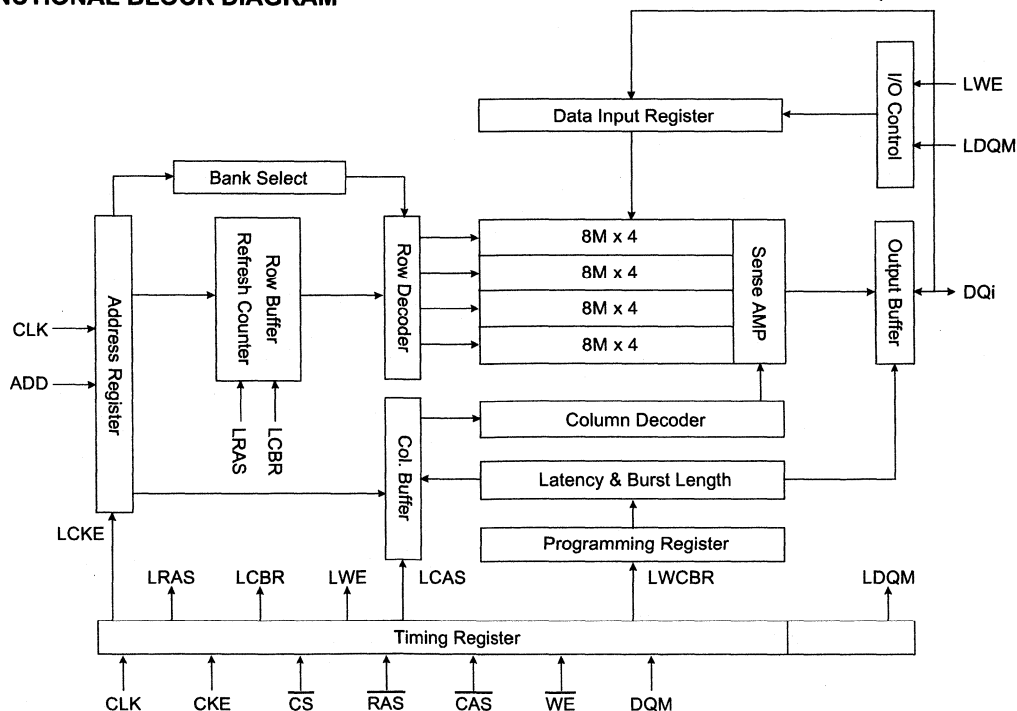
- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4 & 8 page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)

GENERAL DESCRIPTION

The K4S280432M is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 8,388,608 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

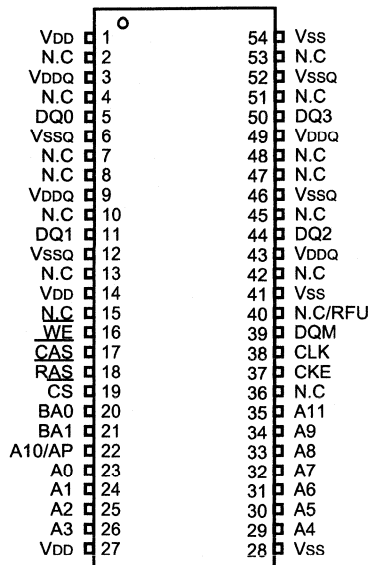
ORDERING INFORMATION

Part No.	Max Freq.	Inter-	Package
K4S280432M-TC/L80	125MHz(CL=3)	LVTTTL	54pin TSOP(II)
K4S280432M-TC/L1H	100MHz(CL=2)		
K4S280432M-TC/L1L	100MHz(CL=3)		
K4S280432M-TC/L10	66MHz(CL=2 & 3)		

FUNCTIONAL BLOCK DIAGRAM

* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{CS}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ 3	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection Reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IIL}	-1	-	1	uA	3
Input leakage current (I/O pins)	I _{IIL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ},

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Clock	C _{CLK}	2.5	4	pF
RAS, CAS, WE, CS, CKE, DQM	C _{IN}	2.5	5	pF
Address	C _{ADD}	2.5	5	pF
DQ0 ~ DQ3	C _{OUT}	4	6.5	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version				Unit	Note
				-80	-1H	-1L	-10		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		120	110	110	105	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 15ns		1				mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞		1					
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc=15ns Input signals are changed one time during 30ns		15				mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		7					
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 15ns		5				mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞		5					
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns.		30				mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		20				mA	
Operating current (Burst mode)	Icc4	IOL = 0 mA Page burst tccd = 2CLKs	3	140	115	115	115	mA	1
			2	105	115	105	105		
Refresh current	Icc5	trc ≥ trc(min)		200			165	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	C	1.5				mA	3
			L	800				uA	4

Notes : 1. Measured with outputs open.

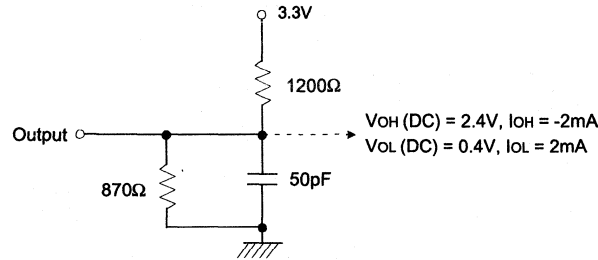
2. Refresh period is 64ms.

3. K4S280432M-C**

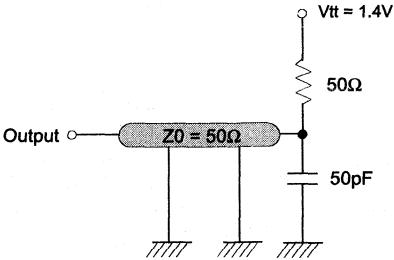
4. K4S280432M-L**

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
Input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			-80	-1H	-1L	-10		
Row active to row active delay		tRRD(min)	16	20	20	20	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay		tRCD(min)	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	24	ns	1
Row active time		tRAS(min)	48	50	50	50	ns	1
		tRAS(max)	100				us	
Row cycle time		tRC(min)	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	8	10	10	12	ns	2
Last data in to new col. address delay		tCDL(min)	1				CLK	2
Last data in to burst stop		tBDL(min)	1				CLK	2
Col. address to col. address delay		tCCD(min)	1				CLK	3
Number of valid output data	CAS latency=3	2				ea	4	
	CAS latency=2	1						

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-80		-1H		-1L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6		7	ns	1,2
	CAS latency=2			6		6		7		7		
Output data hold time	CAS latency=3	tOH	3		3		3		3		ns	2
	CAS latency=2		3		3		3		3			
CLK high pulse width		tCH	3		3		3		3.5		ns	3
CLK low pulse width		tCL	3		3		3		3.5		ns	3
Input setup time		tSS	2		2		2		2.5		ns	3
Input hold time		tSH	1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6		7	ns	
	CAS latency=2			6		6		7		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

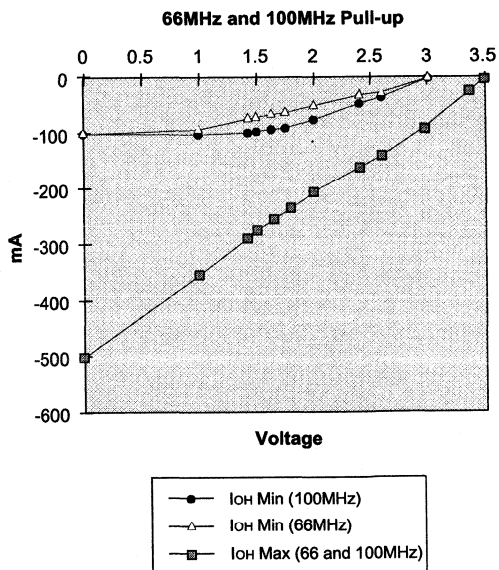
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :**
- Rise time specification based on $0pF + 50 \ \Omega$ to V_{SS} , use these values to design to.
 - Fall time specification based on $0pF + 50 \ \Omega$ to V_{DD} , use these values to design to.
 - Measured into $50pF$ only, use these values to characterize to.
 - All measurements done with respect to V_{SS} .

IBIS SPECIFICATION

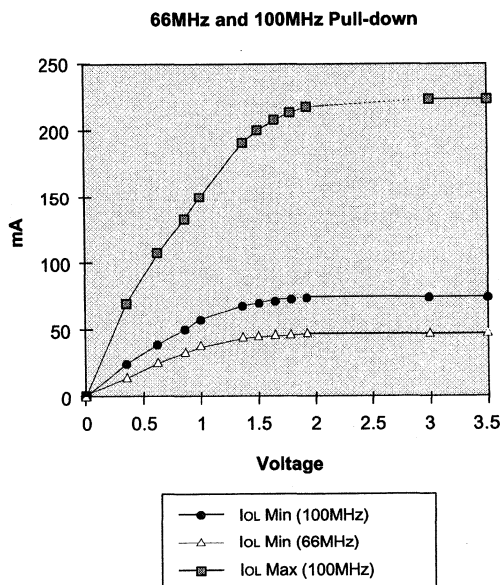
IOH Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



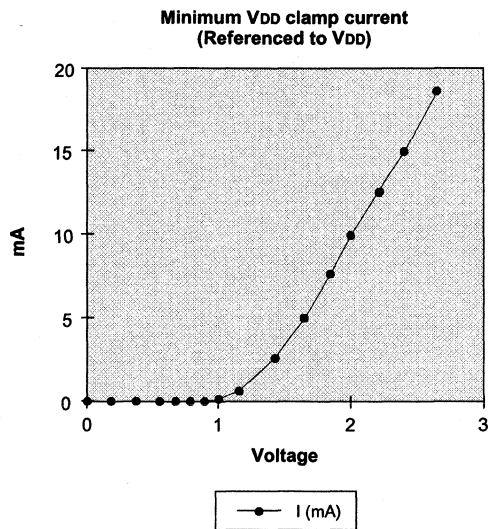
IOL Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

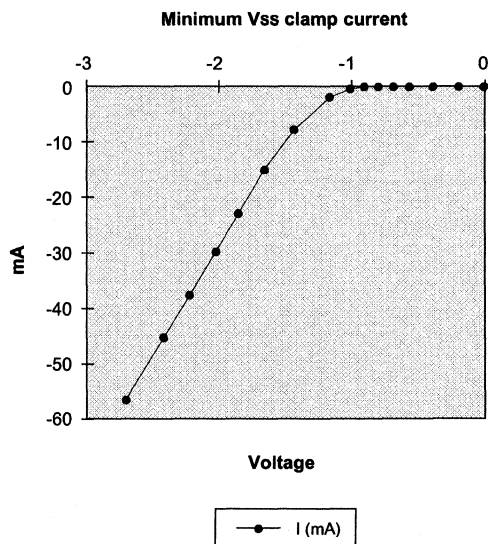


V_{DD} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**V_{SS} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ**

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L							3		
		Exit	L	H	L	H	H	H	X	X	3		
					H	X	X	X			3		
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

4M x 8Bit x 4 Banks Synchronous DRAM**FEATURES**

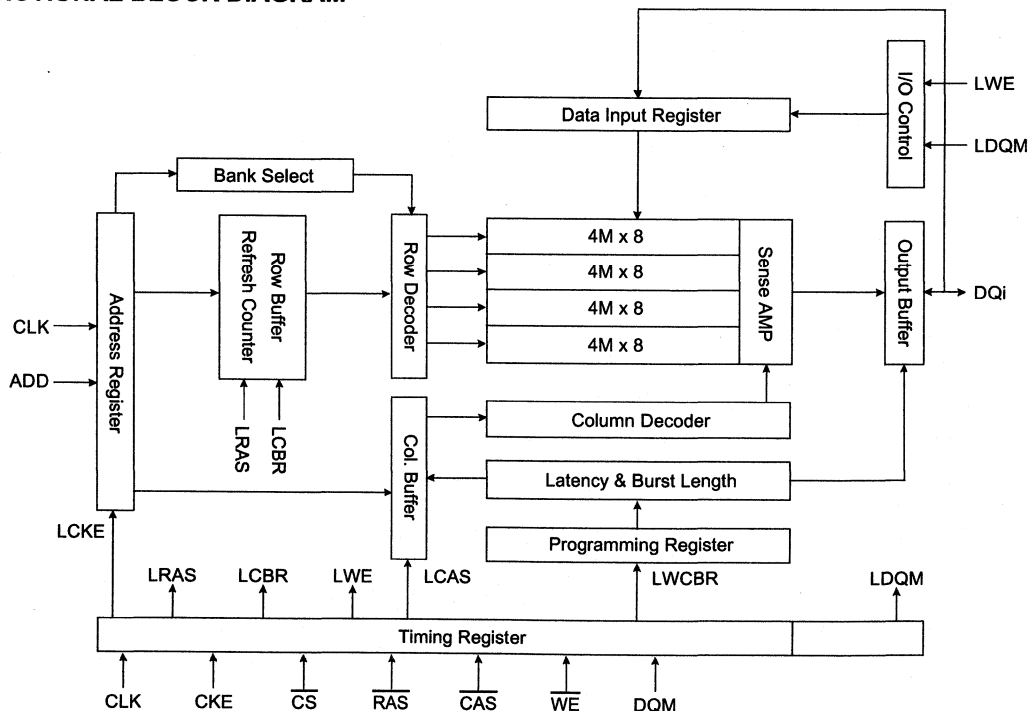
- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

GENERAL DESCRIPTION

The K4S280832M is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 4,194,304 words by 8 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

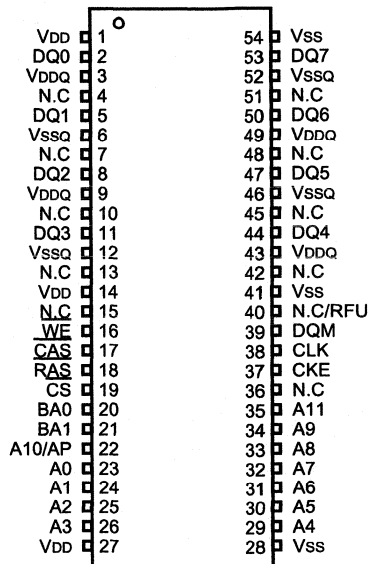
ORDERING INFORMATION

Part No.	Max Freq.	Inter-	Package
K4S280832M-TC/L80	125MHz(CL=3)	LVTTTL	54pin TSOP(II)
K4S280832M-TC/L1H	100MHz(CL=2)		
K4S280832M-TC/L1L	100MHz(CL=3)		
K4S280832M-TC/L10	66MHz(CL=2 & 3)		

FUNCTIONAL BLOCK DIAGRAM

* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ 7	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C./RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _d	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-1	-	1	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ,
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ VDDQ.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Clock	CCLK	2.5	4	pF
RAS, CAS, WE, CS, CKE, DQM	CIN	2.5	5	pF
Address	CADD	2.5	5	pF
DQ0 ~ DQ3	COUT	4	6.5	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version				Unit	Note
				-80	-1H	-1L	-10		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		120	110	110	105	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 15ns		1				mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞		1					
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc=15ns Input signals are changed one time during 30ns		15				mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		7					
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 15ns		5				mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞		5					
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 15ns Input signals are changed one time during 30ns.		30				mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		20				mA	
Operating current (Burst mode)	Icc4	IOL = 0 mA Page burst tccd = 2CLKs	3	150	125	125	125	mA	1
			2	115	125	115	115		
Refresh current	Icc5	trc ≥ trc(min)		200			165	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	C	1.5				mA	3
			L	800				uA	4

Notes : 1. Measured with outputs open.

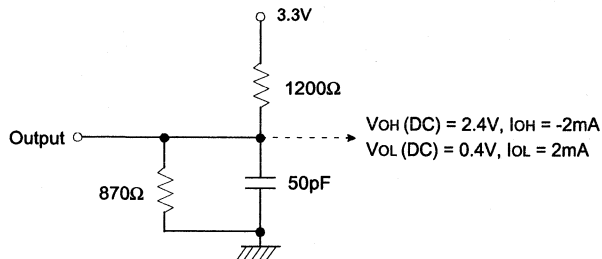
2. Refresh period is 64ms.

3. K4S280832M-TC**

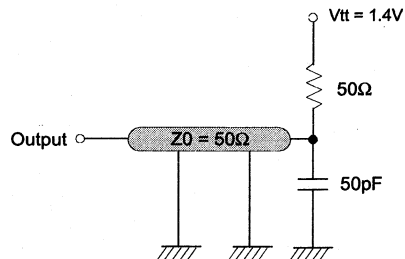
4. K4S280832M-TL**

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			-80	-1H	-1L	-10		
Row active to row active delay		tRRD(min)	16	20	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	24	ns	1
Row active time		tRAS(min)	48	50	50	50	ns	1
		tRAS(max)	100				us	
Row cycle time		tRC(min)	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	8	10	10	12	ns	2
Last data in to new col. address delay		tCDL(min)	1				CLK	2
Last data in to burst stop		tBDL(min)	1				CLK	2
Col. address to col. address delay		tCCD(min)	1				CLK	3
Number of valid output data	CAS latency=3	2					ea	4
	CAS latency=2	1						

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-80		-1H		-1L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12		13			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6		7	ns	1,2
	CAS latency=2			6		6		7		7		
Output data hold time	CAS latency=3	toH	3		3		3		3		ns	2
	CAS latency=2		3		3		3		3			
CLK high pulse width		tCH	3		3		3		3.5		ns	3
CLK low pulse width		tCL	3		3		3		3.5		ns	3
Input setup time		tSS	2		2		2		2.5		ns	3
Input hold time		tSH	1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6		7	ns	
	CAS latency=2			6		6		7		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1$ ns.
If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

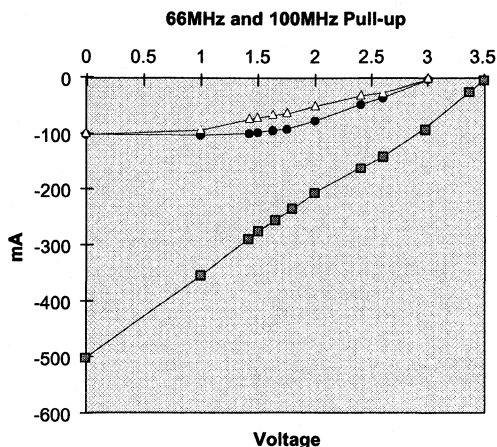
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :**
- Rise time specification based on 0pF + 50 Ω to Vss, use these values to design to.
 - Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
 - Measured into 50pF only, use these values to characterize to.
 - All measurements done with respect to Vss.

IBIS SPECIFICATION

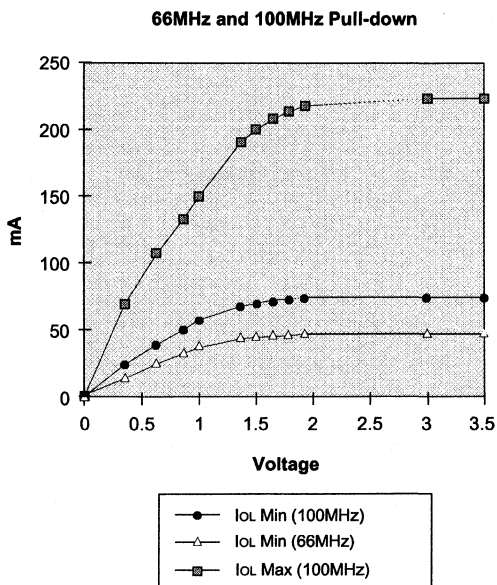
IOH Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



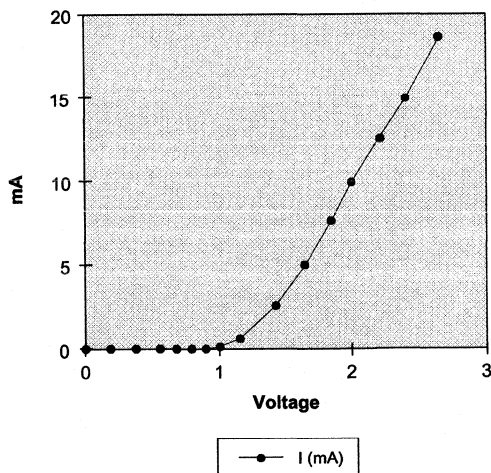
IOL Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

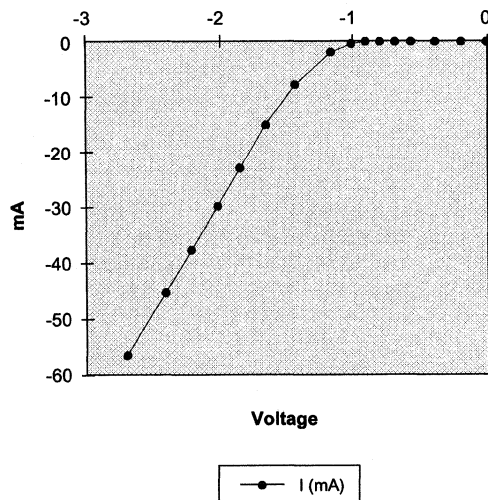


V_{DD} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**Minimum V_{DD} clamp current
(Referenced to V_{DD})****V_{SS} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ**

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

Minimum V_{SS} clamp current

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

2M x 16Bit x 4 Banks Synchronous DRAM**FEATURES**

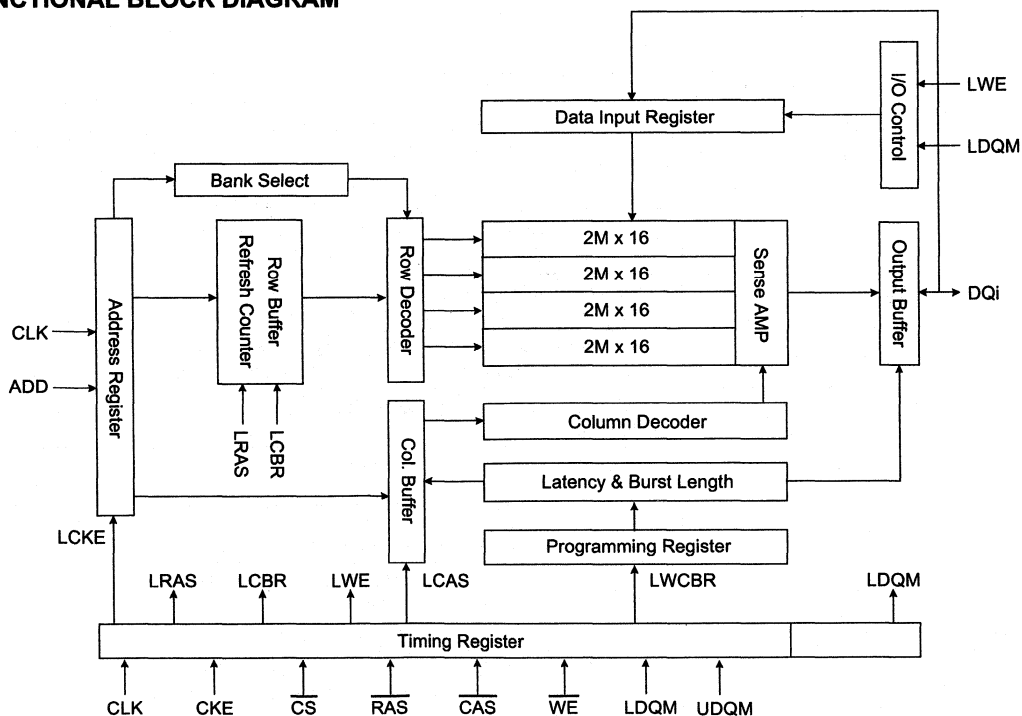
- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

GENERAL DESCRIPTION

The K4S281632M is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 2,097,152 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

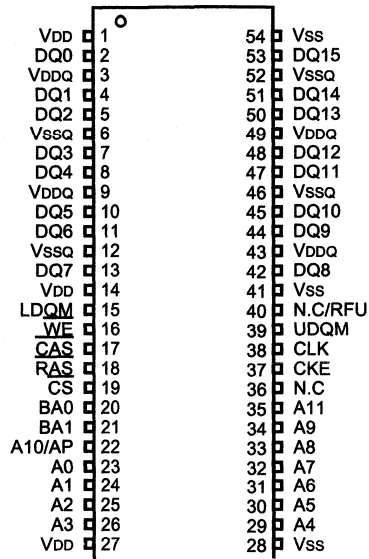
ORDERING INFORMATION

Part No.	Max Freq.	Inter-	Package
K4S281632M-TC/L80	125MHz(CL=3)	LVTTTL	54pin TSOP(II)
K4S281632M-TC/L1H	100MHz(CL=2)		
K4S281632M-TC/L1L	100MHz(CL=3)		
K4S281632M-TC/L10	66MHz(CL=2 & 3)		

FUNCTIONAL BLOCK DIAGRAM

* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
L(U)DQM	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ 15	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-1	-	1	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ,
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, 0V ≤ V_{OUT} ≤ VDDQ.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Clock	CCLK	2.5	4	pF
RAS, CAS, WE, CS, CKE, DQM	CIN	2.5	5	pF
Address	CADD	2.5	5	pF
DQ0 ~ DQ3	COUT	4	6.5	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version				Unit	Note
				-80	-1H	-1L	-10		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IoL = 0 mA		130	120	120	115	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		1				mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		1					
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc=15ns Input signals are changed one time during 30ns		15				mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		7					
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		5				mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		5					
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 15ns Input signals are changed one time during 30ns.		30				mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		20				mA	
Operating current (Burst mode)	ICC4	IoL = 0 mA Page burst tccd = 2CLKs	3	170	145	145	145	mA	1
			2	135	145	135	135		
Refresh current	ICC5	trc ≥ trc(min)		200			165	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	C	1.5				mA	3
			L	800				uA	4

Notes : 1. Measured with outputs open.

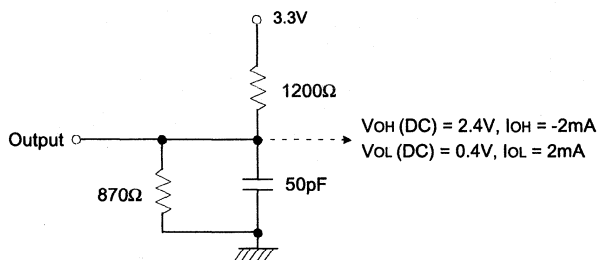
2. Refresh period is 64ms.

3. K4S281632M-TC**

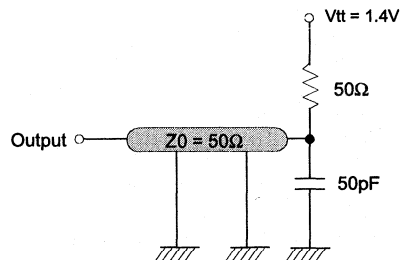
4. K4S281632M-TL**

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			-80	-1H	-1L	-10		
Row active to row active delay		tRRD(min)	16	20	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	24	ns	1
Row active time		tRAS(min)	48	50	50	50	ns	1
		tRAS(max)	100				us	
Row cycle time		tRC(min)	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	8	10	10	12	ns	2
Last data in to new col. address delay		tCDL(min)	1				CLK	2
Last data in to burst stop		tBDL(min)	1				CLK	2
Col. address to col. address delay		tCCD(min)	1				CLK	3
Number of valid output data	CAS latency=3	2					ea	4
	CAS latency=2	1						

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-80		-1H		-1L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12		13			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6		7	ns	1,2
	CAS latency=2			6		6		7		7		
Output data hold time	CAS latency=3	tOH	3		3		3		3		ns	2
	CAS latency=2		3		3		3		3			
CLK high pulse width		tCH	3		3		3		3.5		ns	3
CLK low pulse width		tCL	3		3		3		3.5		ns	3
Input setup time		tSS	2		2		2		2.5		ns	3
Input hold time		tSH	1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6		7	ns	
	CAS latency=2			6		6		7		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

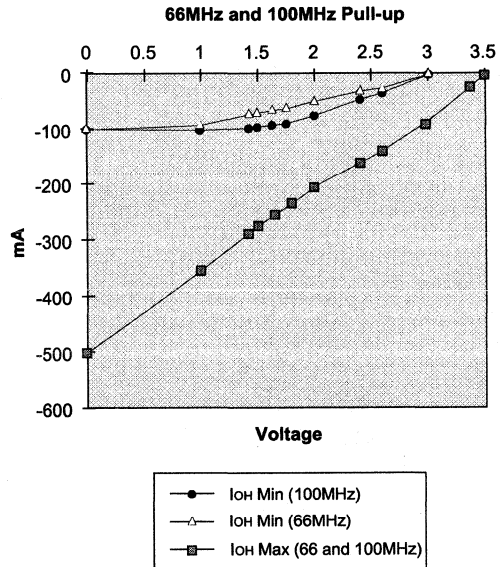
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :**
- Rise time specification based on 0pF + 50 Ω to Vss, use these values to design to.
 - Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
 - Measured into 50pF only, use these values to characterize to.
 - All measurements done with respect to Vss.

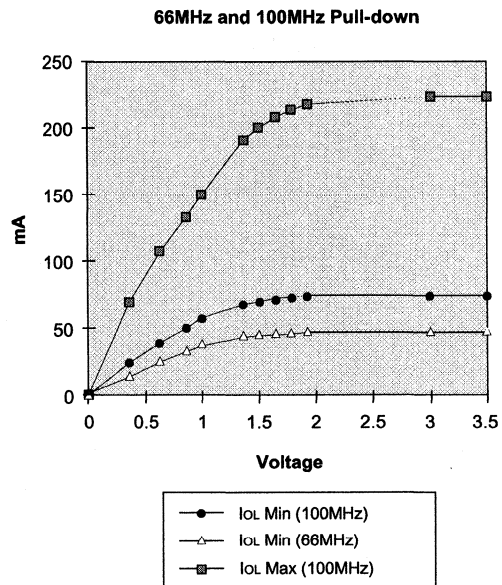
IBIS SPECIFICATION

I_{OH} Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0

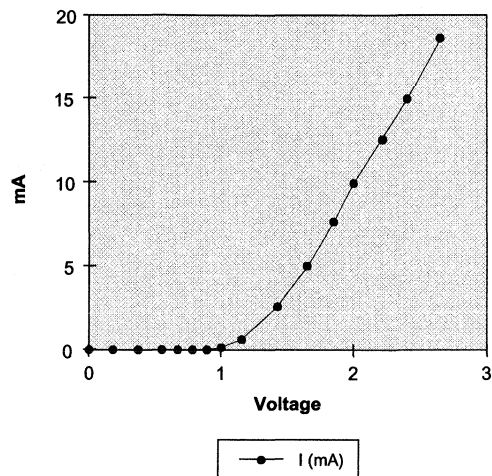
I_{OL} Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

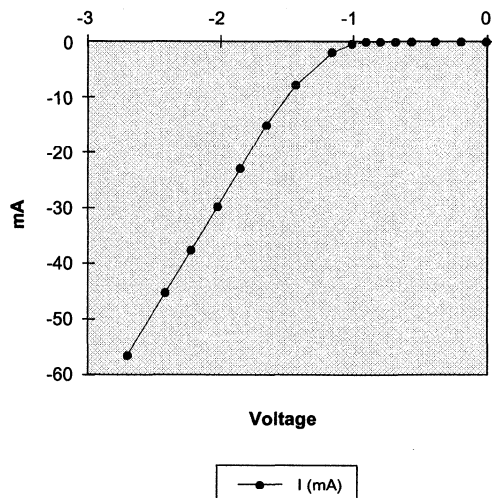


V_{DD} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**Minimum V_{DD} clamp current
(Referenced to V_{DD})****V_{SS} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ**

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

Minimum V_{SS} clamp current

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3	
	Entry		L	L	L	L	H	X	X			3	
	Self fefresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4	
	Auto precharge enable									H		4,5	
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4	
	Auto precharge enable									H		4,5	
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X		
	All banks								X	H			
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A_{10/AP} is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

NOTES

Component Specification

2

128M bit A-die

000000 and 100MHz Pull-downs (front view)

(Back view)

CAS	U	DQ1	DQ0
RAS	U	DQ2	DQ1
OE W A0 A1	DQ3	DQ3	DQ3
CAS	U	DQ1	DQ4
RAS	U	DQ2	DQ5
OE W A0 A1	DQ3	DQ6	DQ7
CAS	U	DQ1	DQ8
RAS	U	DQ2	DQ9
OE W A0 A1	DQ3	DQ10	DQ11
CAS	U	DQ1	DQ12
RAS	U	DQ2	DQ13
OE W A0 A1	DQ3	DQ14	DQ15
CAS	U	DQ1	DQ16
RAS	U	DQ2	DQ17
OE W A0 A1	DQ3	DQ18	DQ19
CAS	U	DQ1	DQ20
RAS	U	DQ2	DQ21
OE W A0 A1	DQ3	DQ22	DQ23
CAS	U	DQ1	DQ24
RAS	U	DQ2	DQ25
OE W A0 A1	DQ3	DQ26	DQ27
CAS	U	DQ1	DQ28
RAS	U	DQ2	DQ29
OE W A0 A1	DQ3	DQ30	DQ31
CAS	U	DQ1	DQ32
RAS	U	DQ2	DQ33
OE W A0 A1	DQ3	DQ34	DQ35

$V_{DD} = 0.050 \pm 0.003$
 $V_{SS} = 0.000 \pm 0.003$
 1. For 0.1µF capacitor for each DRAM
 To all DRAMs

8M x 4Bit x 4 Banks Synchronous DRAM**FEATURES**

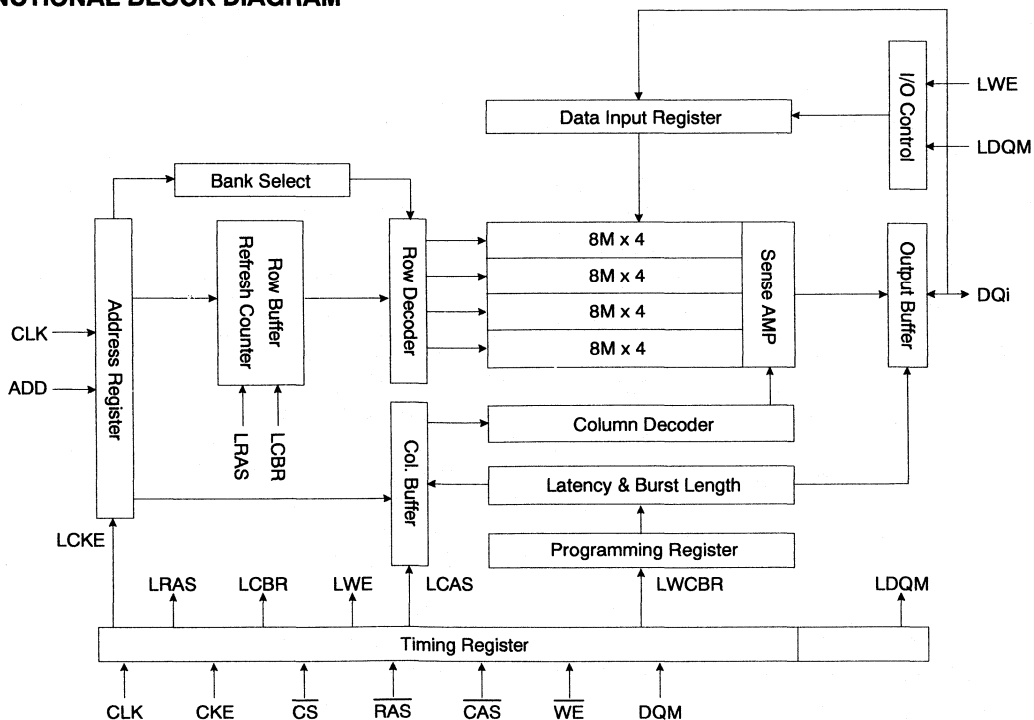
- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 Page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)

GENERAL DESCRIPTION

The K4S280432A is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 8,388,608 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

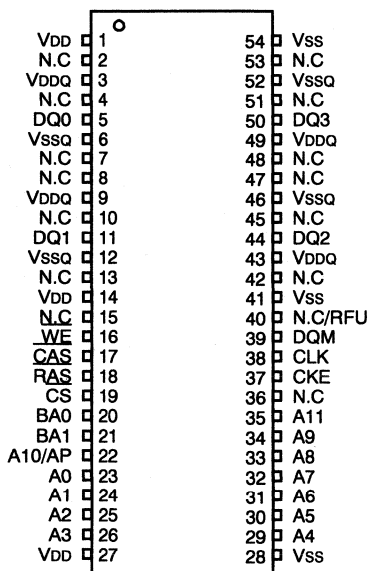
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S280432A-TC/L75	133MHz(CL=3)	LVTTTL	54 TSOP(II)
K4S280432A-TC/L80	125MHz(CL=3)		
K4S280432A-TC/L1H	100MHz(CL=2)		
K4S280432A-TC/L1L	100MHz(CL=3)		
K4S280432A-TC/L10	66MHz(CL=2 & 3)		

FUNCTIONAL BLOCK DIAGRAM

* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ 3	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ},
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C _{CLK}	2.5	4.0	pF	1
RAS, CAS, WE, CS, CE, DQM	C _{IN}	2.5	5.0	pF	2
Address	C _{ADD}	2.5	5.0	pF	2
DQ0 ~ DQ3	C _{OUT}	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF
2. -75 only specify a maximum value of 3.8pF
3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version					Unit	Note	
			-75	-80	-1H	-1L	-10			
Operating current (One bank active)	ICC1	Burst length = 1 tRC ≥ tRC(min) IO = 0 mA	120	120	110	110	110	mA	1	
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tCC = 10ns	1					mA		
	ICC2PS	CKE & CLK ≤ VIL(max), tCC = ∞	1							
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tCC = 10ns Input signals are changed one time during 20ns	20					mA		
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tCC = ∞ Input signals are stable	7							
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tCC = 10ns	5					mA		
	ICC3PS	CKE & CLK ≤ VIL(max), tCC = ∞	5							
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tCC = 10ns Input signals are changed one time during 20ns	30					mA		
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tCC = ∞ Input signals are stable	20					mA		
Operating current (Burst mode)	ICC4	IO = 0 mA Page burst 4Banks Activated tCCD = 2CLKs	140	135	115	115	115	mA	1	
Refresh current	ICC5	tRC ≥ tRC(min)	220	220	210	210	210	mA	2	
Self refresh current	ICC6	CKE ≤ 0.2V	C	1.5					mA	3
			L	800					uA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

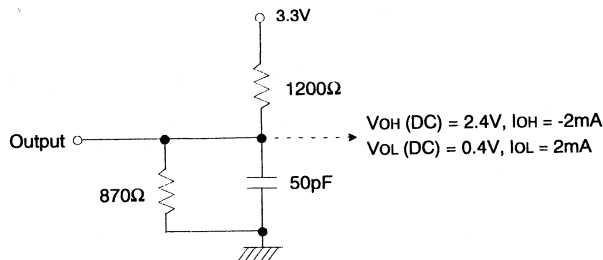
3. K4S280432A-TC**

4. K4S280432A-TL**

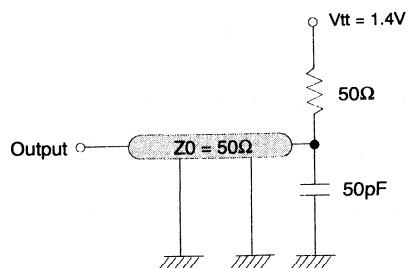
5. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
Input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			- 75	- 80	- 1H	- 1L	-10		
Row active to row active delay		tRRD(min)	15	16	20	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	20	24	ns	1
Row active time		tRAS(min)	45	48	50	50	50	ns	1
		tRAS(max)	100					us	
Row cycle time		tRC(min)	65	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	2					CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns					-	5
Last data in to new col. address delay		tCDL(min)	1					CLK	2
Last data in to burst stop		tBDL(min)	1					CLK	2
Col. address to col. address delay		tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3	2					ea	4	
	CAS latency=2	-		1					

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L/10, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported.

SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 75		- 80		- 1H		- 1L		- 10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12		13			
CLK to valid output delay	CAS latency=3	tsAC		5.4		6		6		6		7	ns	1,2
	CAS latency=2			-		-		6		7		7		
Output data hold time	CAS latency=3	tOH	2.7		3		3		3		3		ns	2
	CAS latency=2		-		-		3		3		3			
CLK high pulse width		tCH	2.5		3		3		3		3.5		ns	3
CLK low pulse width		tCL	2.5		3		3		3		3.5		ns	3
Input setup time		tSS	1.5		2		2		2		2.5		ns	3
Input hold time		tSH	0.8		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6		7	ns	
	CAS latency=2			-		-		6		7		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr + tf) = 1ns$.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

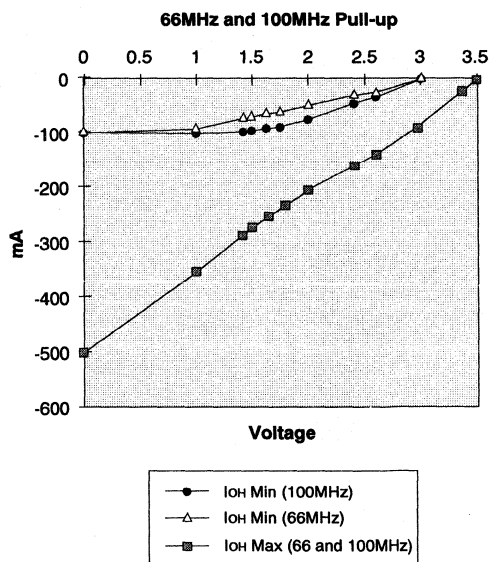
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :**
- Rise time specification based on 0pF + 50 Ω to Vss, use these values to design to.
 - Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
 - Measured into 50pF only, use these values to characterize to.
 - All measurements done with respect to Vss.

IBIS SPECIFICATION

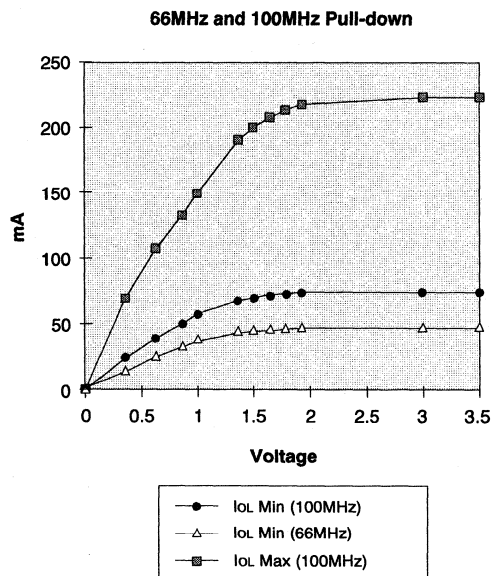
IOH Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



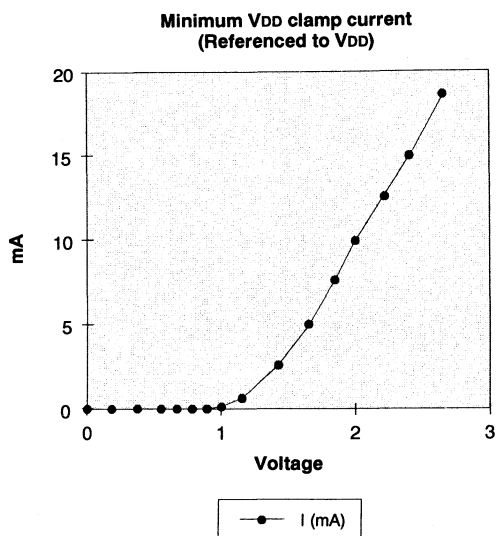
IOL Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

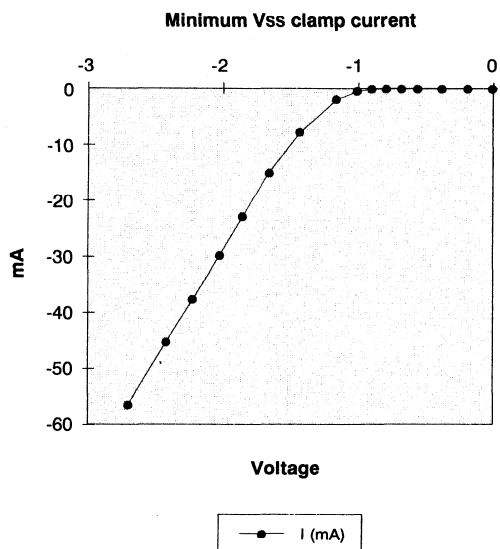


V_{DD} Clamp @ CLK, CKE, CS, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

V_{SS} Clamp @ CLK, CKE, CS, DQM & DQ

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X	X	3	
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H			4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H			4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

4M x 8Bit x 4 Banks Synchronous DRAM**FEATURES**

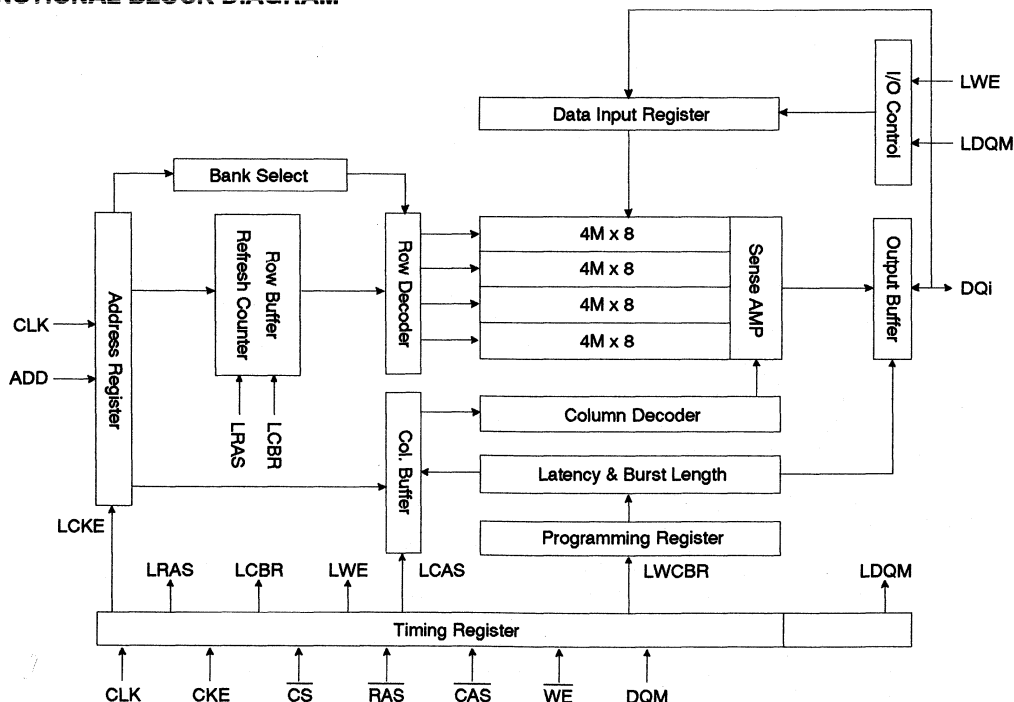
- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

GENERAL DESCRIPTION

The K4S280832A is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 4,194,304 words by 8 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

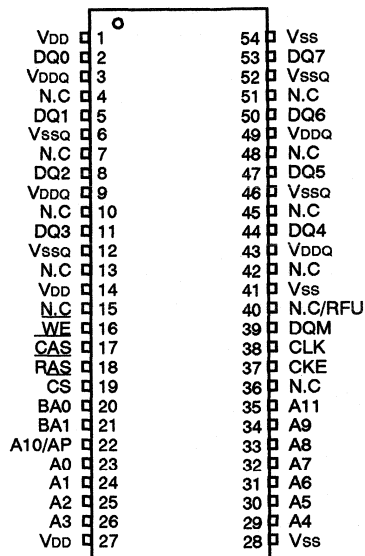
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S280832A-TC/L75	133MHz(CL=3)	LVTTL	54 TSOP(II)
K4S280832A-TC/L80	125MHz(CL=3)		
K4S280832A-TC/L1H	100MHz(CL=2)		
K4S280832A-TC/L1L	100MHz(CL=3)		
K4S280832A-TC/L10	66MHz(CL=2 & 3)		

FUNCTIONAL BLOCK DIAGRAM

* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A ₀ ~ A ₁₁	Address	Row/column addresses are multiplexed on the same pins. Row address : RA ₀ ~ RA ₁₁ , Column address : CA ₀ ~ CA ₉
BA ₀ ~ BA ₁	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
WE	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
DQ ₀ ~ 7	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/Vssq	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ},
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C _{CLK}	2.5	4.0	pF	1
RAS, CAS, WE, CS, CKE, DQM	C _{IN}	2.5	5.0	pF	2
Address	C _{ADD}	2.5	5.0	pF	2
DQ0 ~ DQ7	C _{OUT}	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF
2. -75 only specify a maximum value of 3.8pF
3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Sym- bol	Test Condition	Version					Unit	Not e	
			-75	-80	-1H	-1L	-10			
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	120	120	110	110	110	mA	1	
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	1					mA		
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	1							
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	20					mA		
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	7							
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	5					mA		
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	5							
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	30					mA		
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	20					mA		
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4Banks Activated tccd = 2CLKs	150	145	125	125	125	mA	1	
Refresh current	Icc5	trc ≥ trc(min)	220	220	210	210	210	mA	2	
Self refresh current	Icc6	CKE ≤ 0.2V	C	1.5					mA	3
			L	800					uA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

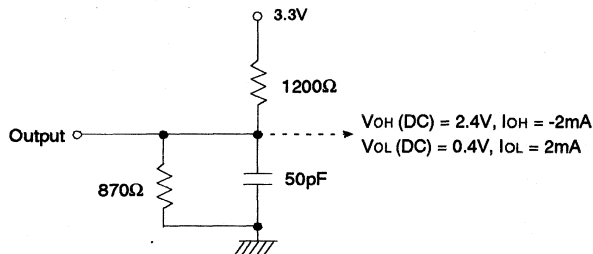
3. K4S280832A-TC**

4. K4S280832A-TL**

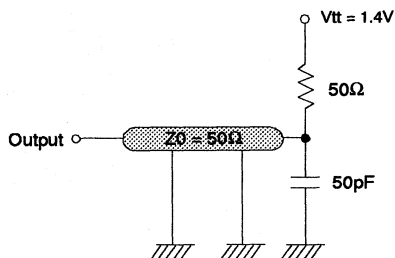
5. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			- 75	- 80	- 1H	- 1L	-10		
Row active to row active delay		tRRD(min)	15	16	20	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	20	24	ns	1
Row active time		tRAS(min)	45	48	50	50	50	ns	1
		tRAS(max)	100					us	
Row cycle time		tRC(min)	65	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	2					CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns					-	5
Last data in to new col. address delay		tCDL(min)	1					CLK	2
Last data in to burst stop		tBDL(min)	1					CLK	2
Col. address to col. address delay		tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3		2					ea	4
	CAS latency=2		-		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L/10, $t_{RDL}=1\text{ CLK}$ and $t_{DAL}=1\text{ CLK}+20\text{ ns}$ is also supported .

SAMSUNG recommends $t_{RDL}=2\text{ CLK}$ and $t_{DAL}=2\text{ CLK} + 20\text{ ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 75		- 60		- 1H		- 1L		- 10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		5.4		6		6		6		7	ns	1,2
	CAS latency=2			-		-		6		7		7		
Output data hold time	CAS latency=3	tOH	2.7		3		3		3		3		ns	2
	CAS latency=2		-		-		3		3		3			
CLK high pulse width		tCH	2.5		3		3		3		3.5		ns	3
CLK low pulse width		tCL	2.5		3		3		3		3.5		ns	3
Input setup time		tSS	1.5		2		2		2		2.5		ns	3
Input hold time		tSH	0.8		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6		7	ns	
	CAS latency=2			-		-		6		7		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.
 - Assumed input rise and fall time (t_r & t_f) = 1ns.
If t_r & t_f is longer than 1ns, transient time compensation should be considered, i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

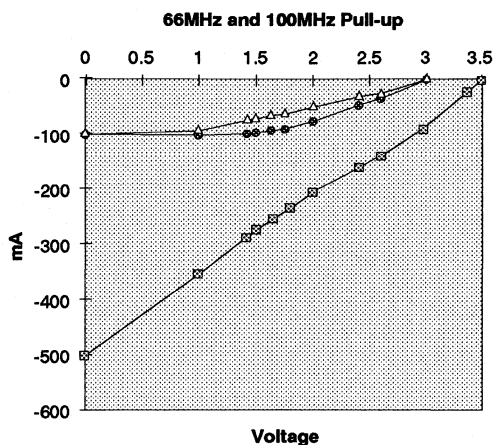
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	t _{rh}	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	t _{fh}	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	t _{rh}	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	t _{fh}	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :**
- Rise time specification based on 0pF + 50 Ω to V_{SS}, use these values to design to.
 - Fall time specification based on 0pF + 50 Ω to V_{DD}, use these values to design to.
 - Measured into 50pF only, use these values to characterize to.
 - All measurements done with respect to V_{SS}.

IBIS SPECIFICATION

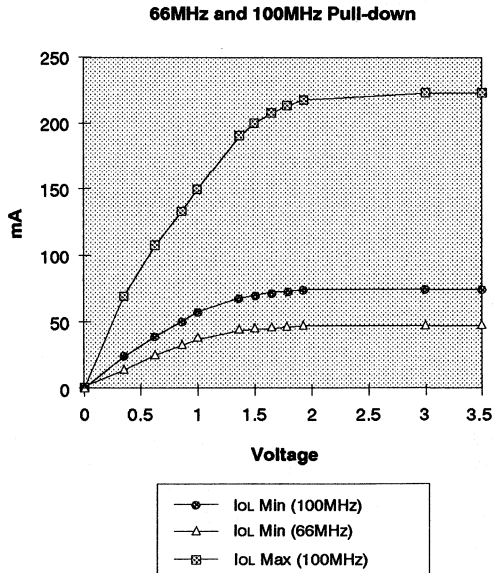
IOH Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



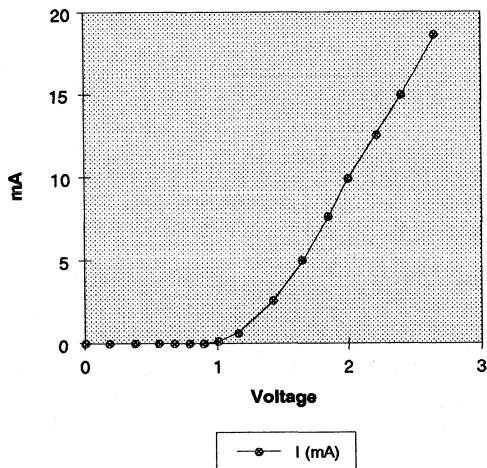
IOL Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

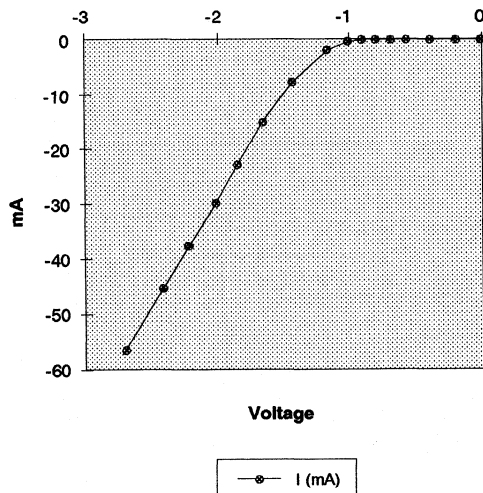


V_{DD} Clamp @ CLK, CKE, CS, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

Minimum V_{DD} clamp current
(Referenced to V_{DD})V_{SS} Clamp @ CLK, CKE, CS, DQM & DQ

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

Minimum V_{SS} clamp current

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A9 ~ A0)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A9 ~ A0)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Component Specification

2

128M bit B-die

50MHz and 100MHz Full down (front view)

Voltage

(Back view)

RAS	W	Q01	Q01
OE	W	Q02	Q02
CAS	W	Q03	Q03
OE	W	Q04	Q04
RAS	W	Q05	Q05
OE	W	Q06	Q06
CAS	W	Q07	Q07
OE	W	Q08	Q08
RAS	W	Q09	Q09
OE	W	Q10	Q10
CAS	W	Q11	Q11
OE	W	Q12	Q12
RAS	W	Q13	Q13
OE	W	Q14	Q14
CAS	W	Q15	Q15
OE	W	Q16	Q16
RAS	W	Q17	Q17
OE	W	Q18	Q18
CAS	W	Q19	Q19
OE	W	Q20	Q20
RAS	W	Q21	Q21
OE	W	Q22	Q22
CAS	W	Q23	Q23
OE	W	Q24	Q24
RAS	W	Q25	Q25
OE	W	Q26	Q26
CAS	W	Q27	Q27
OE	W	Q28	Q28
RAS	W	Q29	Q29
OE	W	Q30	Q30
CAS	W	Q31	Q31
OE	W	Q32	Q32
RAS	W	Q33	Q33
OE	W	Q34	Q34

120MHz (0.09A)

0.050-0.023

0.270-0.10

VDD

VSS

0.1 and 2.2 Capacitors for each VDD/VSS

Total DRAMs

8M x 4Bit x 4 Banks Synchronous DRAM**FEATURES**

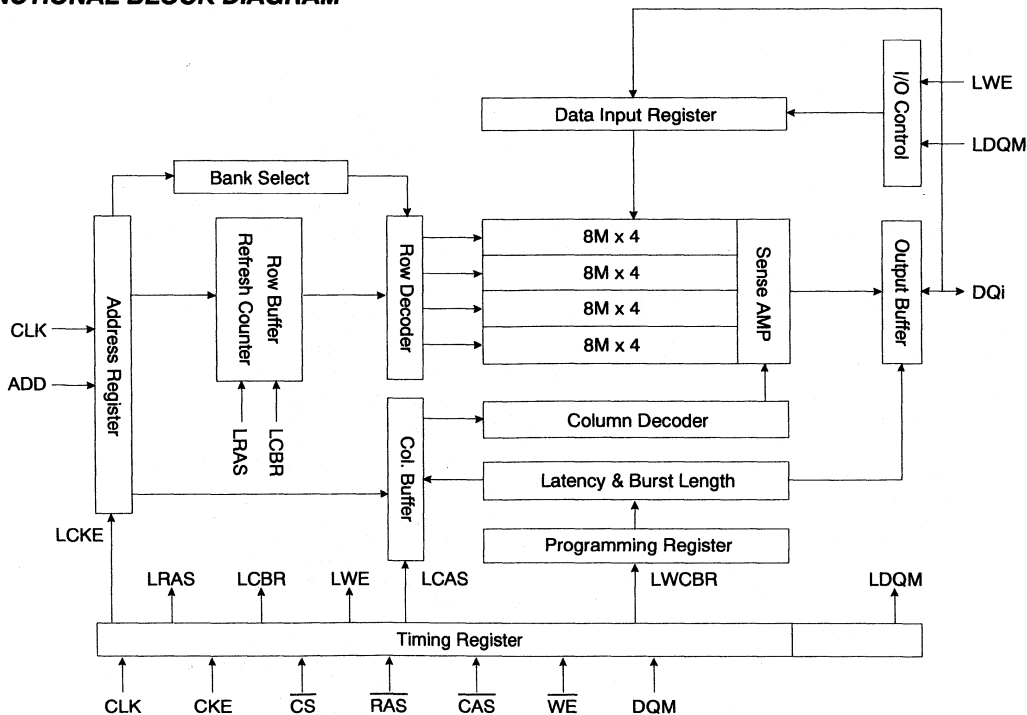
- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4 & 8 Page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)

GENERAL DESCRIPTION

The K4S280432B is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 8,388,608 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

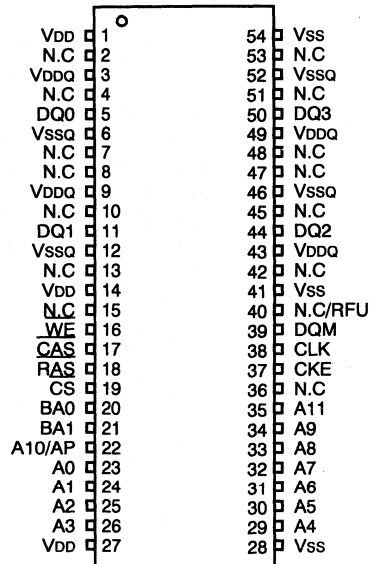
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S280432B-TC/L75	133MHz(CL=3)	LVTTTL	54 TSOP(II)
K4S280432B-TC/L80	125MHz(CL=3)		
K4S280432B-TC/L1H	100MHz(CL=2)		
K4S280432B-TC/L1L	100MHz(CL=3)		
K4S280432B-TC/L10	66MHz(CL=2 & 3)		

FUNCTIONAL BLOCK DIAGRAM

* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ 3	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDD+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ,
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	CCLK	2.5	4.0	pF	1
RAS, CAS, WE, CS, CKE, DQM	CIN	2.5	5.0	pF	2
Address	CADD	2.5	5.0	pF	2
DQ0 ~ DQ3	COUT	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF
2. -75 only specify a maximum value of 3.8pF
3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version					Unit	Note
			-75	-80	-1H	-1L	-10		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	120	120	110	110	110	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	1					mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	1						
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	20					mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	7						
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	5					mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	5						
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	30					mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	20					mA	
Operating current (Burst mode)	ICC4	Io = 0 mA Page burst 4Banks Activated tccd = 2CLKs	140	135	115	115	115	mA	1
Refresh current	ICC5	trc ≥ trc(min)	220	220	210	210	210	mA	2
Self refresh current	ICC6	C	1.5					mA	3
		L	800					uA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

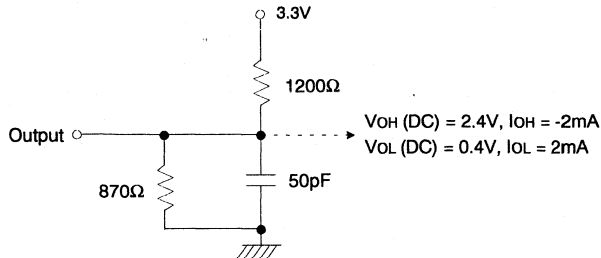
3. K4S280432B-TC**

4. K4S280432B-TL**

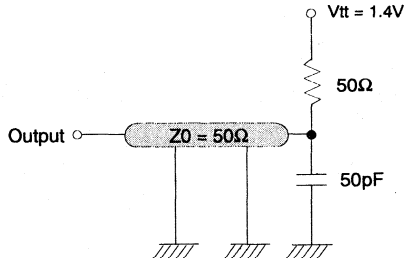
5. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
Input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			- 75	- 80	- 1H	-1 L	-10		
Row active to row active delay		tRRD(min)	15	16	20	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	20	24	ns	1
Row active time		tRAS(min)	45	48	50	50	50	ns	1
		tRAS(max)	100					us	
Row cycle time		tRC(min)	65	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	2					CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns					-	5
Last data in to new col. address delay		tCDL(min)	1					CLK	2
Last data in to burst stop		tBDL(min)	1					CLK	2
Col. address to col. address delay		tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3	2					ea	4	
	CAS latency=2	-		1					

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -80/1H/1L/10, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .
SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 75		- 80		- 1H		-1 L		- 10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	7.5	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12		13			
CLK to valid output delay	CAS latency=3	tsac		5.4		6		6		6		7	ns	1,2
	CAS latency=2			-		-		6		7		7		
Output data hold time	CAS latency=3	toH	2.7		3		3		3		3		ns	2
	CAS latency=2		-		-		3		3		3			
CLK high pulse width		tCH	2.5		3		3		3		3.5		ns	3
CLK low pulse width		tCL	2.5		3		3		3		3.5		ns	3
Input setup time		tSS	1.5		2		2		2		2.5		ns	3
Input hold time		tSH	0.8		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6		7	ns	
	CAS latency=2			-		-		6		7		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr + tf) = 1ns$.
If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tth	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tth	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

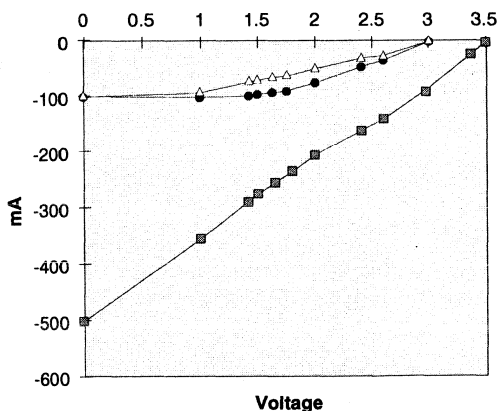
- Notes :**
- Rise time specification based on 0pF + 50 Ω to Vss, use these values to design to.
 - Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
 - Measured into 50pF only, use these values to characterize to.
 - All measurements done with respect to Vss.

IBIS SPECIFICATION

IOH Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0

66MHz and 100MHz Pull-up

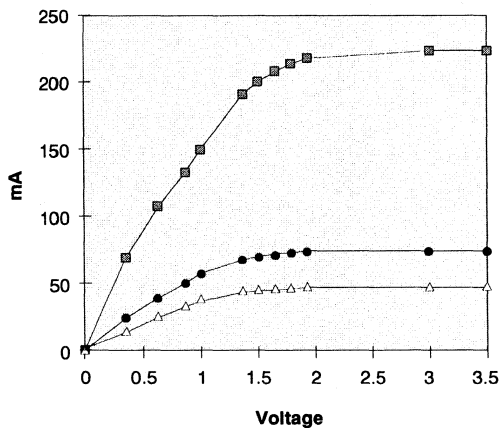


● IOH Min (100MHz)
 △ IOH Min (66MHz)
 ■ IOH Max (66 and 100MHz)

IOL Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

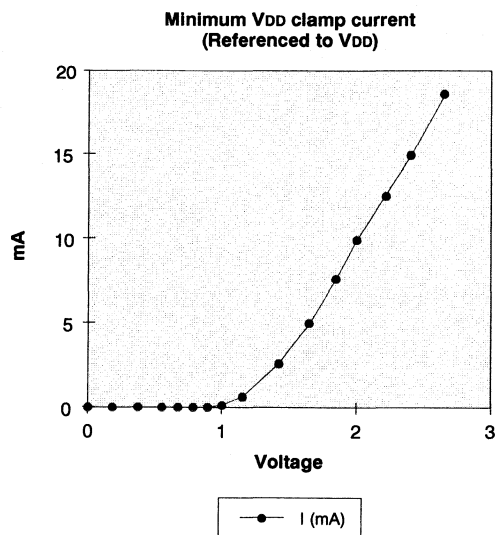
66MHz and 100MHz Pull-down



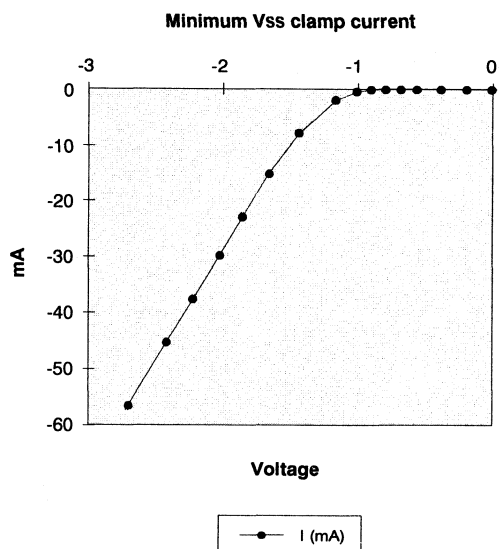
● IOL Min (100MHz)
 △ IOL Min (66MHz)
 ■ IOL Max (100MHz)

V_{DD} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**V_{SS} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ**

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

4M x 8Bit x 4 Banks Synchronous DRAM**FEATURES**

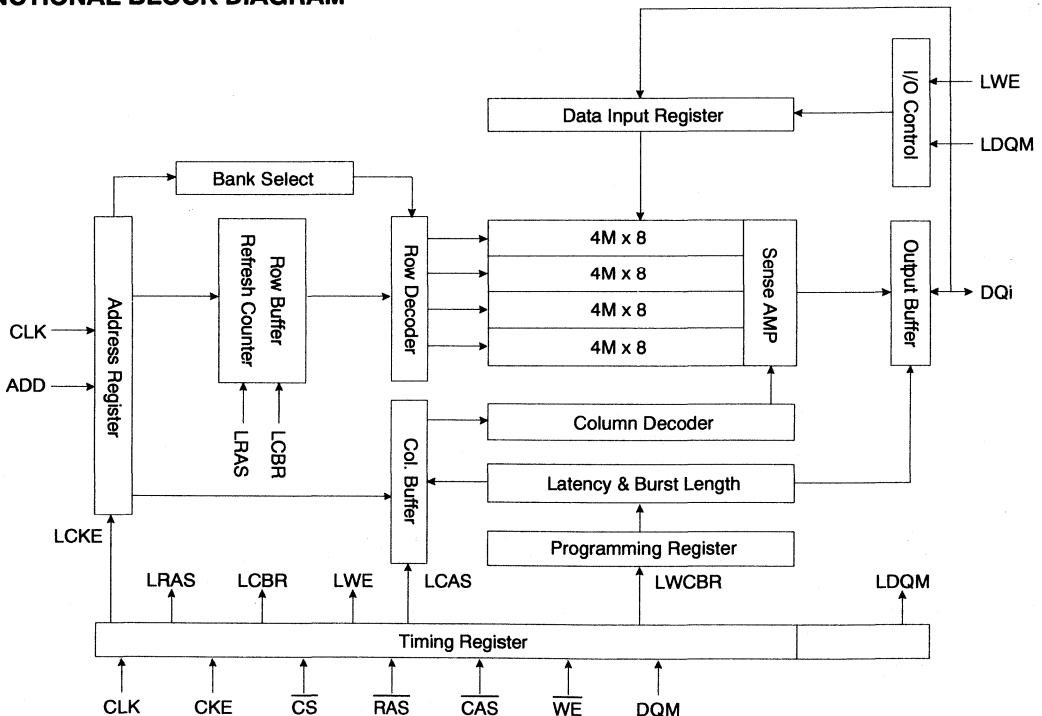
- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

GENERAL DESCRIPTION

The K4S280832B is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 4,194,304 words by 8 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

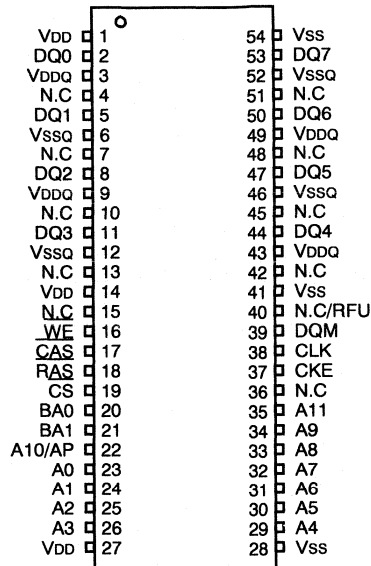
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S280832B-TC/L75	133MHz(CL=3)	LVTTTL	54 TSOP(II)
K4S280832B-TC/L80	125MHz(CL=3)		
K4S280832B-TC/L1H	100MHz(CL=2)		
K4S280832B-TC/L1L	100MHz(CL=3)		
K4S280832B-TC/L10	66MHz(CL=2 & 3)		

FUNCTIONAL BLOCK DIAGRAM

* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ 7	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDD+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ,
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	CCLK	2.5	4.0	pF	1
RAS, CAS, WE, CS, CKE, DQM	CIN	2.5	5.0	pF	2
Address	CADD	2.5	5.0	pF	2
DQ0 ~ DQ7	COUT	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF
 2. -75 only specify a maximum value of 3.8pF
 3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version					Unit	Note
			-75	-80	-1H	-1L	-10		
Operating current (One bank active)	ICC1	Burst length = 1 t _{RC} ≥ t _{RC} (min) I _O = 0 mA	120	120	110	110	110	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ V _{IL} (max), t _{CC} = 10ns	1					mA	
	ICC2PS	CKE & CLK ≤ V _{IL} (max), t _{CC} = ∞	1						
Precharge standby current in non power-down mode	ICC2N	CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(min)$, t _{CC} = 10ns Input signals are changed one time during 20ns	20					mA	
	ICC2NS	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), t _{CC} = ∞ Input signals are stable	7						
Active standby current in power-down mode	ICC3P	CKE ≤ V _{IL} (max), t _{CC} = 10ns	5					mA	
	ICC3PS	CKE & CLK ≤ V _{IL} (max), t _{CC} = ∞	5						
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(min)$, t _{CC} = 10ns Input signals are changed one time during 20ns	30					mA	
	ICC3NS	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), t _{CC} = ∞ Input signals are stable	20					mA	
Operating current (Burst mode)	ICC4	I _O = 0 mA Page burst 4Banks Activated t _{CCD} = 2CLKs	150	145	125	125	125	mA	1
Refresh current	ICC5	t _{RC} ≥ t _{RC} (min)	220	220	210	210	210	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	C	1.5				mA	3
			L	800				uA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

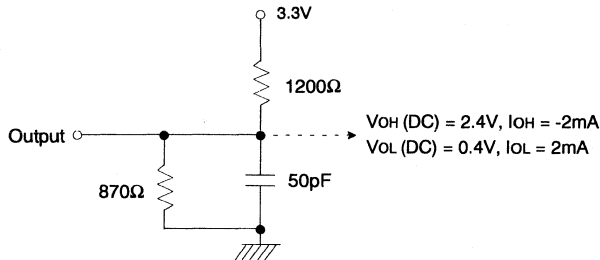
3. K4S280832B-TC**

4. K4S280832B-TL**

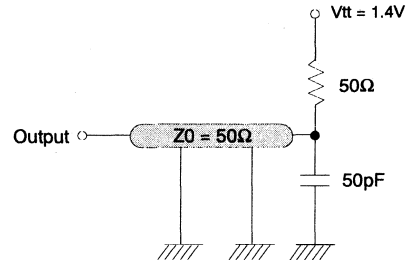
5. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version					Unit	Note
			- 75	- 80	- 1H	- 1L	-10		
Row active to row active delay		tRRD(min)	15	16	20	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	20	20	24	ns	1
Row precharge time		tRP(min)	20	20	20	20	24	ns	1
Row active time		tRAS(min)	45	48	50	50	50	ns	1
		tRAS(max)	100					us	
Row cycle time		tRC(min)	65	68	70	70	80	ns	1
Last data in to row precharge		tRDL(min)	2					CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns					-	5
Last data in to new col. address delay		tCDL(min)	1					CLK	2
Last data in to burst stop		tBDL(min)	1					CLK	2
Col. address to col. address delay		tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3		2					ea	4
	CAS latency=2		-		1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L/10, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported.
SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 75		- 80		- 1H		- 1L		- 10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	7.5	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12		13			
CLK to valid output delay	CAS latency=3	tsac		5.4		6		6		6		7	ns	1,2
	CAS latency=2			-		-		6		7		7		
Output data hold time	CAS latency=3	toH	2.7		3		3		3		3		ns	2
	CAS latency=2		-		-		3		3		3			
CLK high pulse width		tCH	2.5		3		3		3		3.5		ns	3
CLK low pulse width		tCL	2.5		3		3		3		3.5		ns	3
Input setup time		tSS	1.5		2		2		2		2.5		ns	3
Input hold time		tSH	0.8		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6		7	ns	
	CAS latency=2			-		-		6		7		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1$ ns.
If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

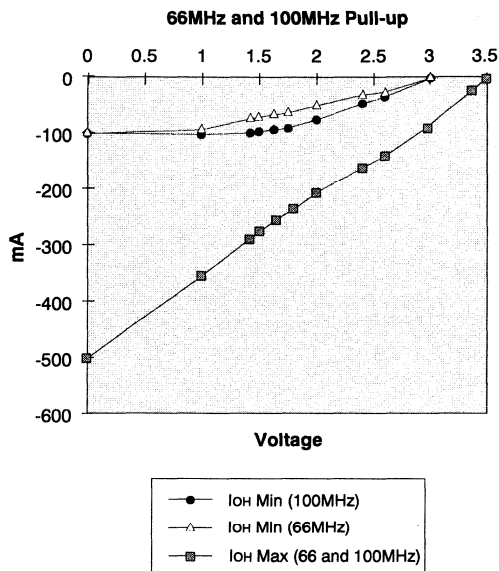
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :**
- Rise time specification based on 0pF + 50 Ω to Vss, use these values to design to.
 - Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
 - Measured into 50pF only, use these values to characterize to.
 - All measurements done with respect to Vss.

IBIS SPECIFICATION

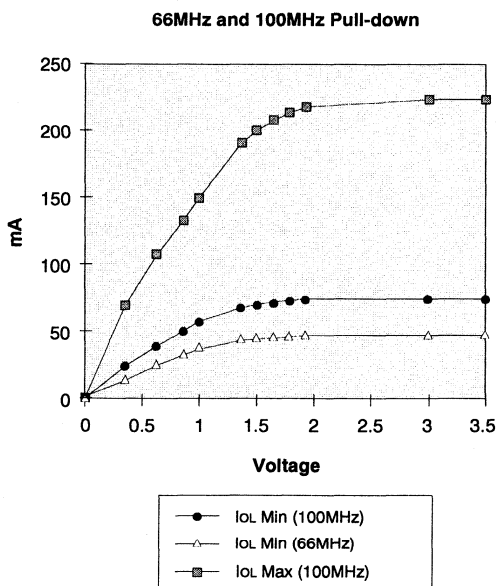
IOH Characteristics (Pull-up)

Voltage (V)	100MHz Min I (mA)	100MHz Max I (mA)	66MHz Min I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



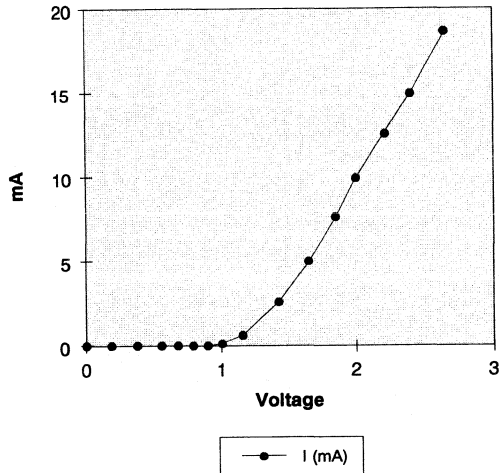
IOL Characteristics (Pull-down)

Voltage (V)	100MHz Min I (mA)	100MHz Max I (mA)	66MHz Min I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

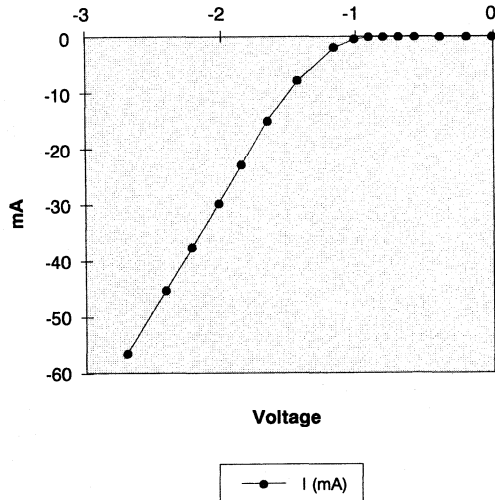


VDD Clamp @ CLK, CKE, CS, DQM & DQ

VDD (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**Minimum VDD clamp current
(Referenced to VDD)****VSS Clamp @ CLK, CKE, CS, DQM & DQ**

VSS (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

Minimum VSS clamp current

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	X	X			3	
												H	X
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

FEATURES

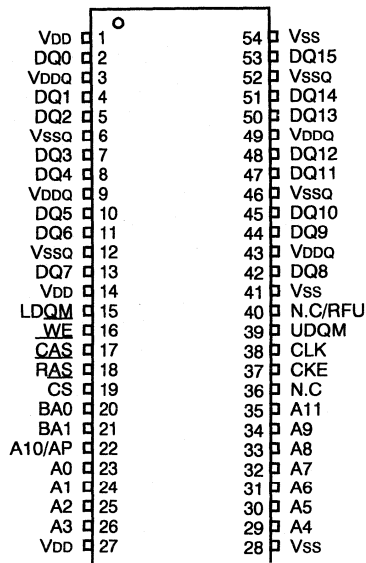
- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

The K4S281632B is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 2,097,152 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Part No.	Max Freq.	Interface	Package
K4S281632B-TC/L75	133MHz(CL=3)	LVTTTL	54 TSOP(II)
K4S281632B-TC/L80	125MHz(CL=3)		
K4S281632B-TC/L1H	100MHz(CL=2)		
K4S281632B-TC/L1L	100MHz(CL=3)		
K4S281632B-TC/L10	66MHz(CL=2 &3)		

* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
L(U)DQM	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ 15	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VssQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ},
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C _{CLK}	2.5	4.0	pF	1
RAS, CAS, WE, CS, CKE, DQM	C _{IN}	2.5	5.0	pF	2
Address	C _{ADD}	2.5	5.0	pF	2
DQ0 ~ DQ15	C _{OUT}	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF
2. -75 only specify a maximum value of 3.8pF
3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version					Unit	Note	
			-75	-80	-1H	-1L	-10			
Operating current (One bank active)	ICC1	Burst length = 1 tRC ≥ tRC(min) IO = 0 mA	150	150	140	140	140	mA	1	
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	1					mA		
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	1							
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS̄ ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	20					mA		
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	7							
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	5					mA		
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	5							
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS̄ ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	30					mA		
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	20					mA		
Operating current (Burst mode)	ICC4	IO = 0 mA Page burst 4Banks Activated tccd = 2CLKs	180	170	145	145	145	mA	1	
Refresh current	ICC5	tRC ≥ tRC(min)	220	220	210	210	210	mA	2	
Self refresh current	ICC6	CKE ≤ 0.2V	C	1.5					mA	3
			L	800					uA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

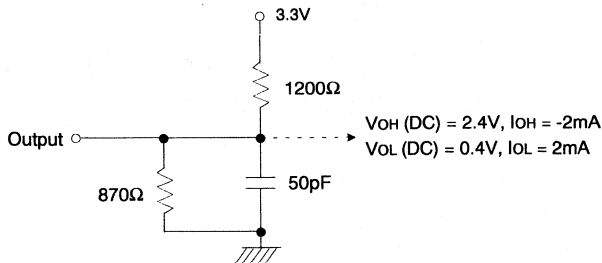
3. K4S281632B-TC**

4. K4S281632B-TL**

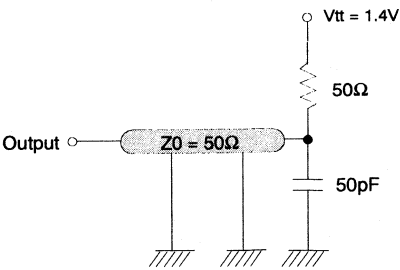
5. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version					Unit	Note
		- 75	- 80	- 1H	- 1L	-10		
Row active to row active delay	tRRD(min)	15	16	20	20	20	ns	1
RAS to CAS delay	tRCD(min)	20	20	20	20	24	ns	1
Row precharge time	tRP(min)	20	20	20	20	24	ns	1
Row active time	tRAS(min)	45	48	50	50	50	ns	1
	tRAS(max)	100					us	
Row cycle time	tRC(min)	65	68	70	70	80	ns	1
Last data in to row precharge	tRDL(min)	2					CLK	2,5
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns					-	5
Last data in to new col. address delay	tCDL(min)	1					CLK	2
Last data in to burst stop	tBDL(min)	1					CLK	2
Col. address to col. address delay	tCCD(min)	1					CLK	3
Number of valid output data	CAS latency=3	2					ea	4
	CAS latency=2	-		1				

- Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L/10, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
- SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 75		- 80		- 1H		- 1L		- 10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		5.4		6		6		6		7	ns	1,2
	CAS latency=2			-		-		6		7		7		
Output data hold time	CAS latency=3	tOH	2.7		3		3		3		3		ns	2
	CAS latency=2		-		-		3		3		3			
CLK high pulse width		tCH	2.5		3		3		3		3.5		ns	3
CLK low pulse width		tCL	2.5		3		3		3		3.5		ns	3
Input setup time		tSS	1.5		2		2		2		2.5		ns	3
Input hold time		tSH	0.8		1		1		1		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6		7	ns	
	CAS latency=2			-		-		6		7		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

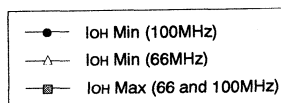
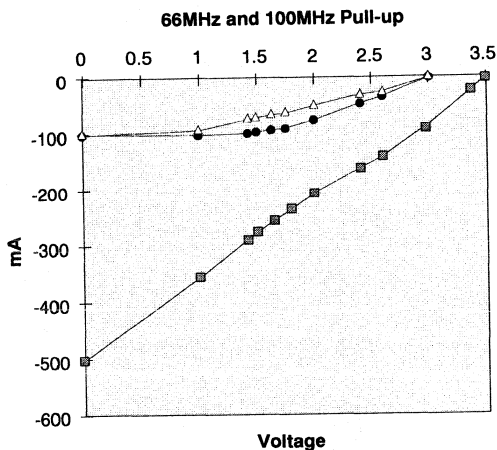
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :**
- Rise time specification based on $0pF + 50 \Omega$ to V_{SS} , use these values to design to.
 - Fall time specification based on $0pF + 50 \Omega$ to V_{DD} , use these values to design to.
 - Measured into $50pF$ only, use these values to characterize to.
 - All measurements done with respect to V_{SS} .

IBIS SPECIFICATION

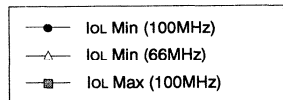
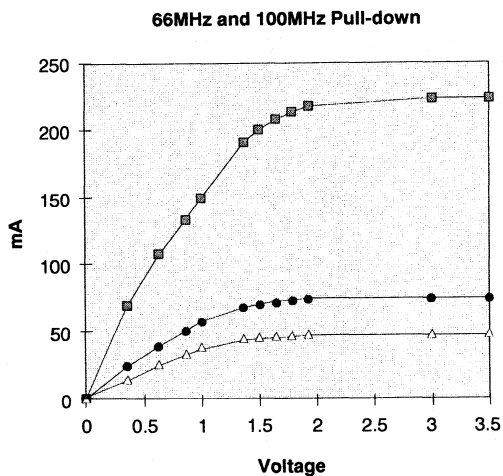
IoH Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



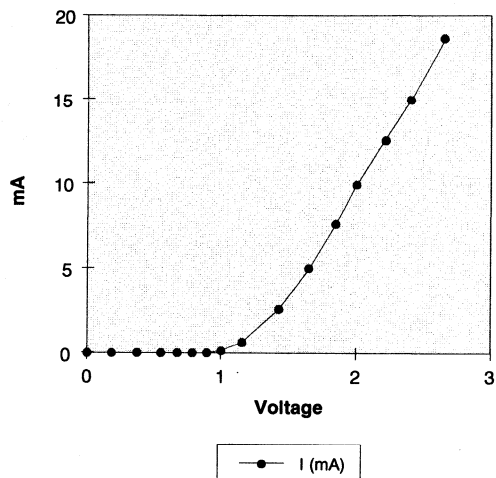
IoL Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

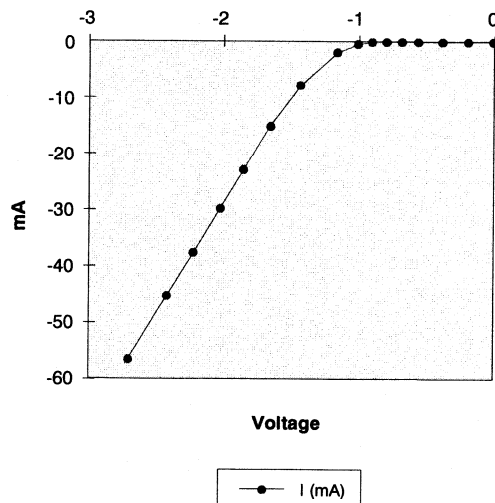


V_{DD} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**Minimum V_{DD} clamp current
(Referenced to V_{DD})****V_{SS} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ**

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

Minimum V_{SS} clamp current

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set		H	X	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self fefresh	L		3									
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

NOTES

Component Specification

2

256M bit A-die



9:10 0/2241 011 01 01

4031 DBAMs

16M x 4Bit x 4 Banks Synchronous DRAM**FEATURES**

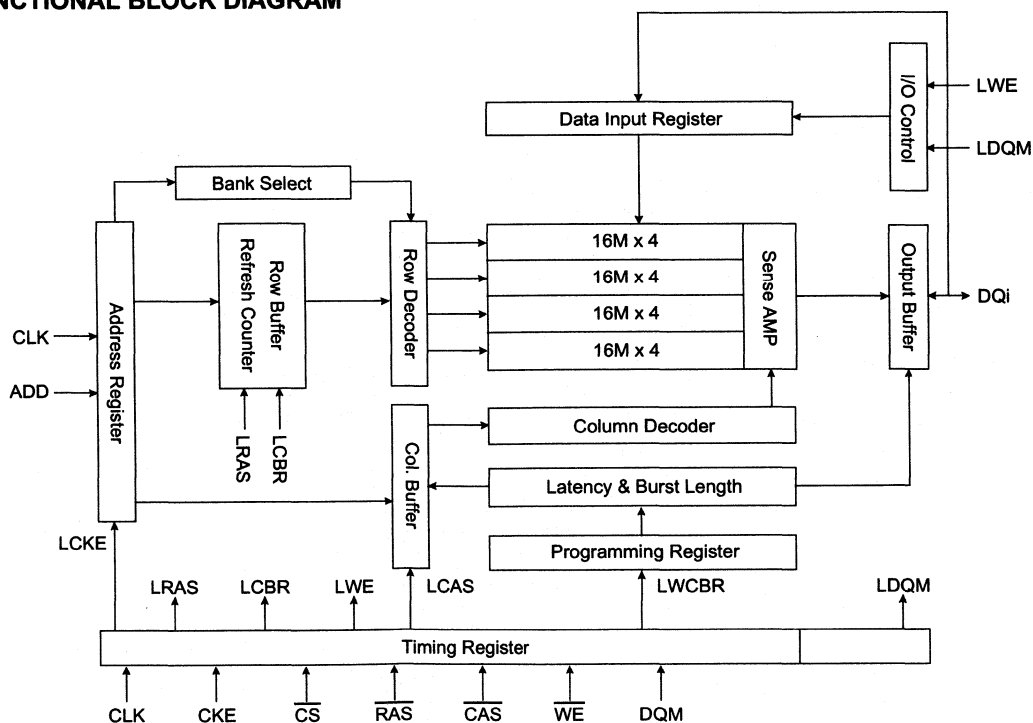
- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (8K cycle)

GENERAL DESCRIPTION

The K4S560432A is 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 16,785,216 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

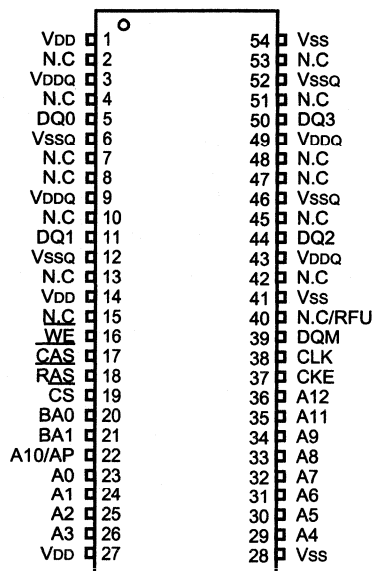
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S560432A-TC/L75	133MHz(CL=3)	LVTTTL	54pin TSOP(II)
K4S560432A-TC/L80	125MHz(CL=3)		
K4S560432A-TC/L1H	100MHz(CL=2)		
K4S560432A-TC/L1L	100MHz(CL=3)		

FUNCTIONAL BLOCK DIAGRAM

* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ 3	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C))

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDD+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	CCLK	2.5	4.0	pF	1
RAS, CAS, WE, CS, CKE, DQM	CIN	2.5	5.0	pF	2
Address	CADD	2.5	5.0	pF	2
DQ0 ~ DQ15	COUT	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF
 2. -75 only specify a maximum value of 3.8pF
 3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version				Unit	Note
			-75	-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	120	120	110	110	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	2				mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	2					
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	16				mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	14					
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	6				mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	6					
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	30				mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	25				mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4banks Activated tccd = 2CLKs	140	140	115	115	mA	1
Refresh current	Icc5	trc ≥ trc(min)	210	210	200	200	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	C	5			mA	3
			L	2			mA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

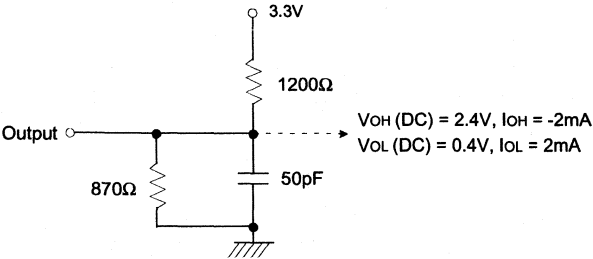
3. K4S560432A-TC**

4. K4S560432A-TL**

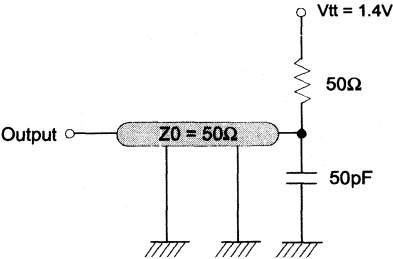
5. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			-75	-80	-1H	-1L		
Row active to row active delay		tRRD(min)	15	16	20	20	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay		tRCD(min)	20	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	20	ns	1
Row active time		tRAS(min)	45	48	50	50	ns	1
		tRAS(max)	100				us	
Row cycle time		tRC(min)	65	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2				CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns				-	5
Last data in to new col. address delay		tCDL(min)	1				CLK	2
Last data in to burst stop		tBDL(min)	1				CLK	2
Col. address to col. address delay		tCCD(min)	1				CLK	3
Number of valid output data	CAS latency=3		2				ea	4
	CAS latency=2		-		1			

- Notes :**
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.
 - 5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	7.5	1000	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12			
CLK to valid output delay	CAS latency=3	tsac		5.4		6		6		6	ns	1, 2
	CAS latency=2			-		6		6		7		
Output data hold time	CAS latency=3	toH	2.7		3		3		3		ns	2
	CAS latency=2		-		-		3		3			
CLK high pulse width		tCH	2.5		3		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		3		ns	3
Input setup time		tSS	1.5		2		2		2		ns	3
Input hold time		tSH	0.8		1		1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6	ns	
	CAS latency=2			-		-		6		7		

- Notes :** 1. Parameters depend on programmed CAS latency.
 2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 3. Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
 If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
 i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

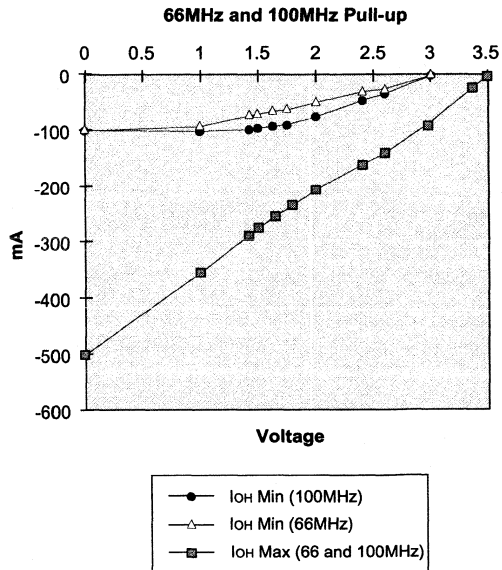
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :** 1. Rise time specification based on 0pF + 50 Ω to Vss, use these values to design to.
 2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
 3. Measured into 50pF only, use these values to characterize to.
 4. All measurements done with respect to Vss.

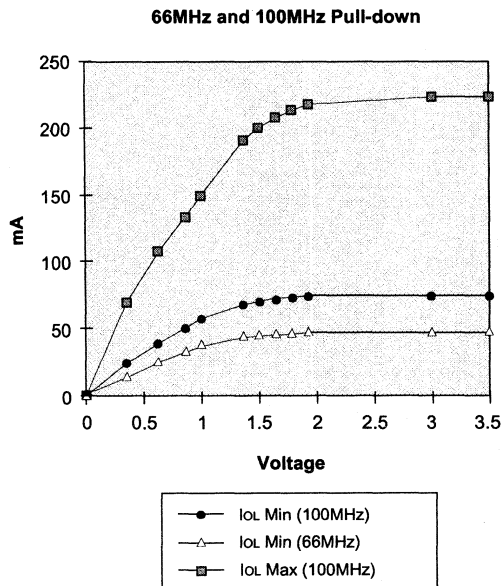
IBIS SPECIFICATION

I_{OH} Characteristics (Pull-up)

Voltage (V)	100MHz Min I (mA)	100MHz Max I (mA)	66MHz Min I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0

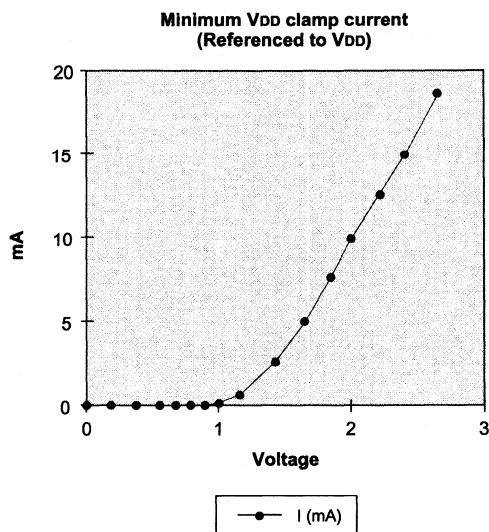
I_{OL} Characteristics (Pull-down)

Voltage (V)	100MHz Min I (mA)	100MHz Max I (mA)	66MHz Min I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

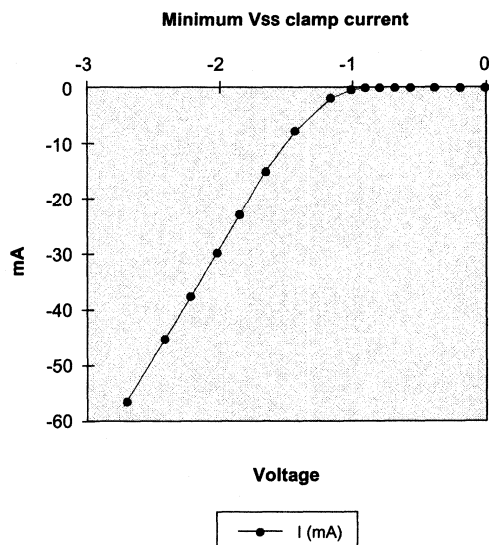


V_{DD} Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**V_{SS} Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ**

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A12, A9 ~ A0	Note
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3
	Self refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X	X	X	3
					H	X	X	X				3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks								X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X		
					L	V	V	V				
		Exit	L	H	X	X	X	X	X			
Precharge power down mode		Entry	H	L	H	X	X	X	X	X		
					L	H	H	H				
		Exit	L	H	H	X	X	X	X			
					L	V	V	V				
DQM		H	X					V	X		7	
No operation command		H	X	H	X	X	X	X	X			
				L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

8M x 8Bit x 4 Banks Synchronous DRAM**FEATURES**

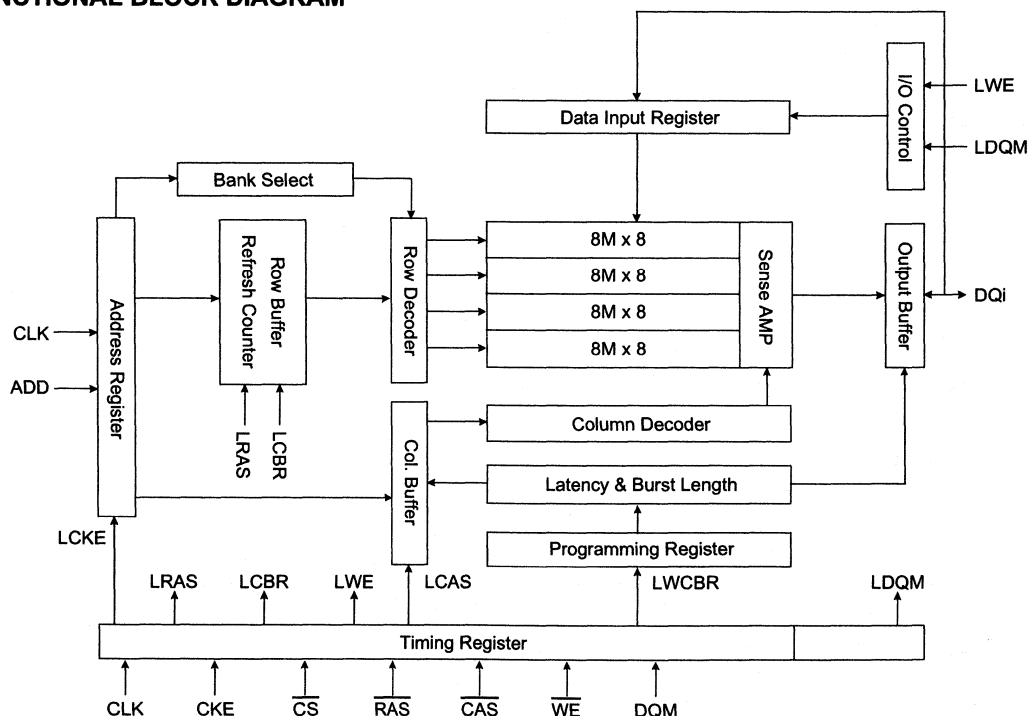
- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (8K Cycle)

GENERAL DESCRIPTION

The K4S560832A is 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 8,392,608 words by 8 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

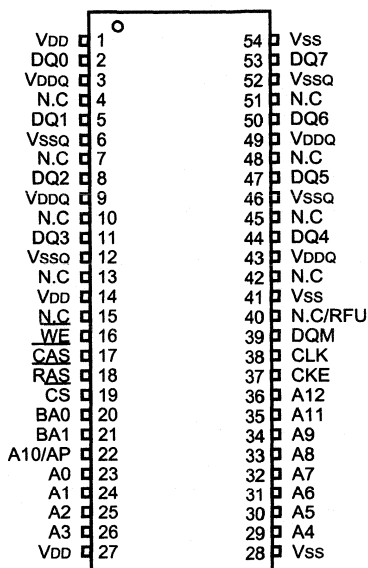
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S560832A-TC/L75	133MHz(CL=3)	LVTTTL	54pin TSOP(II)
K4S560832A-TC/L80	125MHz(CL=3)		
K4S560832A-TC/L1H	100MHz(CL=2)		
K4S560832A-TC/L1L	100MHz(CL=3)		

FUNCTIONAL BLOCK DIAGRAM

* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~7	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _d	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDD+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	CCLK	2.5	4.0	pF	1
RAS, CAS, WE, CS, CKE, DQM	CIN	2.5	5.0	pF	2
Address	CADD	2.5	5.0	pF	2
DQ0 ~ DQ15	COUT	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF
 2. -75 only specify a maximum value of 3.8pF
 3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version				Unit	Note
			-75	-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	120	120	110	110	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	2				mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	2					
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 10ns Input signals are changed one time during 20ns	16				mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	14					
Active Standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	6				mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	6					
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 10ns Input signals are changed one time during 20ns	30				mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	25				mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4banks activated. tccd = 2CLKs	140	140	115	115	mA	1
Refresh current	Icc5	trc ≥ trc(min)	210	210	200	200	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	C	5			mA	3
			L	2			mA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

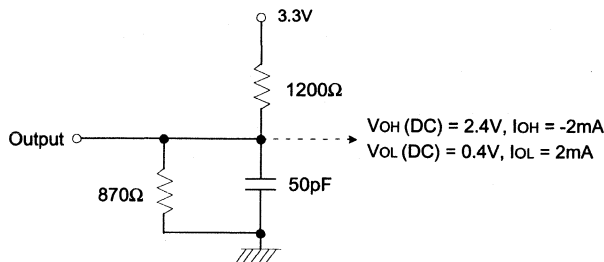
3. K4S560832A-TC**

4. K4S560832A-TL**

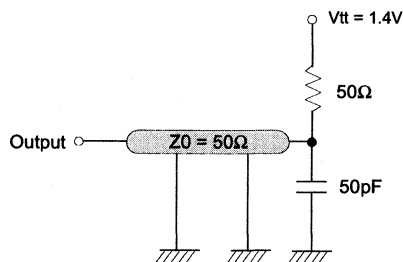
5. Unless otherwise noticed, input swing level is CMOS(VIH/UIL=VDDQ/VSSQ).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			-75	-80	-1H	-1L		
Row active to row active delay		trrd(min)	15	16	20	20	ns	1
RAS to CAS delay		trcd(min)	20	20	20	20	ns	1
Row precharge time		trp(min)	20	20	20	20	ns	1
Row active time		tras(min)	45	48	50	50	ns	1
		tras(max)	100				us	
Row cycle time		trc(min)	65	68	70	70	ns	1
Last data in to row precharge		trdl(min)	2				CLK	2,5
Last data in to Active delay		tdal(min)	2 CLK + 20 ns				-	5
Last data in to new col. address delay		tcdl(min)	1				CLK	2
Last data in to burst stop		tbdl(min)	1				CLK	2
Col. address to col. address delay		tccd(min)	1				CLK	3
Number of valid output data	CAS latency=3		2				ea	4
	CAS latency=2		-		1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -80/1H/1L, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .
SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12			
CLK to valid output delay	CAS latency=3	tSAC		5.4		6		6		6	ns	1,2
	CAS latency=2			-		-		6		7		
Output data hold time	CAS latency=3	tOH	2.7		3		3		3		ns	2
	CAS latency=2		-		-		3		3			
CLK high pulse width		tCH	2.5		3		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		3		ns	3
Input setup time		tSS	1.5		2		2		2		ns	3
Input hold time		tSH	0.8		1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6	ns	
	CAS latency=2			-		-		6		7		

- Notes :** 1. Parameters depend on programmed CAS latency.
 2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.
 3. Assumed input rise and fall time $(tr \ \& \ tf) = 1$ ns.
 If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
 i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

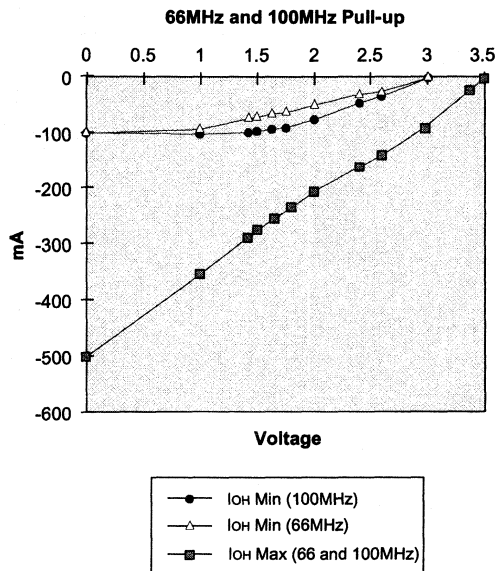
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :** 1. Rise time specification based on 0pF + 50 Ohms to Vss, use these values to design to.
 2. Fall time specification based on 0pF + 50 Ohms to VDD, use these values to design to.
 3. Measured into 50pF only, use these values to characterize to.
 4. All measurements done with respect to Vss.

IBIS SPECIFICATION

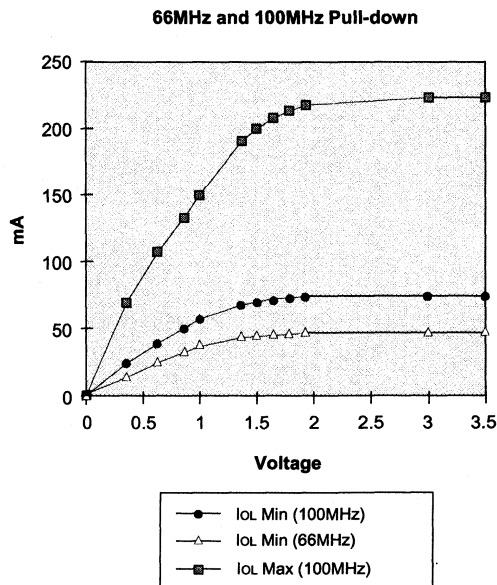
IOH Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



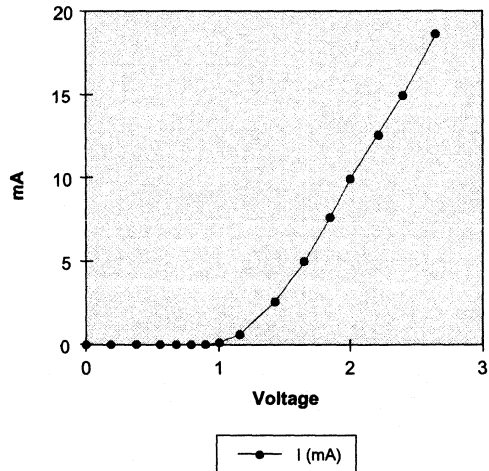
IOL Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3	80.3	219.6	54.2
3.45	81.4	222.6	54.9

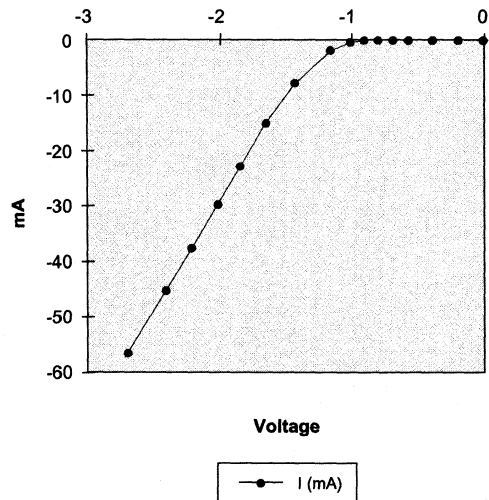


V_{DD} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**Minimum V_{DD} clamp current
(Referenced to V_{DD})****V_{SS} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ**

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

Minimum V_{SS} clamp current

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11,A12, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at trp after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

4M x 16Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (8K Cycle)

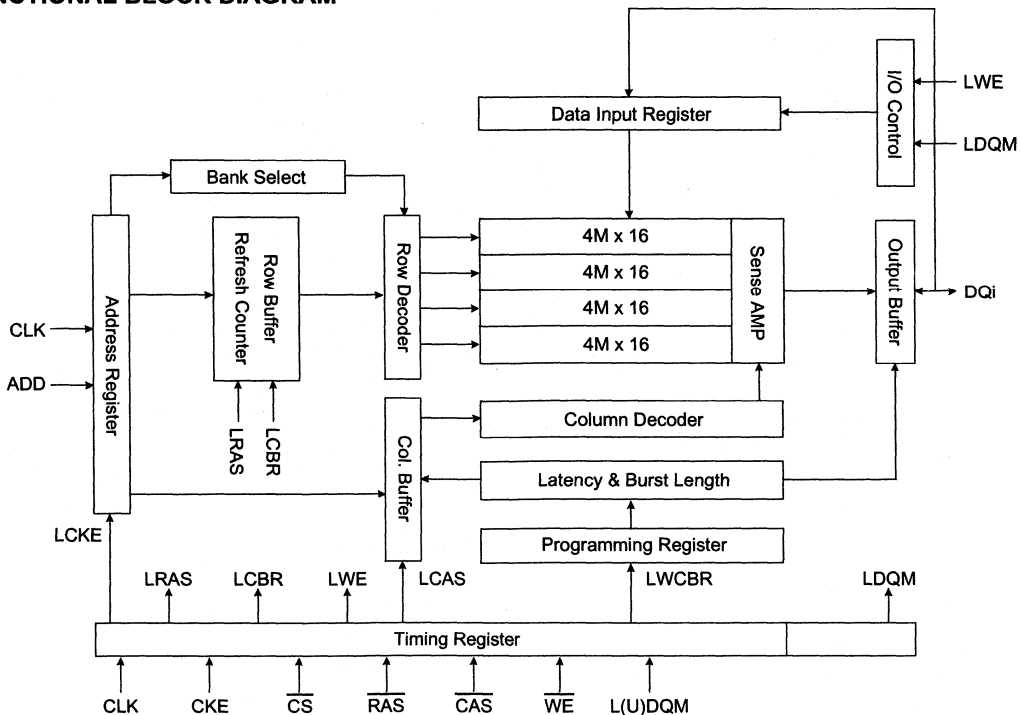
GENERAL DESCRIPTION

The K4S561632A is 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 4,196,304 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

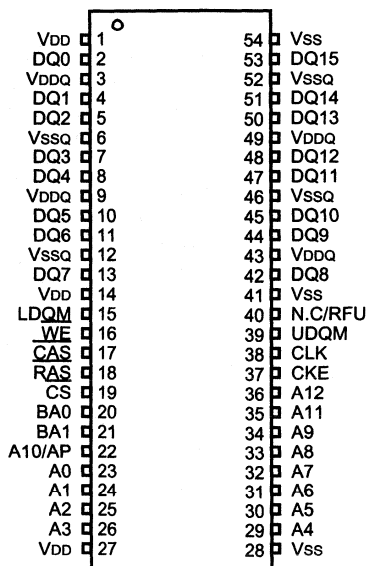
Part No.	Max Freq.	Interface	Package
K4S561632A-TC/L75	133MHz(CL=3)	LVTTL	54pin TSOP(II)
K4S561632A-TC/L80	125MHz(CL=3)		
K4S561632A-TC/L1H	100MHz(CL=2)		
K4S561632A-TC/L1L	100MHz(CL=3)		

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA8
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
L(U)DQM	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ 15	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C./RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDD+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ VDDQ.

Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C _{CLK}	2.5	4.0	pF	1
RAS, CAS, WE, CS, CKE, DQM	C _{IN}	2.5	5.0	pF	2
Address	C _{ADD}	2.5	5.0	pF	2
DQ0 ~ DQ15	C _{OUT}	4.0	6.5	pF	3

Notes : 1. -75 only specify a maximum value of 3.5pF

2. -75 only specify a maximum value of 3.8pF

3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version				Unit	Note
			-75	-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	150	150	140	140	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	2				mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	2					
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	16				mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	14					
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	6				mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	6					
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	35				mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	30				mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4banks Activated. tccd = 2CLKs	180	180	145	145	mA	1
Refresh current	Icc5	trc ≥ trc(min)	210	210	200	200	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	C	5			mA	3
			L	2			mA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

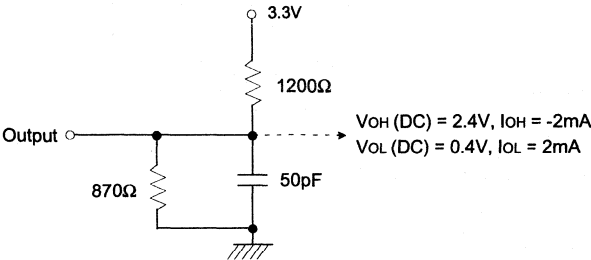
3. K4S561632A-TC**

4. K4S561632A-TL**

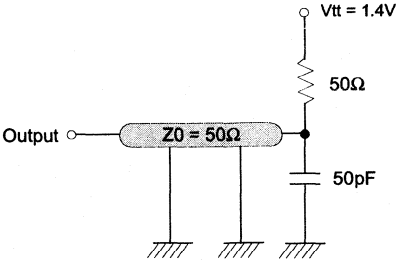
5. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			-75	-80	-1H	-1L		
Row active to row active delay		tRRD(min)	15	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	20	ns	1
Row active time		tRAS(min)	45	48	50	50	ns	1
		tRAS(max)	100				us	
Row cycle time		tRC(min)	65	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2				CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns				-	5
Last data in to new col. address delay		tCDL(min)	1				CLK	2
Last data in to burst stop		tBDL(min)	1				CLK	2
Col. address to col. address delay		tCCD(min)	1				CLK	3
Number of valid output data	CAS latency=3		2				ea	4
	CAS latency=2		-		1			

- Notes :**
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.
 - 5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-75		-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12			
CLK to valid output delay	CAS latency=3	tsAC		5.4		6		6		6	ns	1,2
	CAS latency=2			-		-		6		7		
Output data hold time	CAS latency=3	tOH	2.7		3		3		3		ns	2
	CAS latency=2		-		-		3		3			
CLK high pulse width		tCH	2.5		3		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		3		ns	3
Input setup time		tSS	1.5		2		2		2		ns	3
Input hold time		tSH	0.8		1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6		6	ns	
	CAS latency=2			-		-		6		7		

- Notes :** 1. Parameters depend on programmed CAS latency.
 2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
 3. Assumed input rise and fall time (tr & tf) = 1ns.
 If tr & tf is longer than 1ns, transient time compensation should be considered,
 i.e., [(tr + tf)/2-1]ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

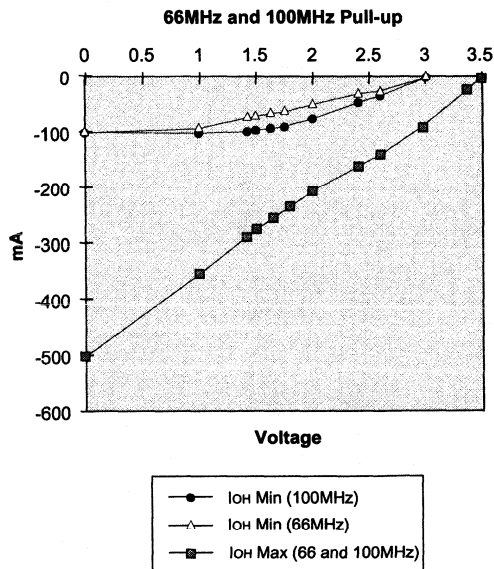
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :** 1. Rise time specification based on 0pF + 50 Ω to Vss, use these values to design to.
 2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
 3. Measured into 50pF only, use these values to characterize to.
 4. All measurements done with respect to Vss.

IBIS SPECIFICATION

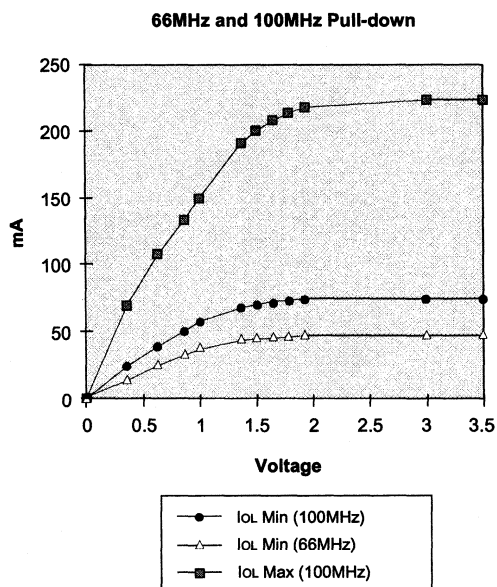
IOH Characteristics (Pull-up)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



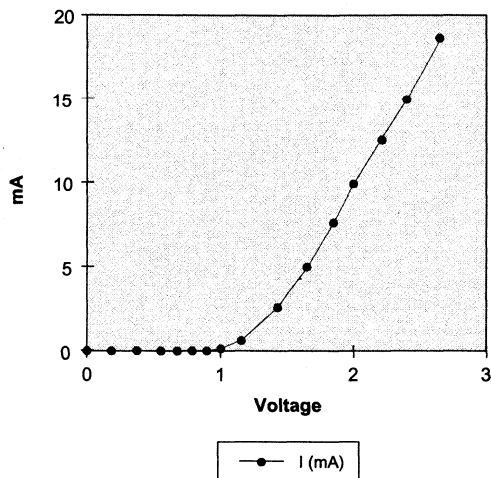
IOL Characteristics (Pull-down)

Voltage	100MHz Min	100MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

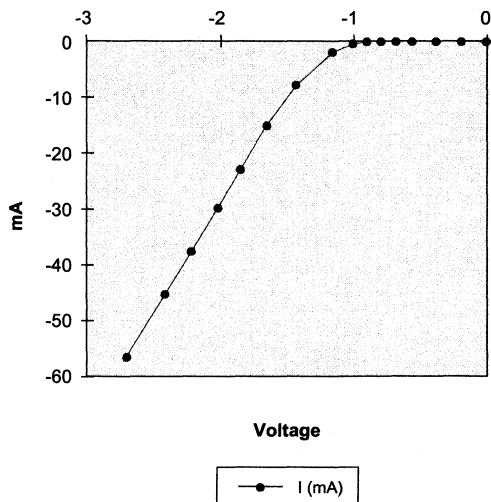


V_{DD} Clamp @ CLK, CKE, CS, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**Minimum V_{DD} clamp current
(Referenced to V_{DD})****V_{SS} Clamp @ CLK, CKE, CS, DQM & DQ**

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

Minimum V_{SS} clamp current

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11,A12, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	L		3									
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at trp after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Component Specification

2

Device Operation & Timing Diagram

56MHz and 100MHz PLL Lockup

(Back view)

0.001-0.003
2.70-2.9
0.001-0.003
All on 0.25µm Dielectric
100-ohm DPAK

A. MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA0 ~ BA1	Ar ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT = 0	BT = 1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length : x4 (1024), x8 (512), x16 (256)

B. POWER UP SEQUENCE

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
 2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
 3. Issue precharge commands for all banks of the devices.
 4. Issue 2 or more auto-refresh commands.
 5. Issue a mode register set command to initialize the mode register.
- cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

- Note :** 1. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

C. BURST SEQUENCE

1. BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A ₁	A ₀								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

2. BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A ₂	A ₁	A ₀																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

D. DEVICE OPERATIONS

ADDRESSES of 128Mb

BANK ADDRESSES (BA0 ~ BA1)

: In case x 4

This SDRAM is organized as four independent banks of 8,388,608 words x 4 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and pre-charge operations.

: In case x 8

This SDRAM is organized as four independent banks of 4,194,304 words x 8 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and pre-charge operations.

: In case x 16

This SDRAM is organized as four independent banks of 2,097,152 words x 16 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and pre-charge operations.

ADDRESS INPUTS (A0 ~ A11)

: In case x 4

The 23 address bits are required to decode the 8,388,608 word locations are multiplexed into 12 address input pins (A0 ~ A11). The 12 bit row addresses are latched along with $\overline{\text{RAS}}$ and BA0 ~ BA1 during bank activate command. The 11 bit column addresses are latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 ~ BA1 during read or write command.

: In case x 8

The 22 address bits are required to decode the 4,194,304 word locations are multiplexed into 12 address input pins (A0 ~ A11). The 12 bit row addresses are latched along with $\overline{\text{RAS}}$ and BA0 ~ BA1 during bank activate command. The 10 bit column addresses are latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 ~ BA1 during read or write command.

: In case x 16

The 21 address bits are required to decode the 2,097,152 word locations are multiplexed into 12 address input pins (A0 ~ A11). The 12 bit row addresses are latched along with $\overline{\text{RAS}}$ and BA0 ~ BA1 during bank activate command. The 9 bit column addresses are latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 ~ BA1 during read or write command.

ADDRESSES of 256Mb

BANK ADDRESSES (BA0 ~ BA1)

: In case x 4

This SDRAM is organized as four independent banks of 16,777,216 words x 4 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and pre-charge operations.

: In case x 8

This SDRAM is organized as four independent banks of 8,388,608 words x 8 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and pre-charge operations.

: In case x 16

This SDRAM is organized as four independent banks of 4,194,304 words x 16 bits memory arrays. The BA0 ~ BA1 inputs are latched at the time of assertion of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the bank to be used for the operation. The bank addresses BA0 ~ BA1 are latched at bank active, read, write, mode register set and pre-charge operations.

ADDRESS INPUTS (A0 ~ A12)

: In case x 4

The 24 address bits are required to decode the 16,777,216 word locations are multiplexed into 13 address input pins (A0 ~ A12). The 13 bit row addresses are latched along with $\overline{\text{RAS}}$ and BA0 ~ BA1 during bank activate command. The 11 bit column addresses are latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 ~ BA1 during read or write command.

: In case x 8

The 23 address bits are required to decode the 8,388,608 word locations are multiplexed into 13 address input pins (A0 ~ A12). The 13 bit row addresses are latched along with $\overline{\text{RAS}}$ and BA0 ~ BA1 during bank activate command. The 10 bit column addresses are latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 ~ BA1 during read or write command.

: In case x 16

The 22 address bits are required to decode the 4,194,304 word locations are multiplexed into 13 address input pins (A0 ~ A12). The 13 bit row addresses are latched along with $\overline{\text{RAS}}$ and BA0 ~ BA1 during bank activate command. The 9 bit column addresses are latched along with $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and BA0 ~ BA1 during read or write command.

D. DEVICE OPERATIONS (continued)

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH} . During operation with CKE high all inputs are assumed to be in a valid state (low or high) for the duration of set-up and hold time around positive edge of the clock in order to function well Q perform and lcc specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time are the same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + tss" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interruptions of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. Please refer to DQM timing diagram also.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins $A_0 \sim A_n$ and $BA_0 \sim BA_1$ in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on the fields of functions. The burst length field uses $A_0 \sim A_2$, burst type uses A_3 , CAS latency (read latency from column address) use $A_4 \sim A_6$, vendor specific options or test mode use $A_7 \sim A_8$, $A_{10}/AP \sim A_n$ and $BA_0 \sim BA_1$. The write burst length is programmed using A_9 . $A_7 \sim A_8$, $A_{10}/AP \sim A_n$ and $BA_0 \sim BA_1$ must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

D. DEVICE OPERATIONS (continued)

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of $\text{trCD}(\text{min})$ from the time of bank activation. trCD is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing $\text{trCD}(\text{min})$ with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high, requiring some time for power supplies to recover before another bank can be sensed reliably. $\text{trRD}(\text{min})$ specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to trCD specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by $\text{trAS}(\text{min})$. Every SDRAM bank activate command must satisfy $\text{trAS}(\text{min})$ specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by $\text{trAS}(\text{max})$. The number of cycles for both $\text{trAS}(\text{min})$ and $\text{trAS}(\text{max})$ can be calculated similar to trCD specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{\text{CS}}$ and $\overline{\text{CAS}}$ with $\overline{\text{WE}}$ being high on the positive edge of the clock. The bank must be active for at least $\text{trCD}(\text{min})$ before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed.

The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{\text{CS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and precharging the bank trDL after the last data input to be written into the active row. See DQM OPERATION also.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ with high on A10/AP after all banks have satisfied $\text{trAS}(\text{min})$ requirement, performs precharge on all banks. At the end of trP after performing precharge to all the banks, both banks are in idle state.

D. DEVICE OPERATIONS (continued)

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A10/AP with valid BA0 ~ BA1 of the bank to be precharged. The precharge command can be asserted anytime after $t_{RAS}(\min)$ is satisfied from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t_{RP} with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by $t_{RAS}(\max)$. Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to Power down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy $t_{RAS}(\min)$ and "trp" for the programmed burst length and $\overline{CAS}$ latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A10/AP. If burst read or burst write by asserting high on A10/AP, the bank is left active until a new command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

AUTO REFRESH

The storage cells of 64Mb, 128Mb and 256Mb SDRAM need to be refreshed every 64ms to maintain data and 16Mb SDRAM need to be refreshed every 32ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle).

The time required to complete the auto refresh operation is specified by $t_{RC}(\min)$. The minimum number of clock cycles required can be calculated by driving t_{RC} with clock cycle time and then rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. All banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The 16Mb SDRAMs auto refresh cycle can be performed once in 15.6us or a burst of 2048 auto refresh cycles once in 32ms. The 64Mb and 128Mb SDRAMs auto refresh cycle can be performed once in 15.6us or a burst of 4096 auto refresh cycles once in 64ms. The 256Mb SDRAMs auto refresh cycle can be performed once in 7.8us or a burst of 8192 auto refresh cycles once in 64ms.

SELF REFRESH

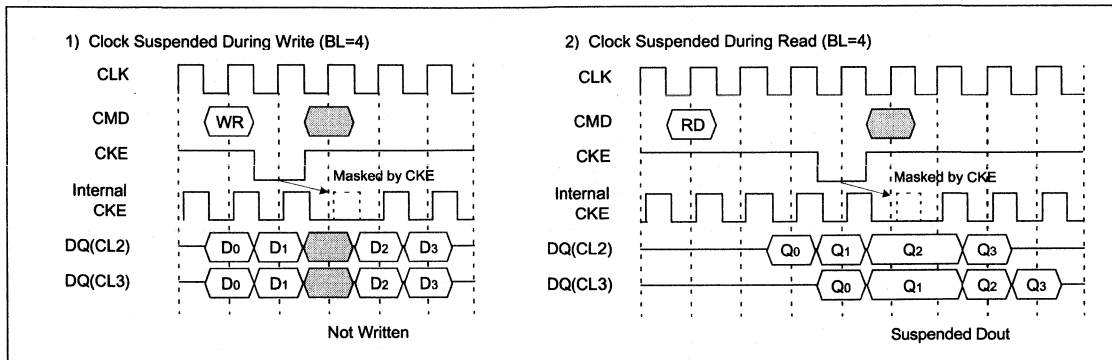
The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing are internally generated to reduce power consumption.

The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including the clock are ignored in order to remain in the self refresh mode.

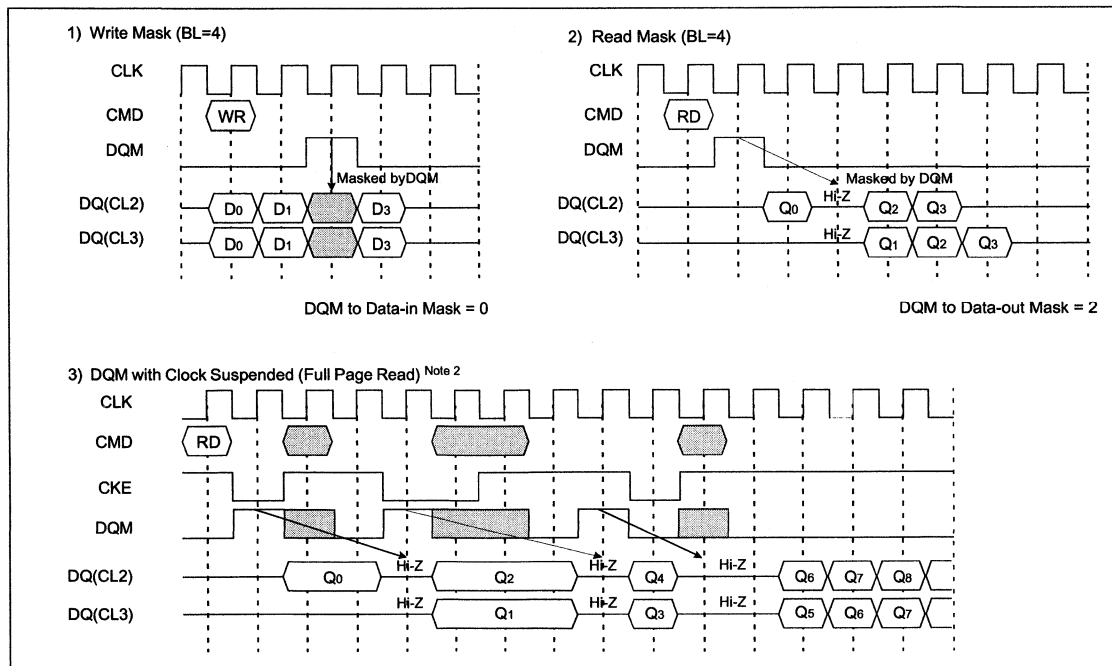
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 8192 auto refresh cycles for 256Mb and burst 4096 auto refresh cycles for 128Mb/64Mb and burst 2048 auto refresh cycles for 16Mb immediately after exiting in self refresh mode.

E. BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend

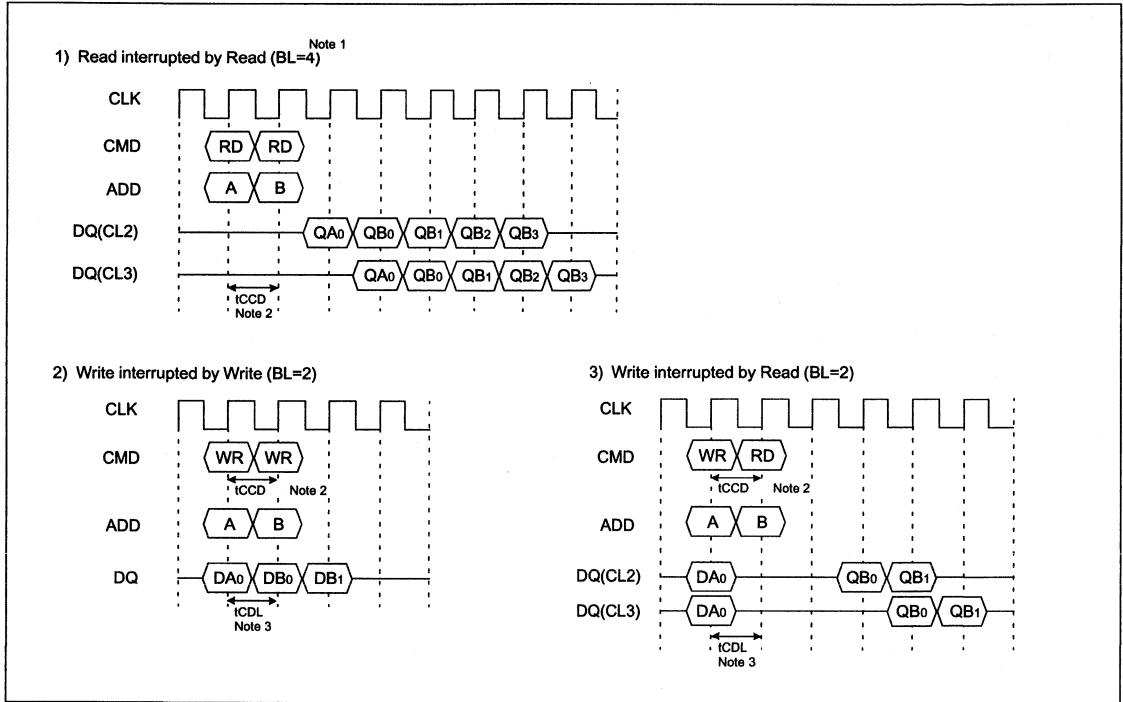


2. DQM Operation



- *Note : 1. CKE to CLK disable/enable = 1CLK.
 2. DQM makes data out Hi-Z after 2CLKs which should be masked by CKE "L"
 3. DQM masks both data-in and data-out.

3. CAS Interrupt (I)



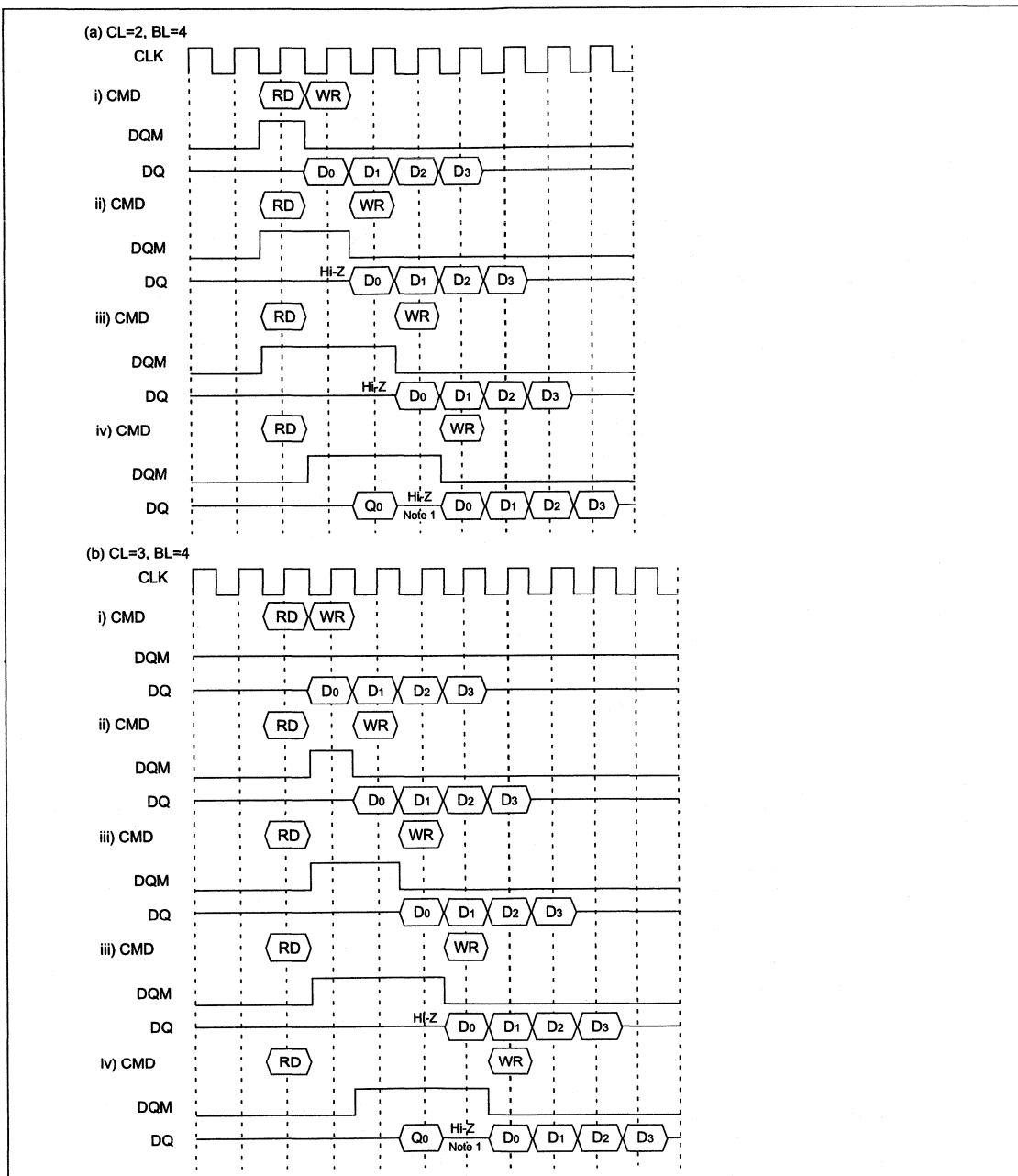
***Note :** 1. By " Interrupt", It is meant to stop burst read/write by external command before the end of burst.

By "CAS Interrupt", to stop burst read/write by CAS access ; read and write.

2. t_{CCD} : CAS to CAS delay. (=1CLK)

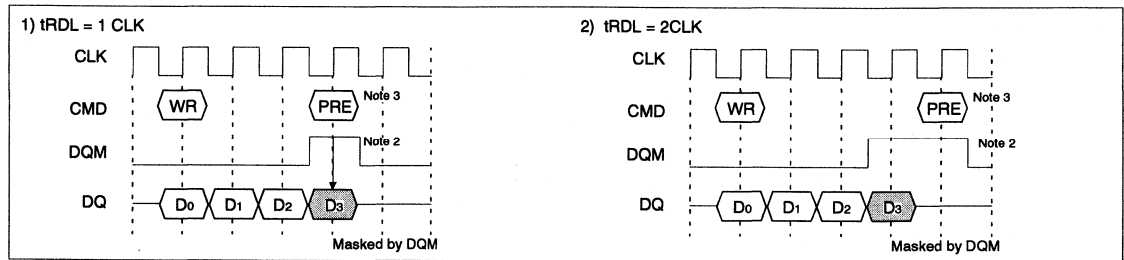
3. t_{CDL} : Last data in to new column address delay. (=1CLK)

4. CAS Interrupt (II) : Read Interrupted by Write & DQM



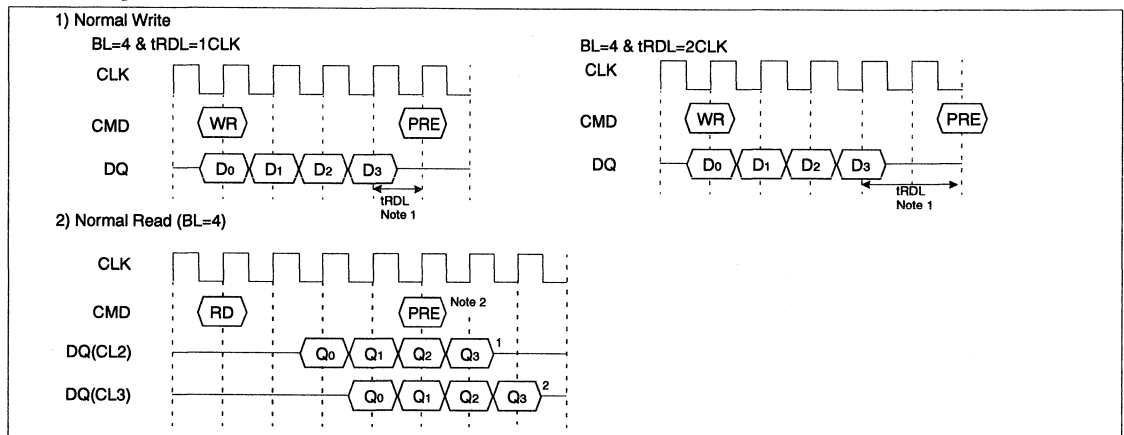
*Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM

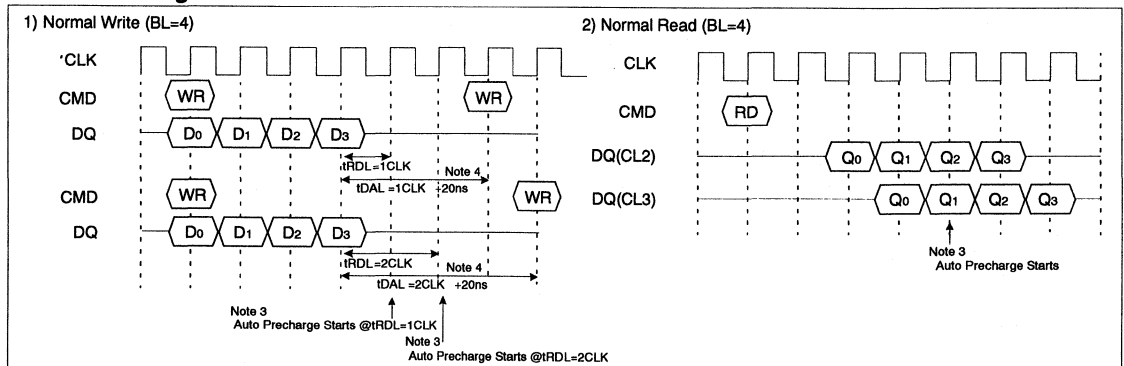


- *Note :**
1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
 2. To inhibit invalid write, DQM should be issued.
 3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of four banks operation.

6. Precharge



7. Auto Precharge

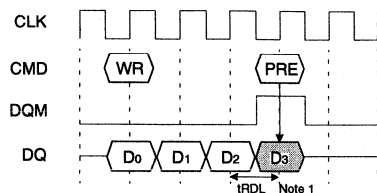


- *Note :**
1. SAMSUNG can support $t_{RDL}=1\text{CLK}$ and $t_{RDL}=2\text{CLK}$ for all memory devices. SAMSUNG recommends $t_{RDL}=2 \text{ CLK}$.
 2. Number of valid output data after row precharge : 1, 2 for CAS Latency = 2, 3 respectively.
 3. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same bank is illegal
 4. t_{DAL} defined Last data in to Active delay. SAMSUNG can support $t_{DAL}=1\text{CLK}+20\text{ns}$ and $2\text{CLK}+20\text{ns}$, recommends $t_{DAL}=2\text{CLK}+20\text{ns}$.

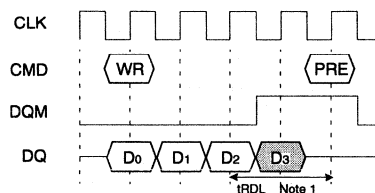
8. Burst Stop & Interrupted by Precharge

1) Normal Write

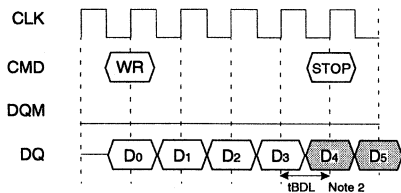
BL=4 & tRDL=1CLK



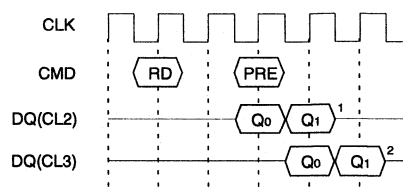
BL=4 & tRDL=2CLK



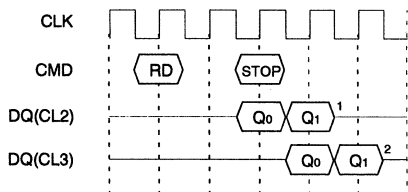
2) Write Burst Stop (BL=8)



3) Read Interrupted by Precharge (BL=4)

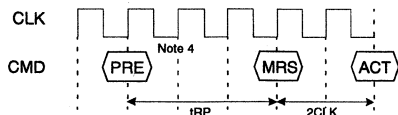


4) Read Burst Stop (BL=4)



9. MRS

1) Mode Register Set



***Note :** 1. SAMSUNG can support tRDL=1CLK and tRDL=2CLK for all memory devices. SAMSUNG recommends tRDL=2 CLK.

2. tRDL : 1 CLK ; Last data in to burst stop delay.

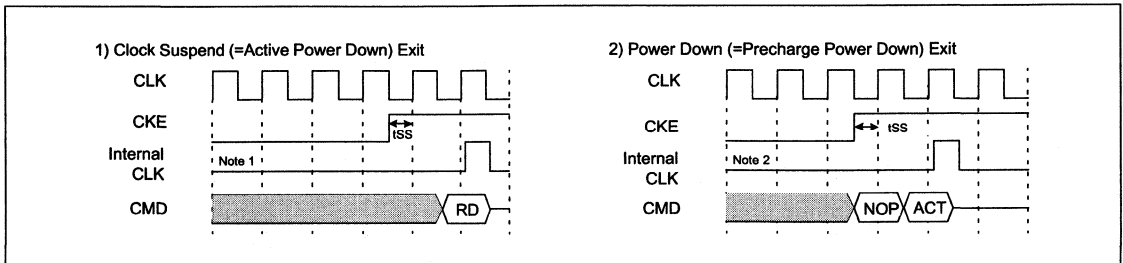
Read or write burst stop command is valid at every burst length.

3. Number of valid output data after row precharge or burst stop : 1, 2 for CAS latency= 2, 3 respectively.

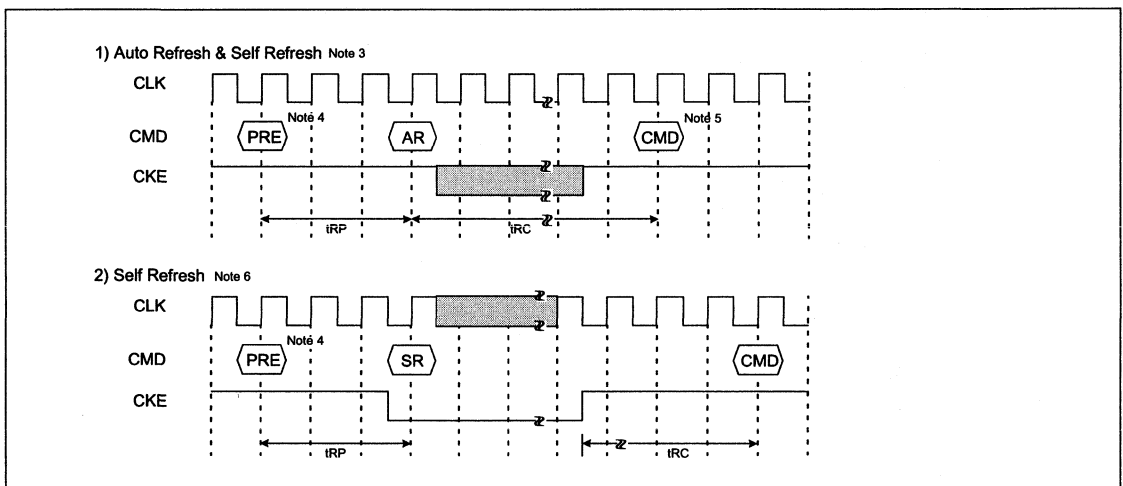
4. PRE : All banks precharge if necessary.

MRS can be issued only at all banks precharge state.

10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



- *Note :**
1. Active power down : one or more banks active state.
 2. Precharge power down : all banks precharge state.
 3. The auto refresh is the same as CBR refresh of conventional DRAM.
No precharge commands are required after auto refresh command.
During t_{rc} from auto refresh command, any other command can not be accepted.
 4. Before executing auto/self refresh command, all banks must be idle state.
 5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
 6. During self refresh mode, refresh interval and refresh operation are performed internally.
After self refresh entry, self refresh mode is kept while CKE is low.
During self refresh mode, all inputs except CKE will be don't cared, and outputs will be in Hi-Z state.
For the time interval of t_{rc} from self refresh exit command, any other command can not be accepted.
Before/After self refresh mode, burst auto refresh cycle is recommended.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A ₃ = "0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A ₃ = "1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting
Random MODE	Random column Access tccd = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS A _{2,1,0} = "000". At auto precharge, t _{ras} should not be violated.
	2	At MRS A _{2,1,0} = "001". At auto precharge, t _{ras} should not be violated.
	4	At MRS A _{2,1,0} = "010".
	8	At MRS A _{2,1,0} = "011".
	Full Page	At MRS A _{2,1,0} = "111". Wrap around mode(infinite burst length) should be stopped by burst stop. RAS interrupt or CAS interrupt
Special MODE	BRSW	At MRS A ₀ = "1". Read burst =1, 2, 4, 8, full page write Burst =1 At auto precharge of write, t _{ras} should not be violated.
Random MODE	Burst Stop	t _{bol} = 1, Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{\text{RAS}}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t _{rdl} = 2 with DQM, valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. During read/write burst with auto precharge, $\overline{\text{RAS}}$ interrupt can not be issued.
	$\overline{\text{CAS}}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{\text{CAS}}$ interrupt can not be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A10/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
Row Active	L	L	L	L	OP code	OP code	Mode Register Access	5
	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A10/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A10/AP	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
Read	L	L	H	L	BA	A10/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
Write	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New read, Determine AP	3
Read with Auto Precharge	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
Write with Auto Precharge	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
Pre-charging	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Idle after trp	
	L	H	H	H	X	X	NOP --> Idle after trp	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
Pre-charging	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	NOP --> Idle after trp	4

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after trcd	
	L	H	H	H	X	X	NOP --> Row Active after trcd	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after trc	
	L	H	H	X	X	X	NOP --> Idle after trc	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations : RA = Row Address

BA = Bank Address

NOP = No Operation Command

CA = Column Address

AP = Auto Precharge

- *Note :**
1. All entries assume the CKE was active (High) during the precharge clock and the current clock cycle.
 2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
 3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
 4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A10/AP).
 5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (TABLE 2)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	ACTION	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after trfc (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after trfc (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
All Banks Precharge Power Down	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	7
	L	H	L	L	X	X	X	ILLEGAL	
All Banks Idle	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	8
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	L	H	X	Enter Self Refresh	8
Any State other than Listed above	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clock Suspend	

Abbreviations : ABI = All Banks Idle, RA = Row Address

*Note : 6. CKE low to high transition is asynchronous.

7. CKE low to high transition is asynchronous if restarts internal clock.

A minimum setup time 1CLK + tss must be satisfied before any command other than exit.

8. Power down and self refresh can be entered only from the both banks idle state.

9. Must be a legal command.

Single Bit Read - Write - Read Cycle(Same Page) @CAS Latency=3, Burst Length=1

Power Up Sequence

Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK

Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK

Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=1CLK

Page Read & Write Cycle at Same Bank @Burst Length=4, tRDL=2CLK

Page Read Cycle at Different Bank @Burst Length=4

Page Write Cycle at Different Bank @Burst Length=4, tRDL=1CLK

Page Write Cycle at Different Bank @Burst Length=4, tRDL=2CLK

Read & Write Cycle at Different Bank @Burst Length=4

Read & Write Cycle With Auto Precharge I @Burst Length=4

Read & Write Cycle With Auto Precharge II @Burst Length=4

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4

Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=1CLK

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=2CLK

Burst Read Single bit Write Cycle @Burst Length =2

Active/precharge Power Down Mode @CAS Latency=2 Burst Length=4

Self Refresh Entry & Exit Cycle & Exit Cycle

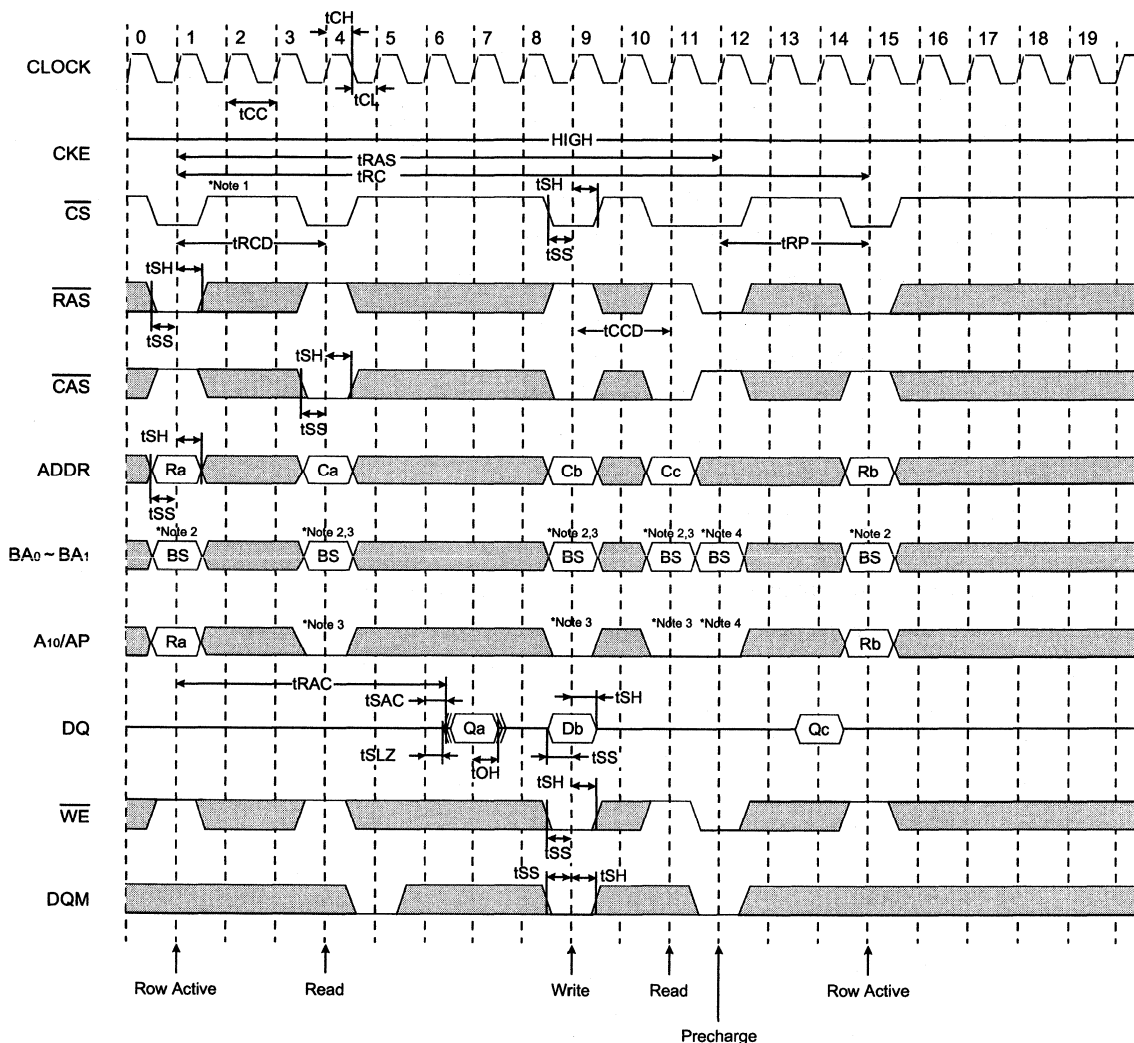
Mode Register Set Cycle

Auto Refresh Cycle

TIMING DIAGRAM

CMOS SDRAM

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



Don't care

- *Note : 1. All input except CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.
 2. Bank active & read/write are controlled by BA0~BA1.

BA0	BA1	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

3. Enable and disable auto precharge function are controlled by A10/AP in read/write command

A10/AP	BA0	BA1	Operation
0	0	0	Disable auto precharge, leave bank A active at end of burst.
	0	1	Disable auto precharge, leave bank B active at end of burst.
	1	0	Disable auto precharge, leave bank C active at end of burst.
	1	1	Disable auto precharge, leave bank D active at end of burst.
1	0	0	Enable auto precharge, precharge bank A at end of burst.
	0	1	Enable auto precharge, precharge bank B at end of burst.
	1	0	Enable auto precharge, precharge bank C at end of burst.
	1	1	Enable auto precharge, precharge bank D at end of burst.

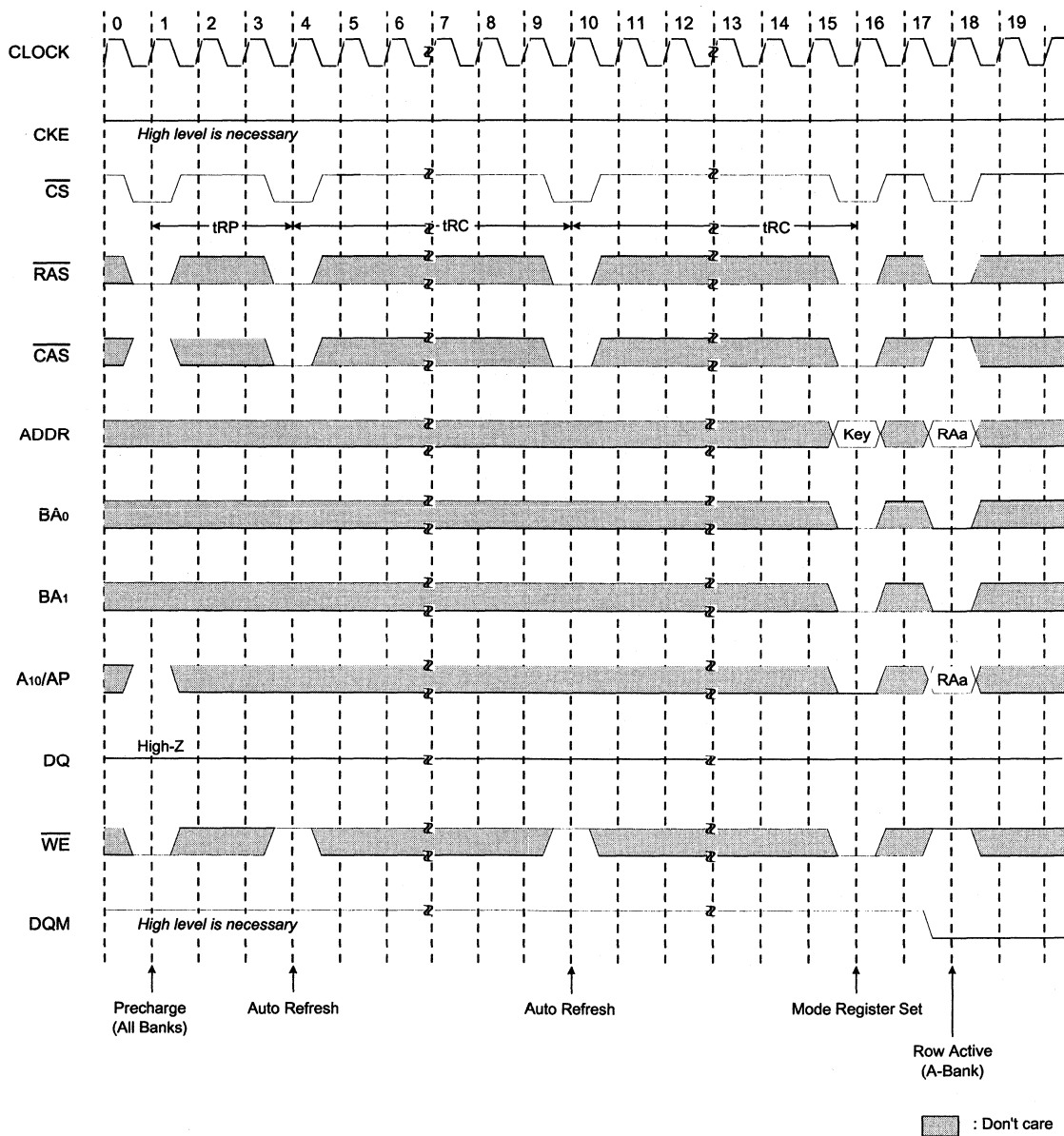
4. A10/AP and BA0~BA1 control bank precharge when precharge command is asserted.

A10/AP	BA0	BA1	Precharge
0	0	0	Bank A
0	0	1	Bank B
0	1	0	Bank C
0	1	1	Bank D
1	x	x	All Banks

TIMING DIAGRAM

CMOS SDRAM

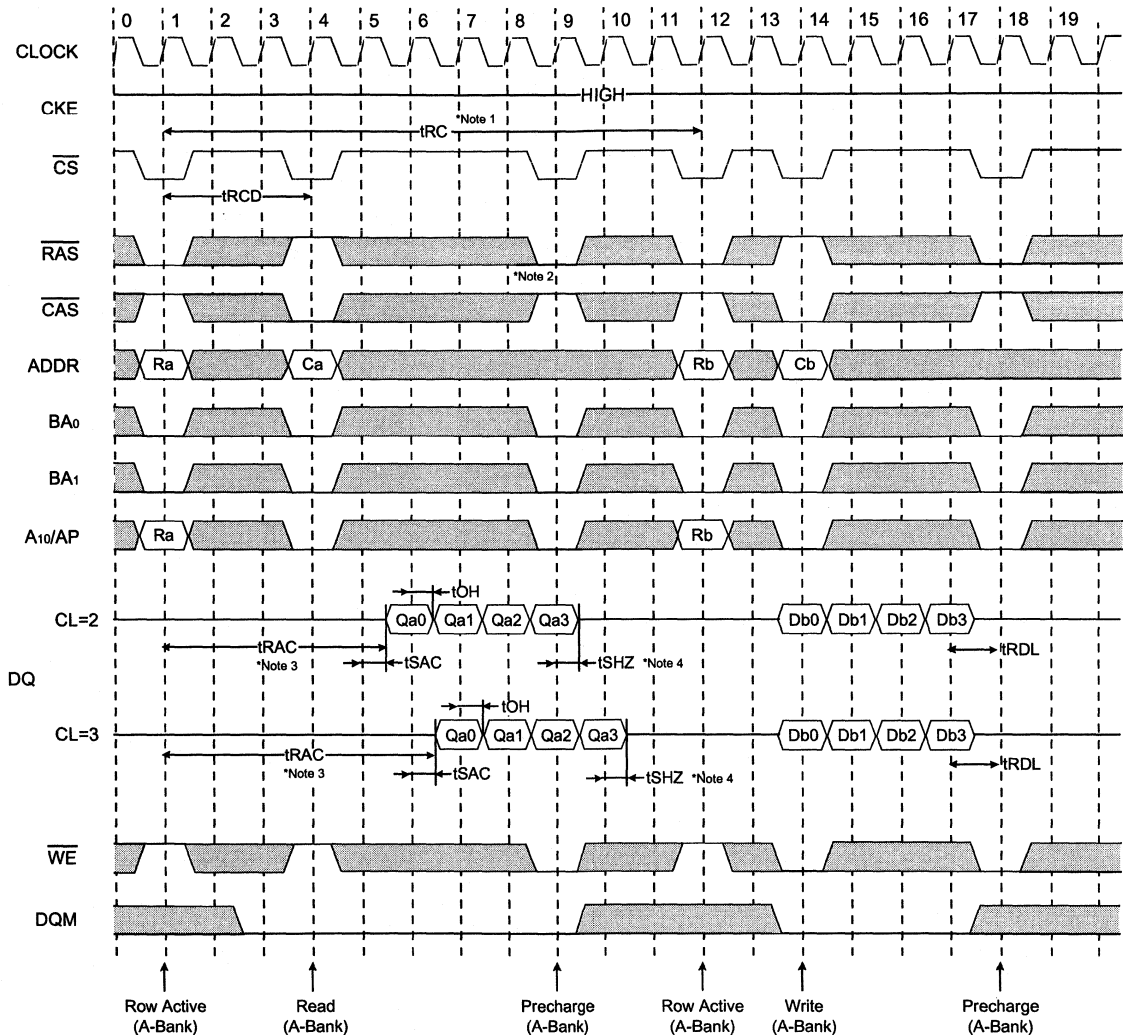
Power Up Sequence



TIMING DIAGRAM

CMOS SDRAM

Read & Write Cycle at Same Bank @Burst Length=4, $t_{RDL}=1CLK$



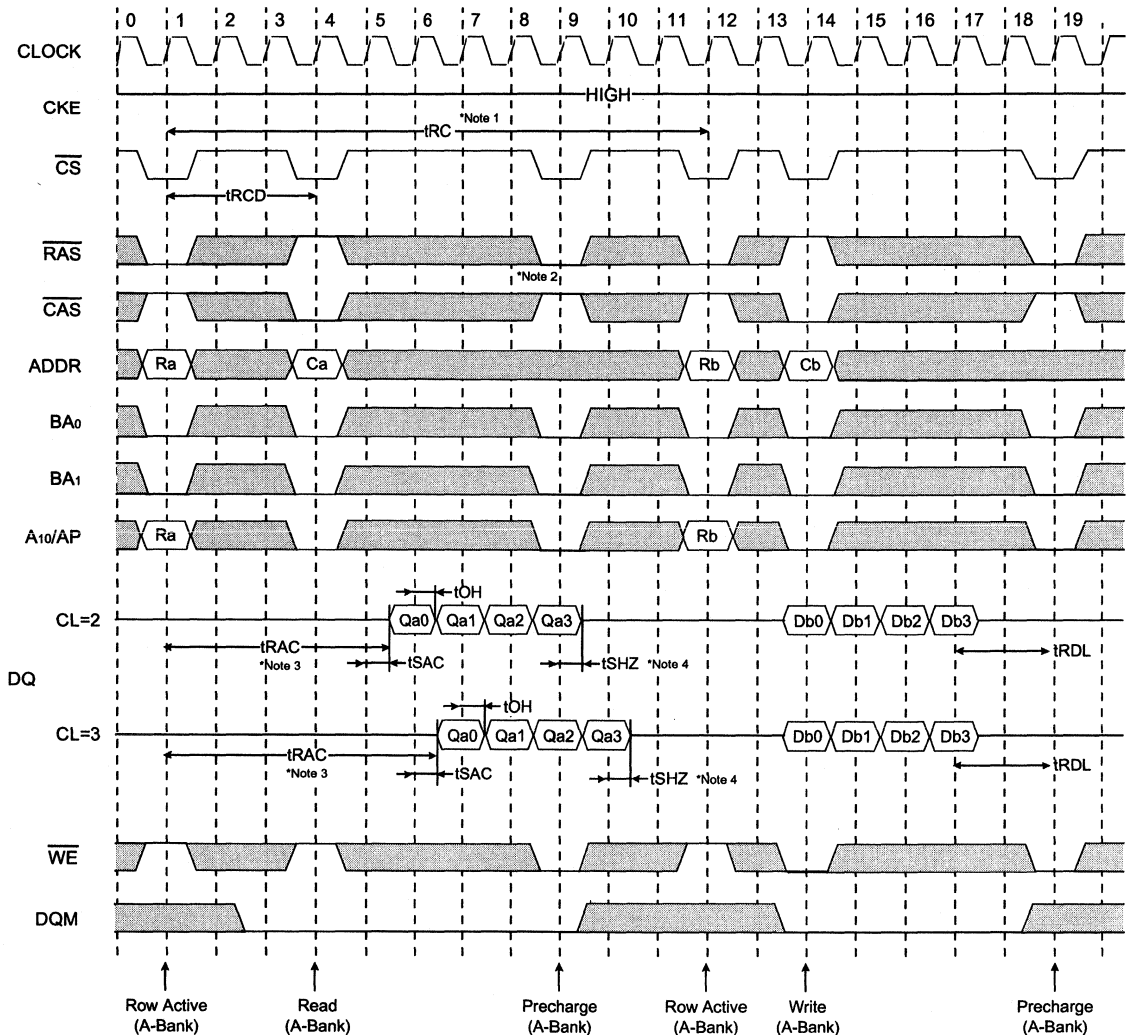
■ : Don't care

- *Note :**
1. Minimum row cycle times is required to complete internal DRAM operation.
 2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{shz}) after the clock.
 3. Access time from Row active command. $t_{acc} = (t_{RCD} + CAS\ latency - 1) + t_{SAC}$
 4. Output will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

TIMING DIAGRAM

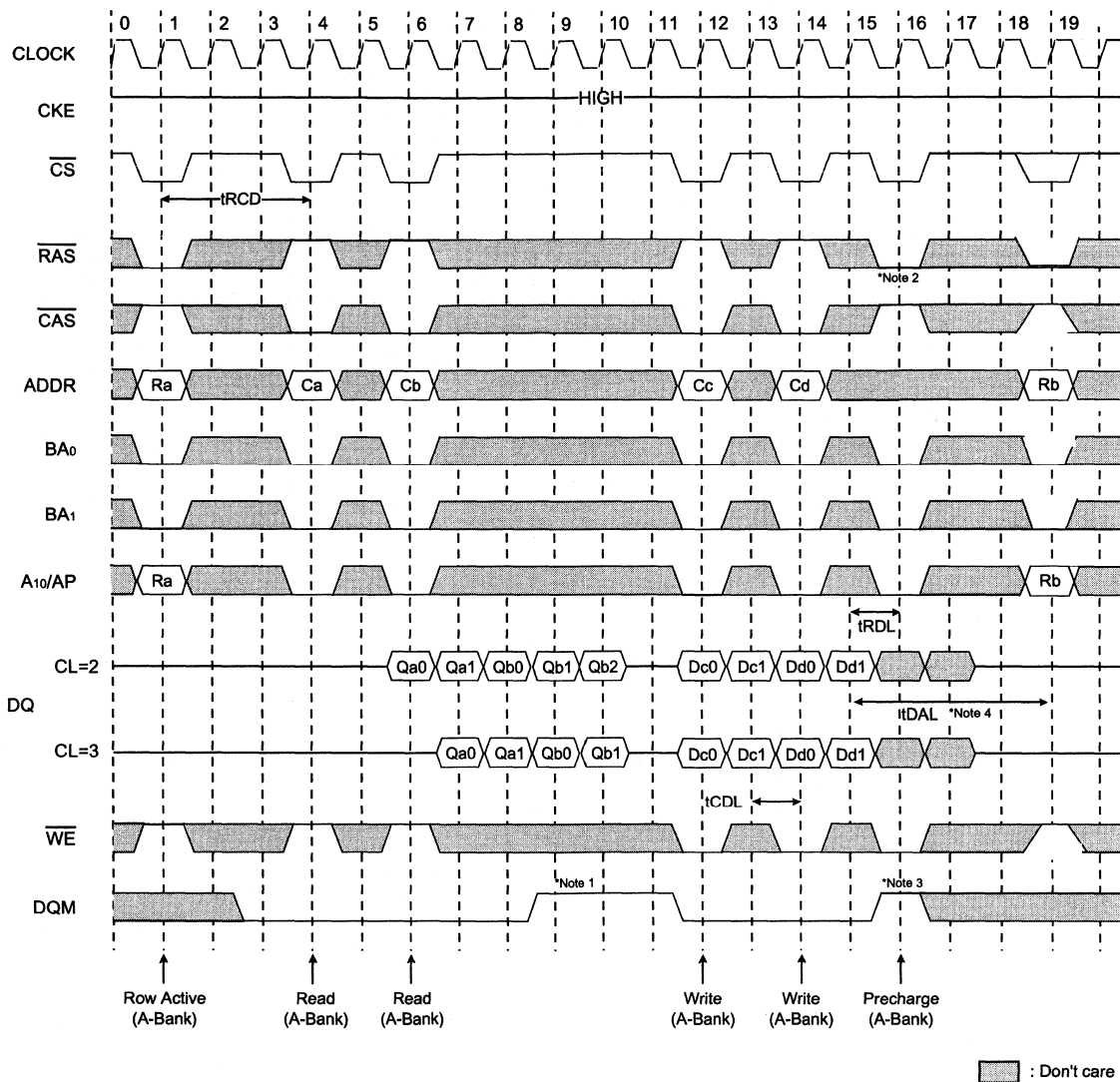
CMOS SDRAM

Read & Write Cycle at Same Bank @Burst Length=4, $t_{RDL}=2CLK$



□ : Don't care

- *Note :**
1. Minimum row cycle times is required to complete internal DRAM operation.
 2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clock.
 3. Access time from Row active command. $t_{CC} = (t_{RCD} + \text{CAS latency} - 1) + t_{SAC}$
 4. Output will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

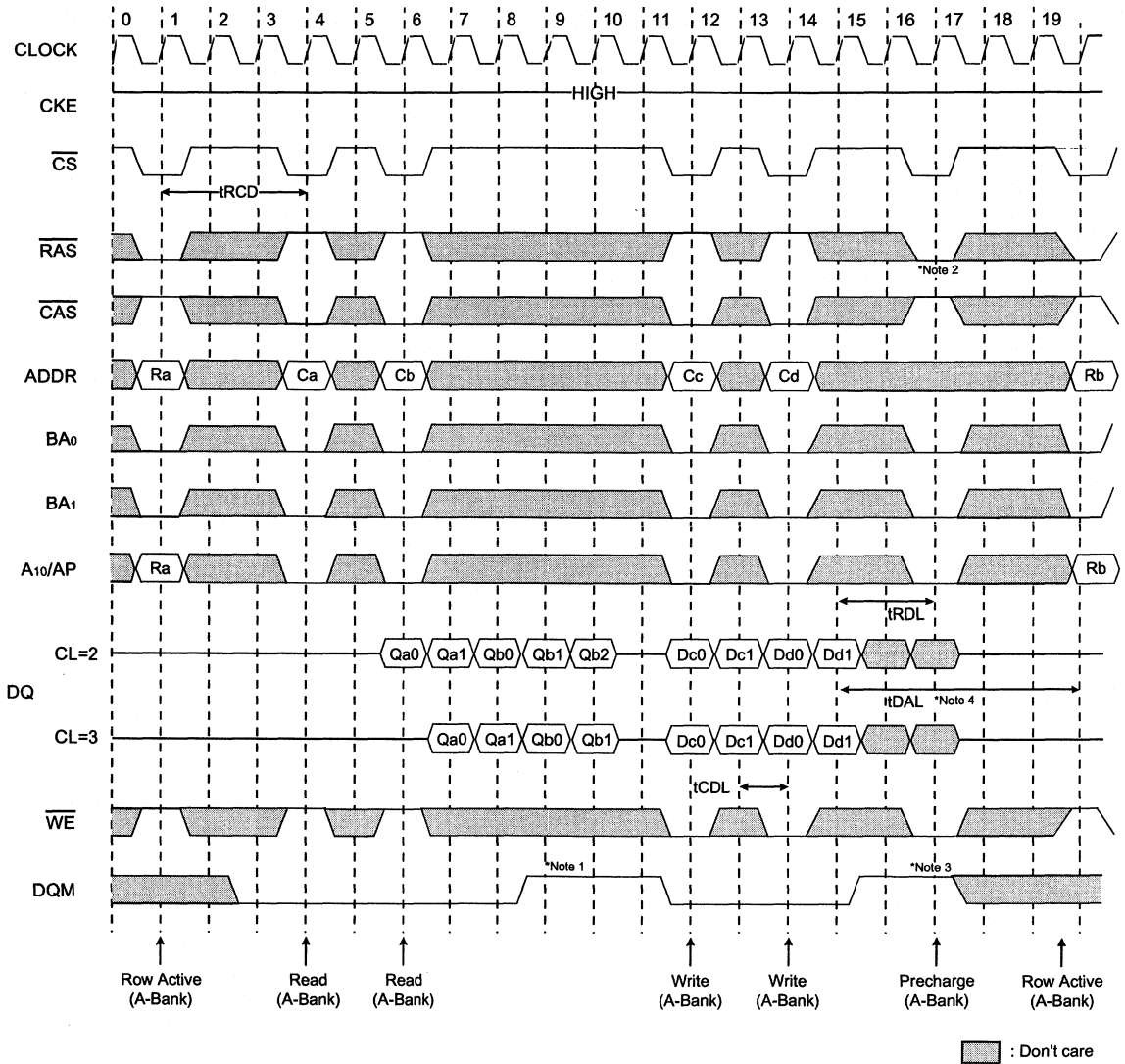
Page Read & Write Cycle at Same Bank @Burst Length=4, $t_{RDL}=1CLK$ 

- *Note :**
1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
 2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.
 3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
 4. tDAL, last data in to active delay, is $1CLK + 20ns$

TIMING DIAGRAM

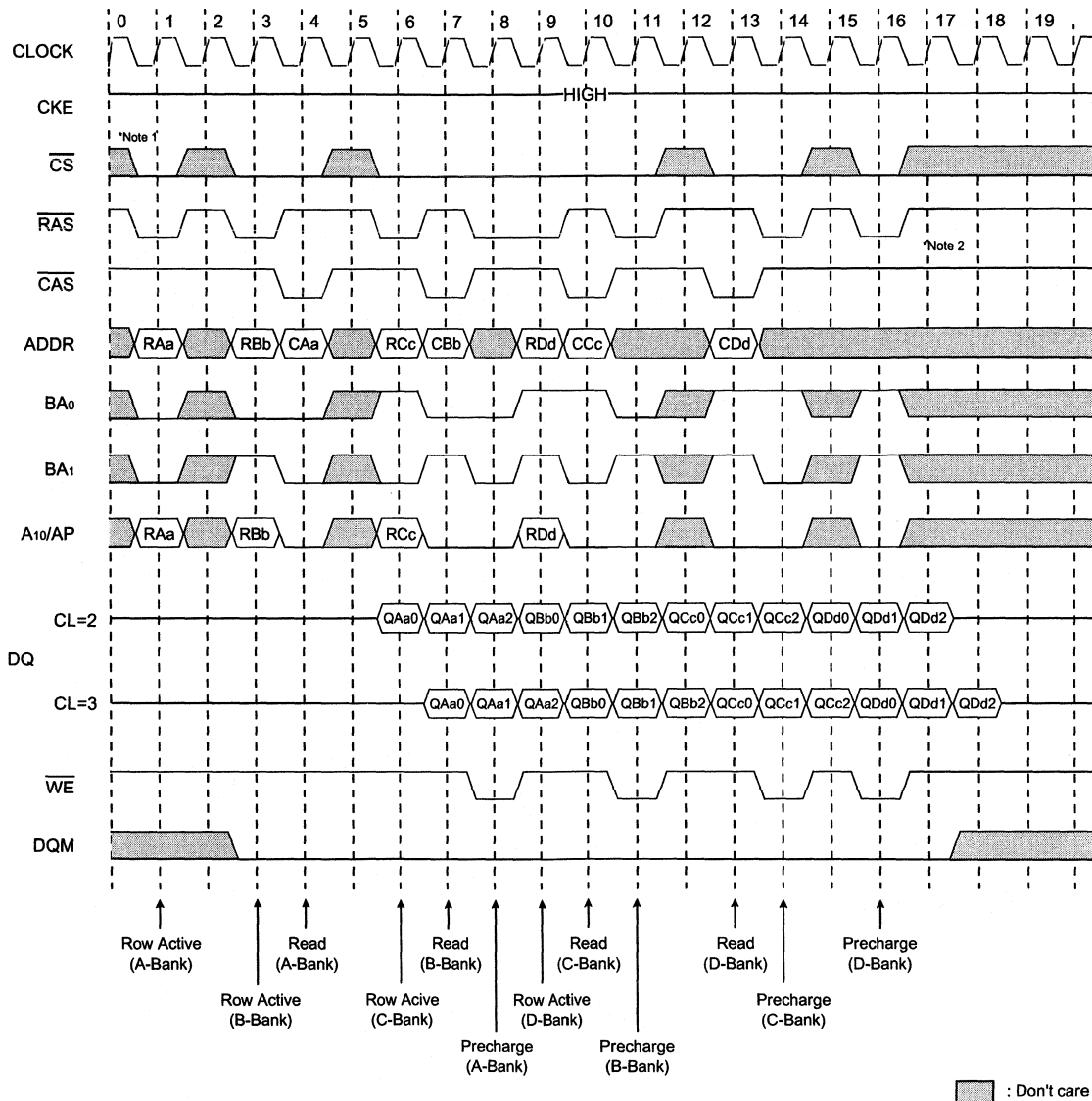
CMOS SDRAM

Page Read & Write Cycle at Same Bank @Burst Length=4, $t_{RD L}=2CLK$



- *Note :**
1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
 2. Row precharge will interrupt writing. Last data input, $t_{RD L}$ before Row precharge, will be written.
 3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
 4. t_{DAL} , last data in to active delay, is $2CLK + 20ns$.

Page Read Cycle at Different Bank @Burst Length=4

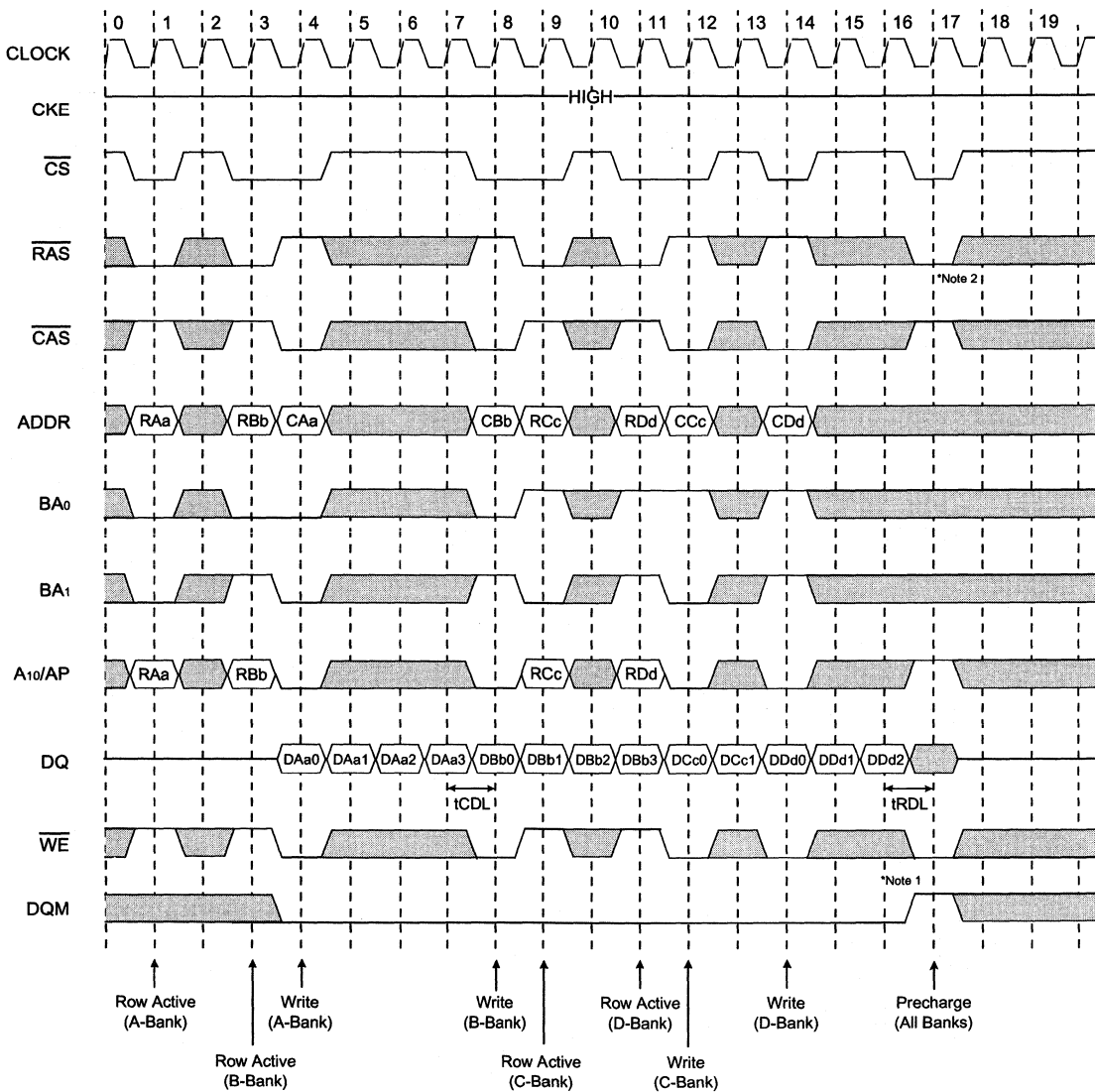


***Note :** 1. $\overline{CS}$ can be don't care when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going dege.
 2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

TIMING DIAGRAM

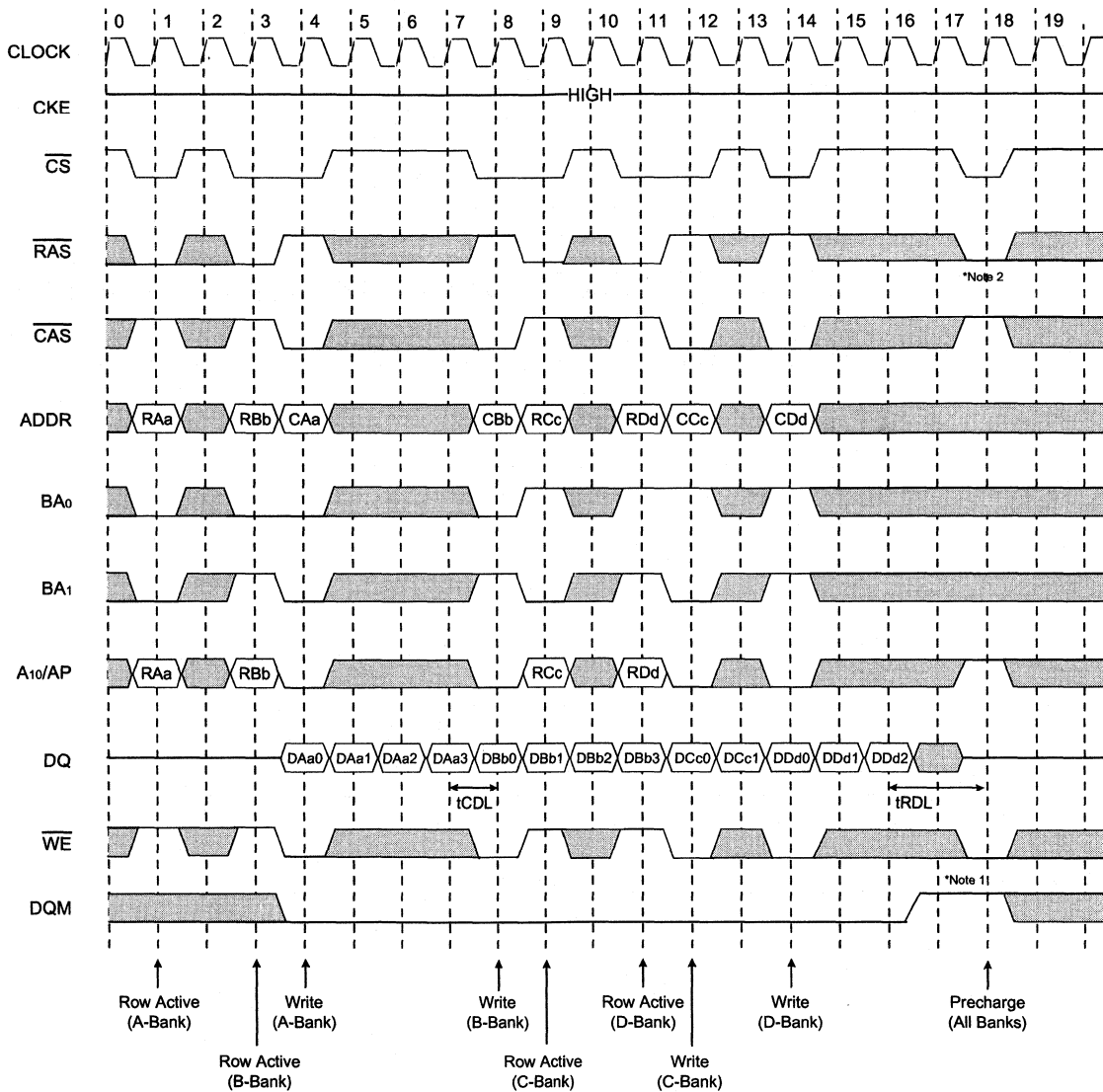
CMOS SDRAM

Page Write Cycle at Different Bank @Burst Length=4, tRDL=1CLK



□ : Don't care

***Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

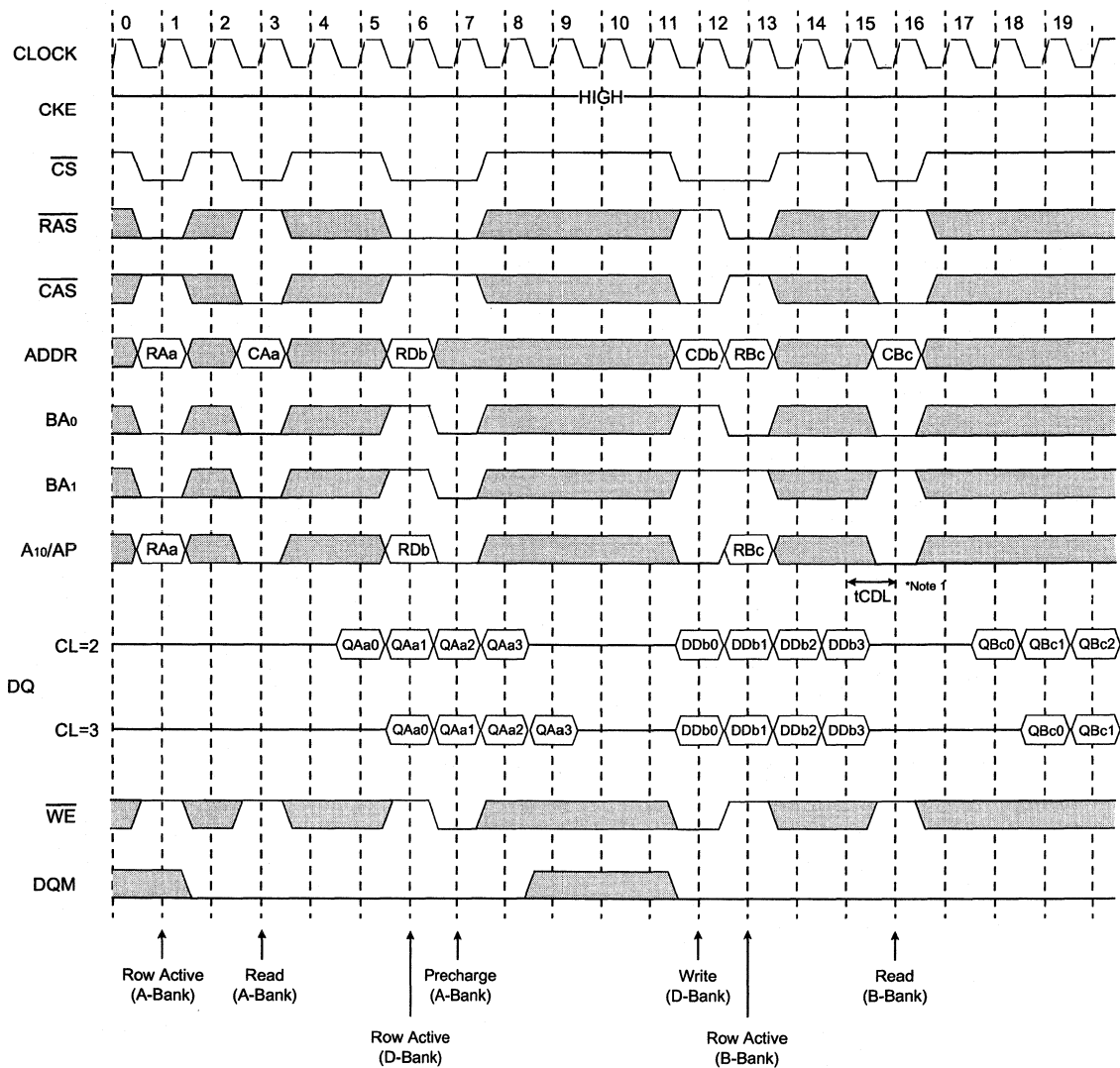
Page Write Cycle at Different Bank @Burst Length=4, t_{RDL}=2CLK

***Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
 2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

TIMING DIAGRAM

CMOS SDRAM

Read & Write Cycle at Different Bank @Burst Length=4

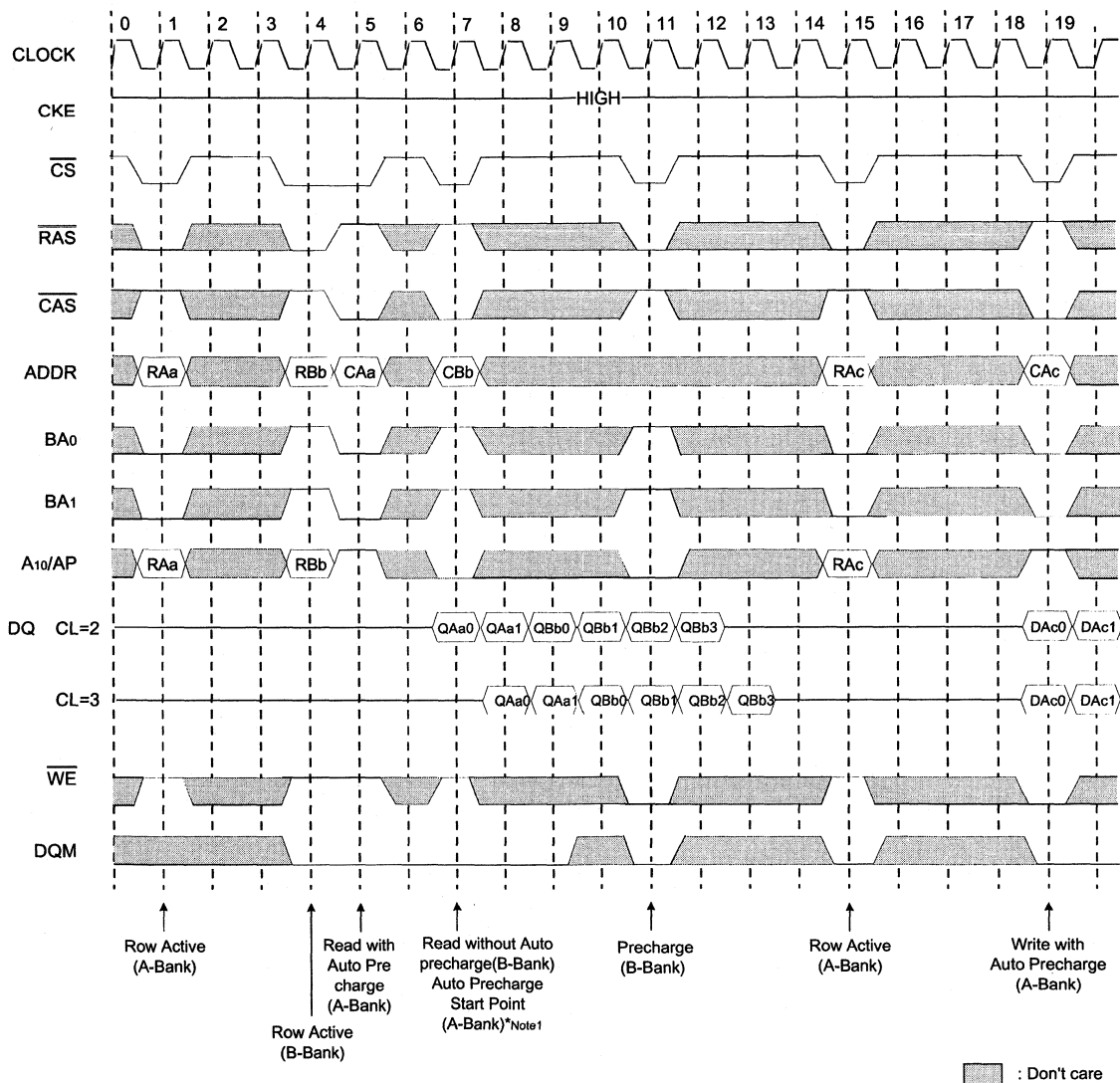


*Note : 1. t_{CDL} should be met to complete write.

TIMING DIAGRAM

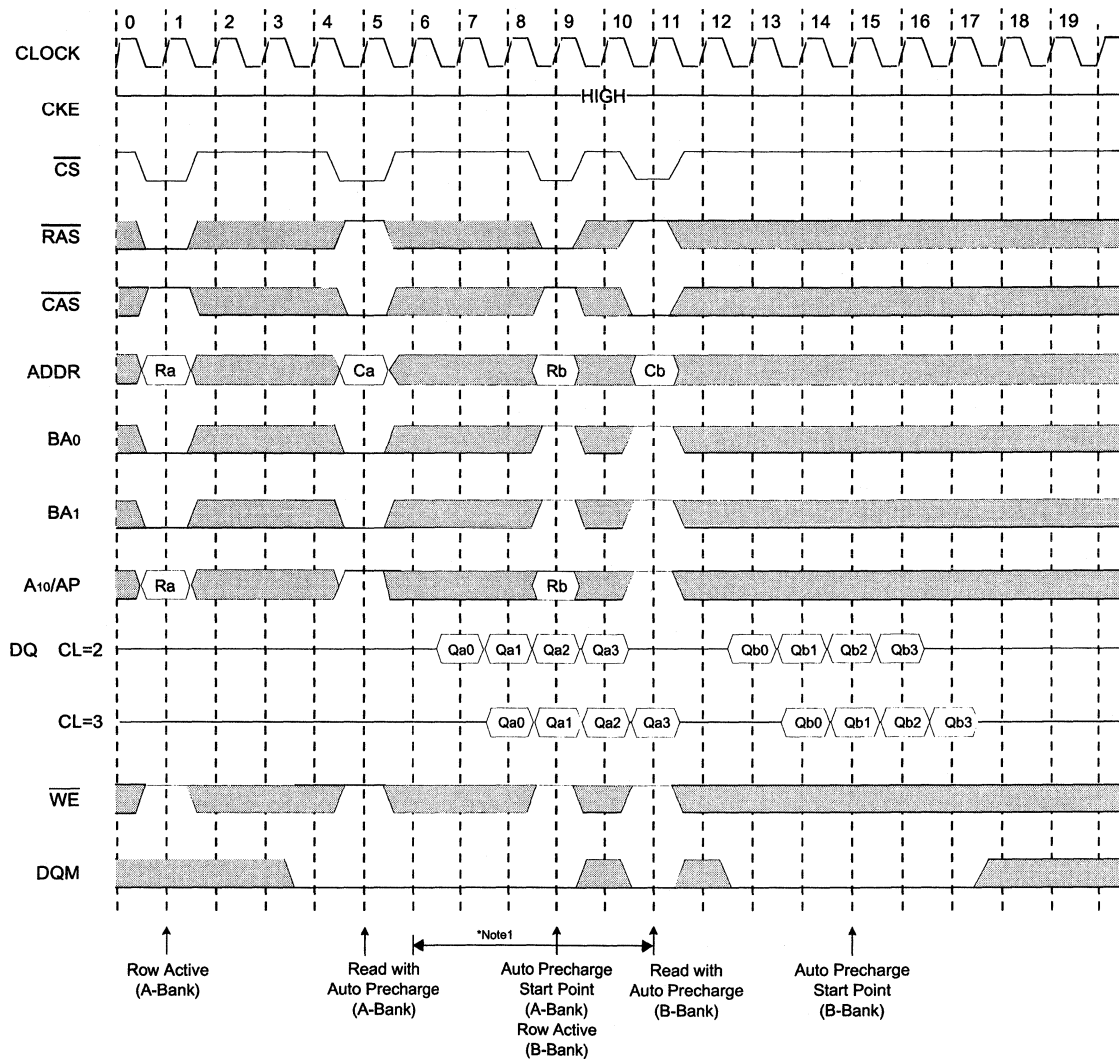
CMOS SDRAM

Read & Write Cycle with Auto Precharge I @Burst Length=4



- *Note1:** When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation.
- if Read(Write) command without auto precharge is issued at B-Bank before A-Bank auto precharge starts, A-Bank auto precharge will start at B-Bank read command input point.
 - any command can not be issued at A-Bank during tRP after A-Bank auto precharge starts.

Read & Write Cycle with Auto Precharge II @Burst Length=4

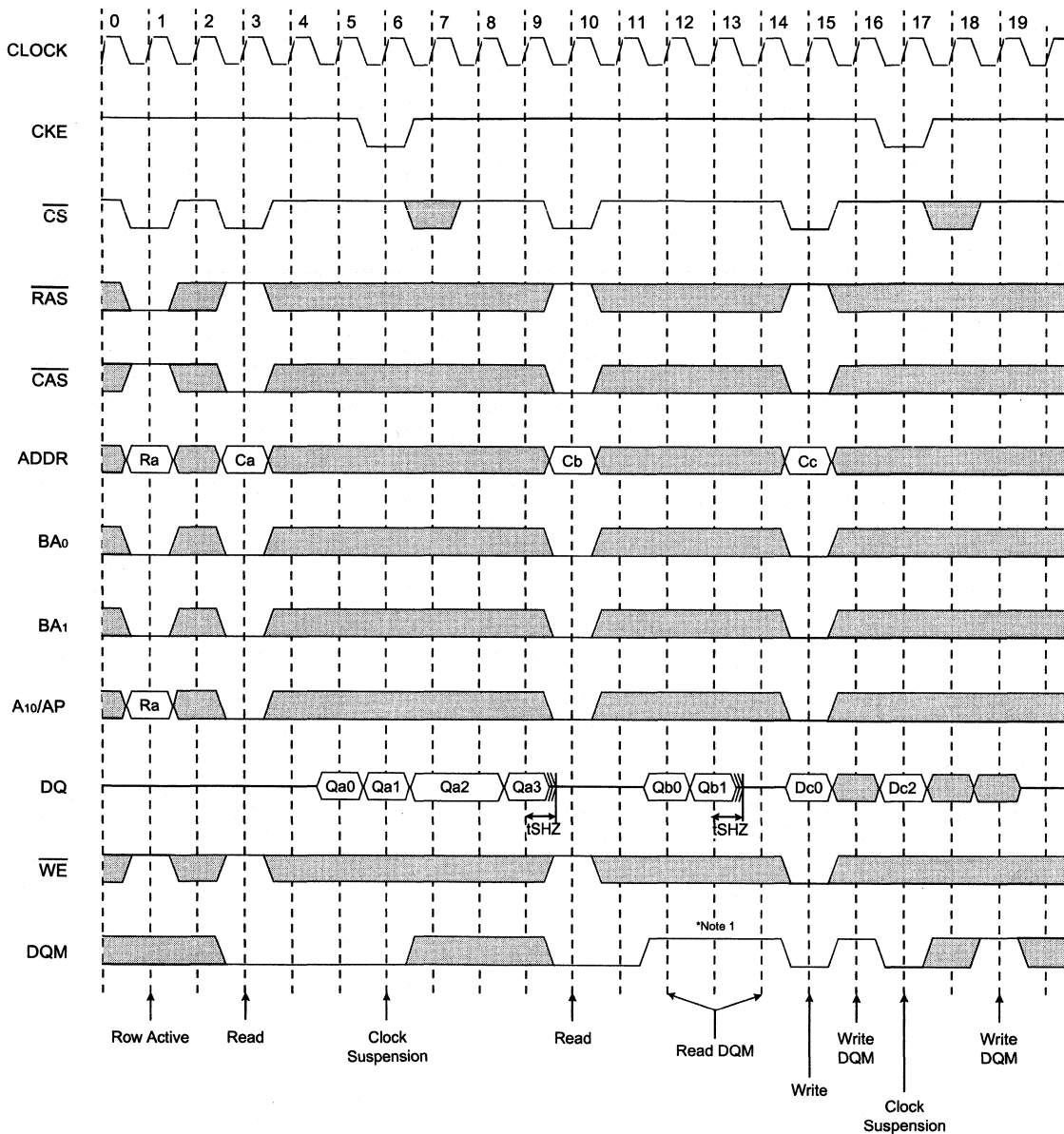


***Note 1:** Any command to A-bank is not allowed in this period.
tRP is determined from at auto precharge start point

TIMING DIAGRAM

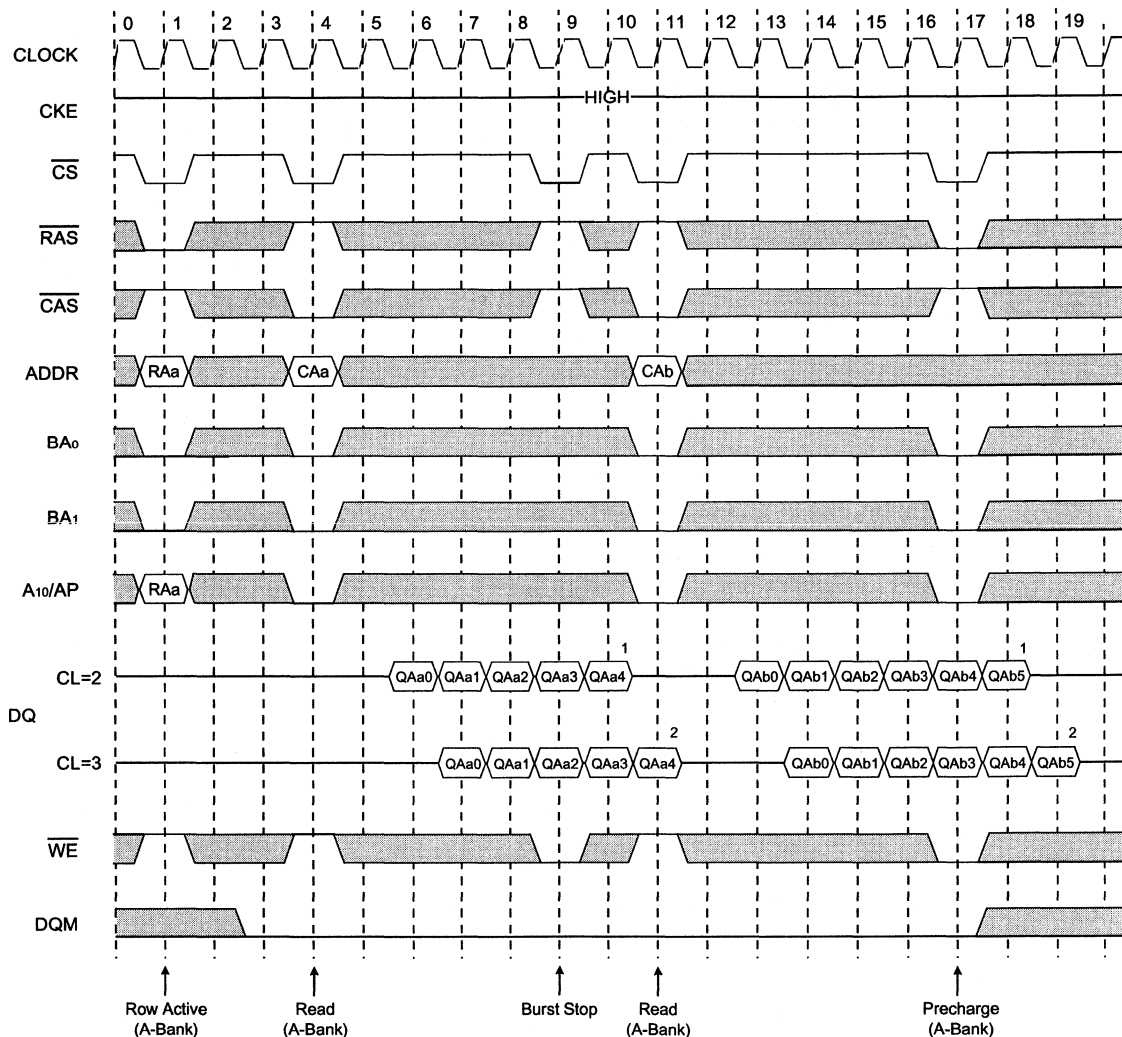
CMOS SDRAM

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



*Note1 : DQM is needed to prevent bus contention.

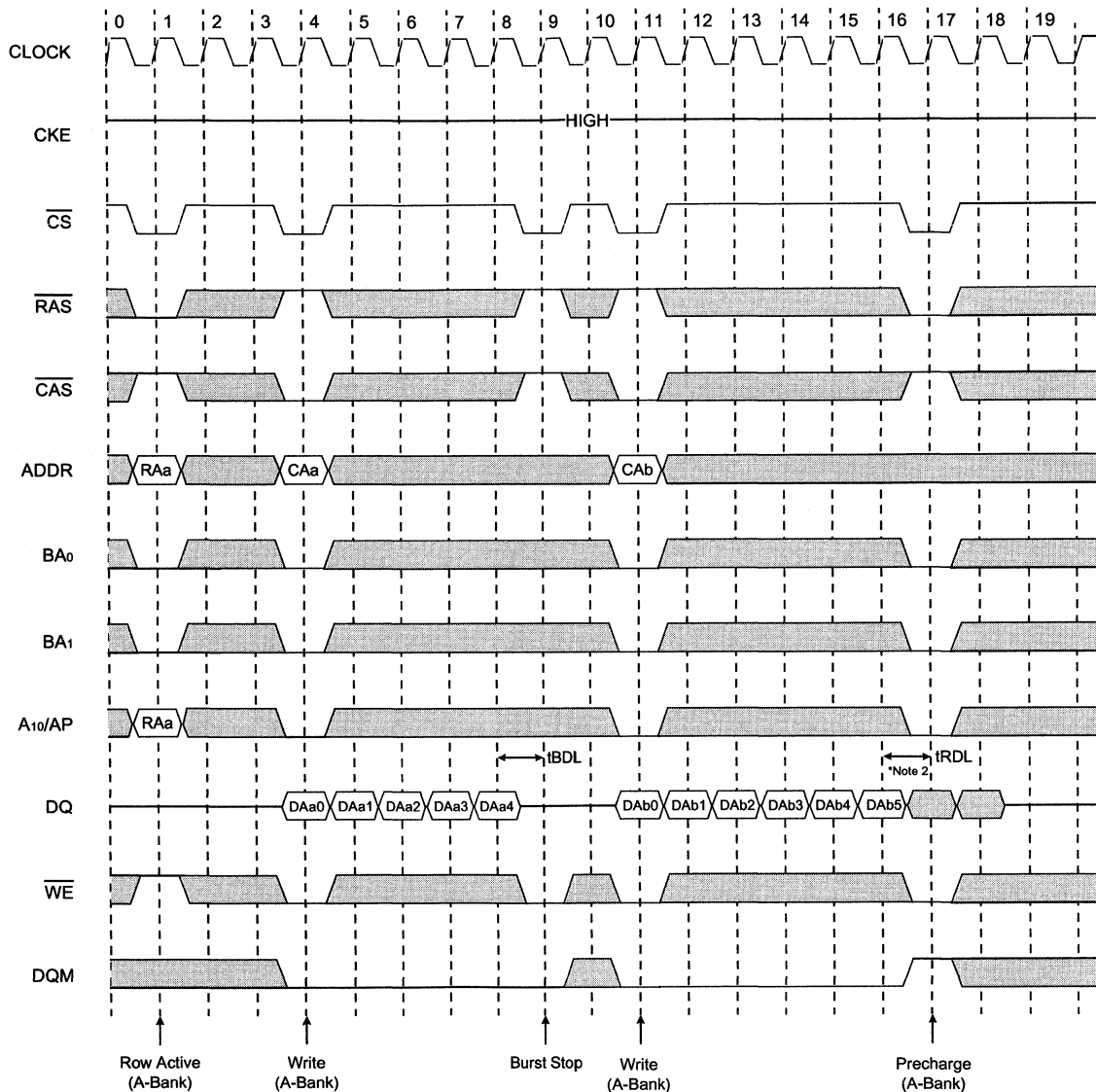
Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Full Page Burst



□ : Don't care

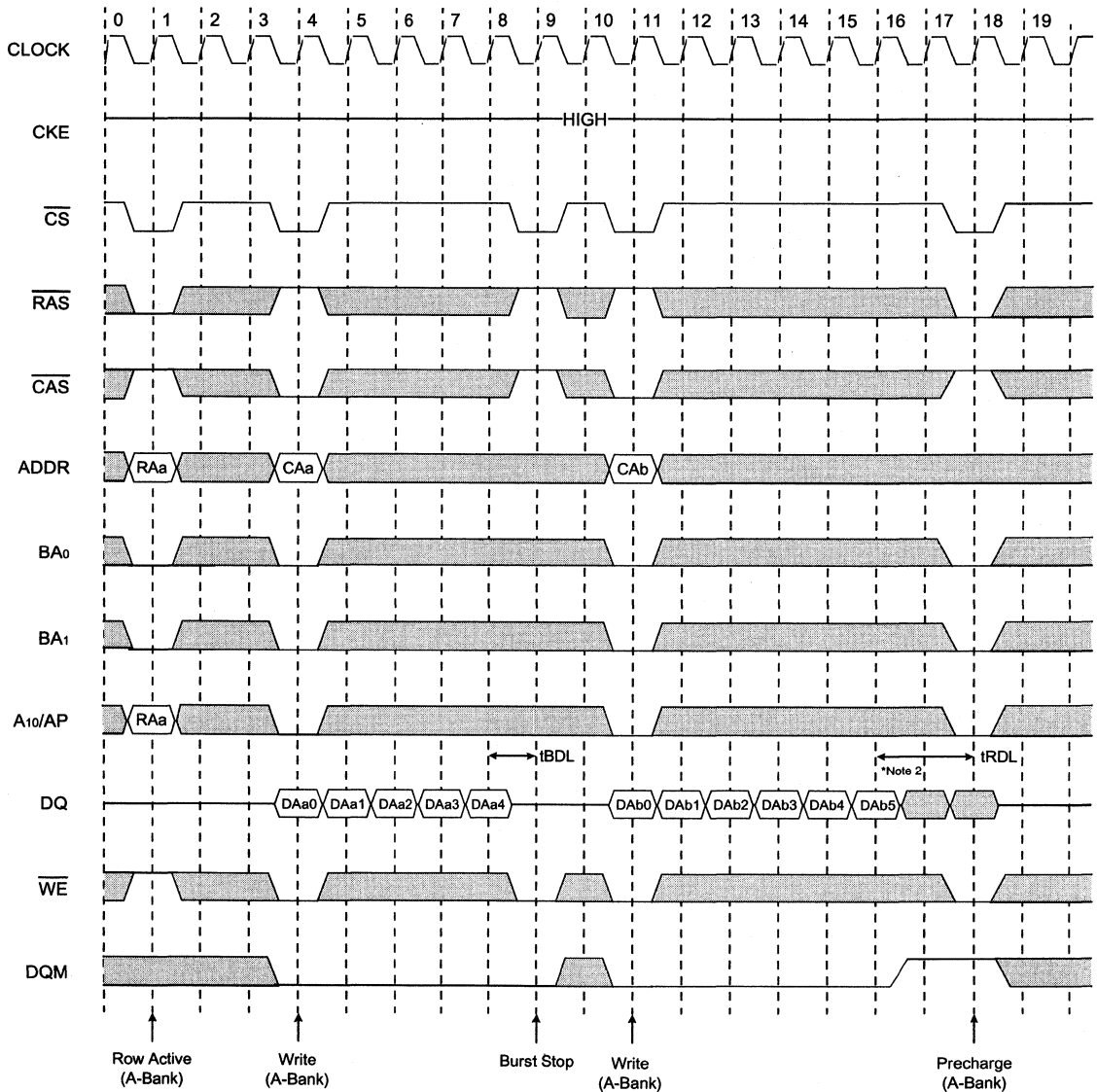
- *Note :**
1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
 2. About the valid DQs after burst stop, it is same as the case of RAS interrupt. Both cases are illustrated above timing diagram. See the label 1, 2 on them. But at burst write, Burst stop and RAS interrupt should be compared carefully. Refer the timing diagram of "Full page write burst stop cycle".
 3. Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, tRDL=1CLK



- *Note :**
1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
 2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of tRDL.
DQM at write interrupted by precharge command is needed to prevent invalid write.
DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
 3. Burst stop is valid at every burst length.

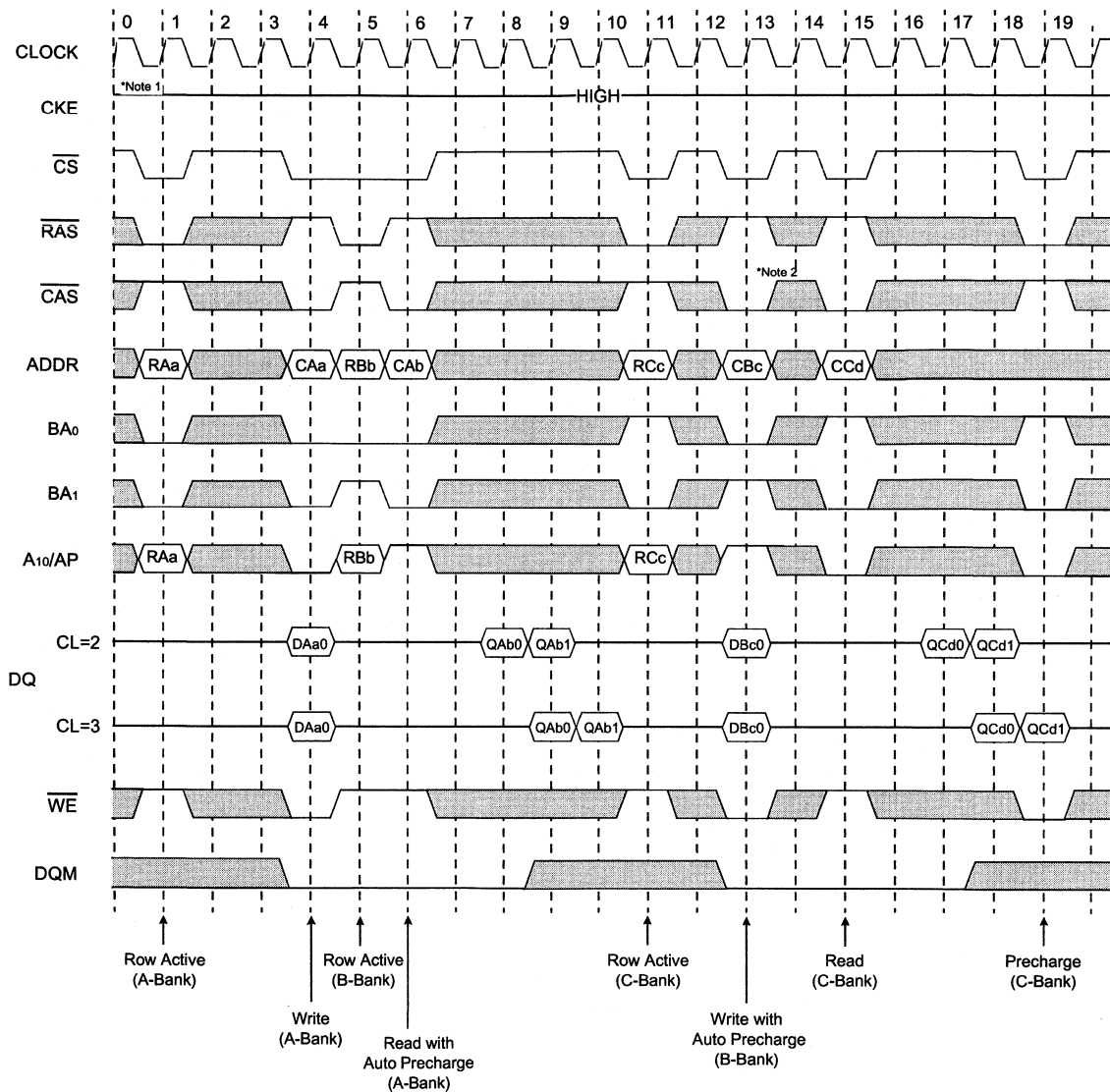
■ : Don't care

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Full Page Burst, $t_{RDL}=2CLK$ 

- *Note :**
1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
 2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL} .
DQM at write interrupted by precharge command is needed to prevent invalid write.
DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
 3. Burst stop is valid at every burst length.

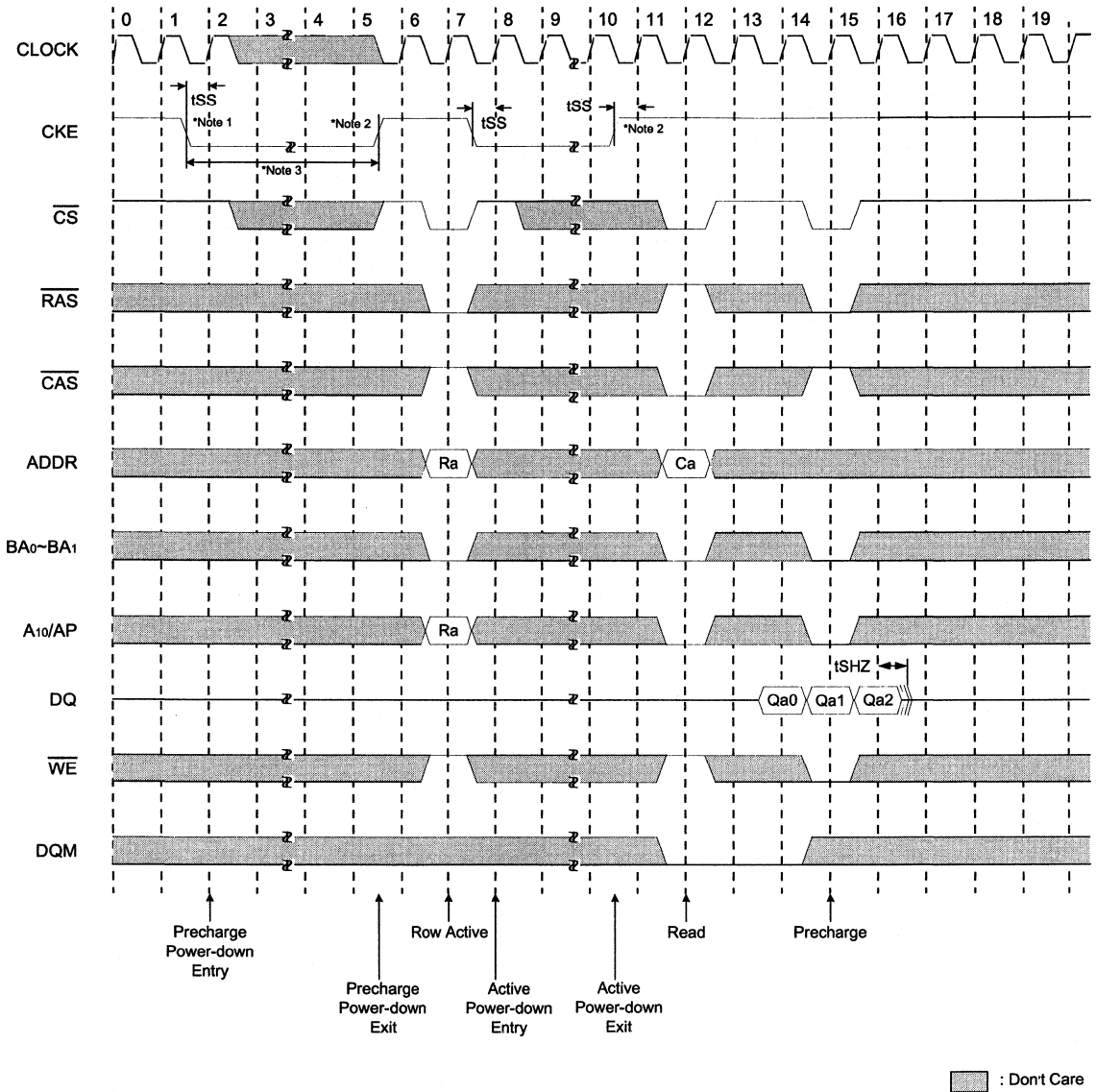
■ : Don't care

Burst Read Single bit Write Cycle @Burst Length=2



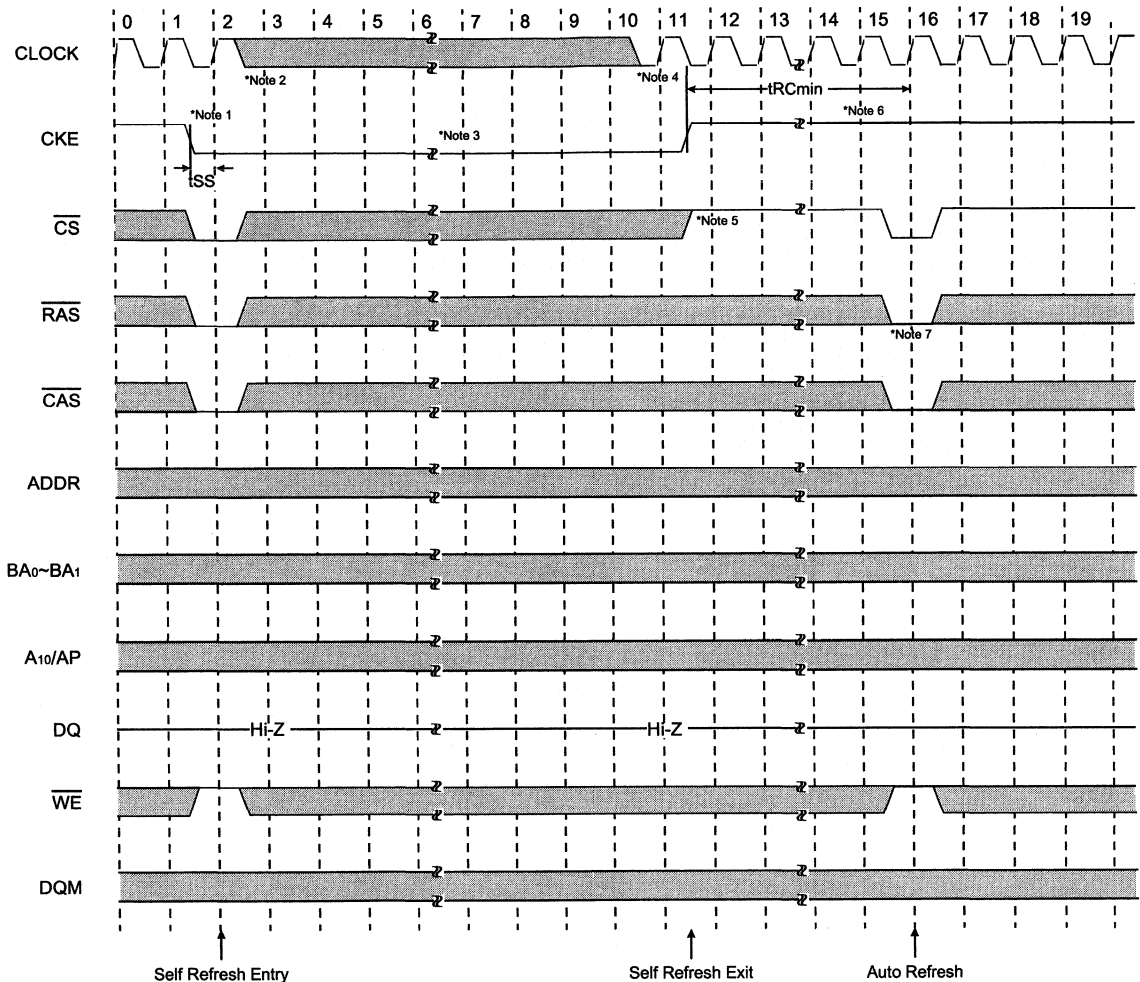
- *Note :**
1. BRSW modes is enabled by setting A₉ "High" at MRS (Mode Register Set).
At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
 2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



- *Note :**
1. Both banks should be in idle state prior to entering precharge power down mode.
 2. CKE should be set high at least $1CLK + t_{ss}$ prior to Row active command.
 3. Can not violate minimum refresh specification. (64ms)

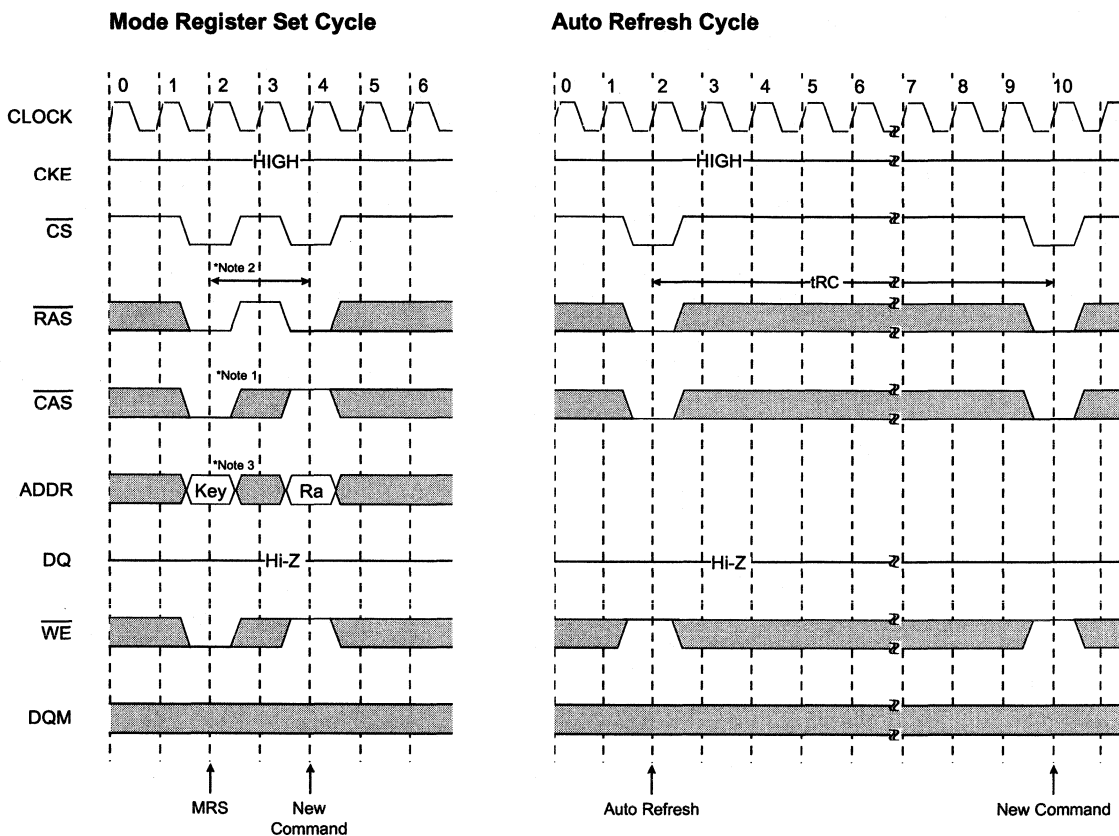
Self Refresh Entry & Exit Cycle

***Note : TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
(cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

TO EXIT SELF REFRESH MODE

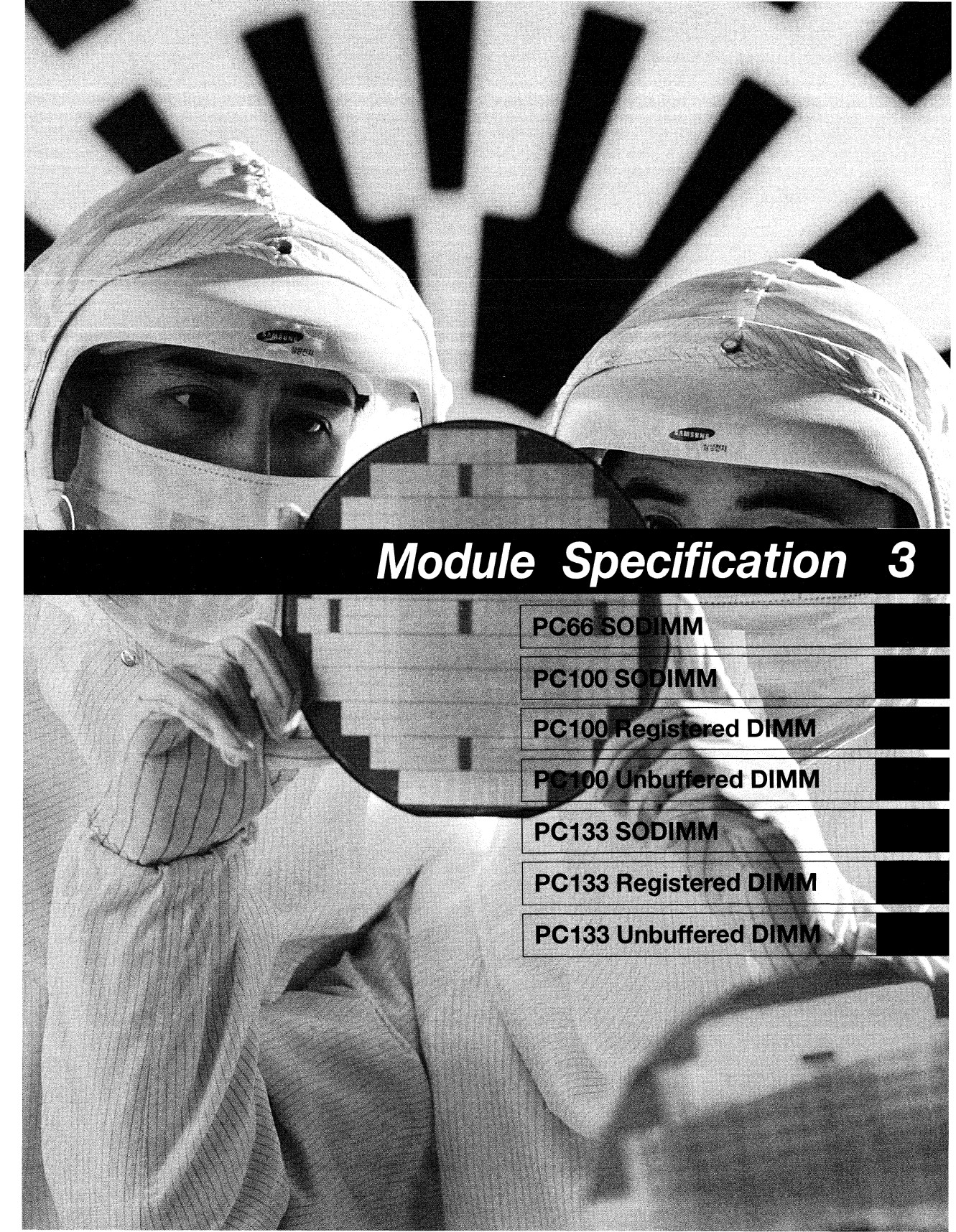
4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 4K cycle(64Mb 5th, 128Mb 2nd/3rd) or 8K cycle(256Mb 2nd) of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.



* All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

- *Note :**
1. CS, RAS, CAS, & WE activation at the same clock cycle with address key will set internal mode register.
 2. Minimum 2 clock cycles should be met before new RAS activation.
 3. Please refer to Mode Register Set table.



Module Specification 3

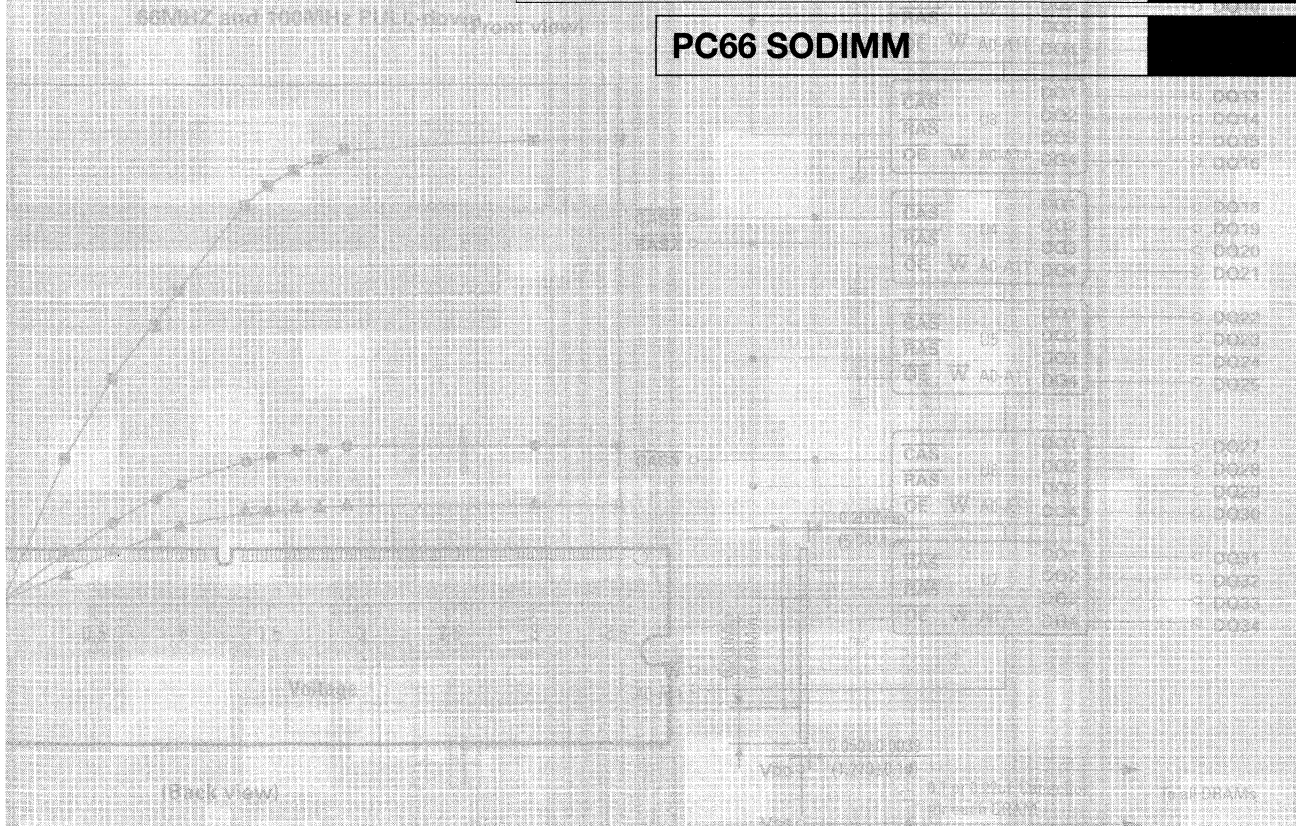
PC66 SODIMM	
PC100 SODIMM	
PC100 Registered DIMM	
PC100 Unbuffered DIMM	
PC133 SODIMM	
PC133 Registered DIMM	
PC133 Unbuffered DIMM	



Module Specification

3

PC66 SODIMM



M466S0924MT0 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S0924MT0 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0924MT0 consists of four CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0924MT0 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S0924MT0-L10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

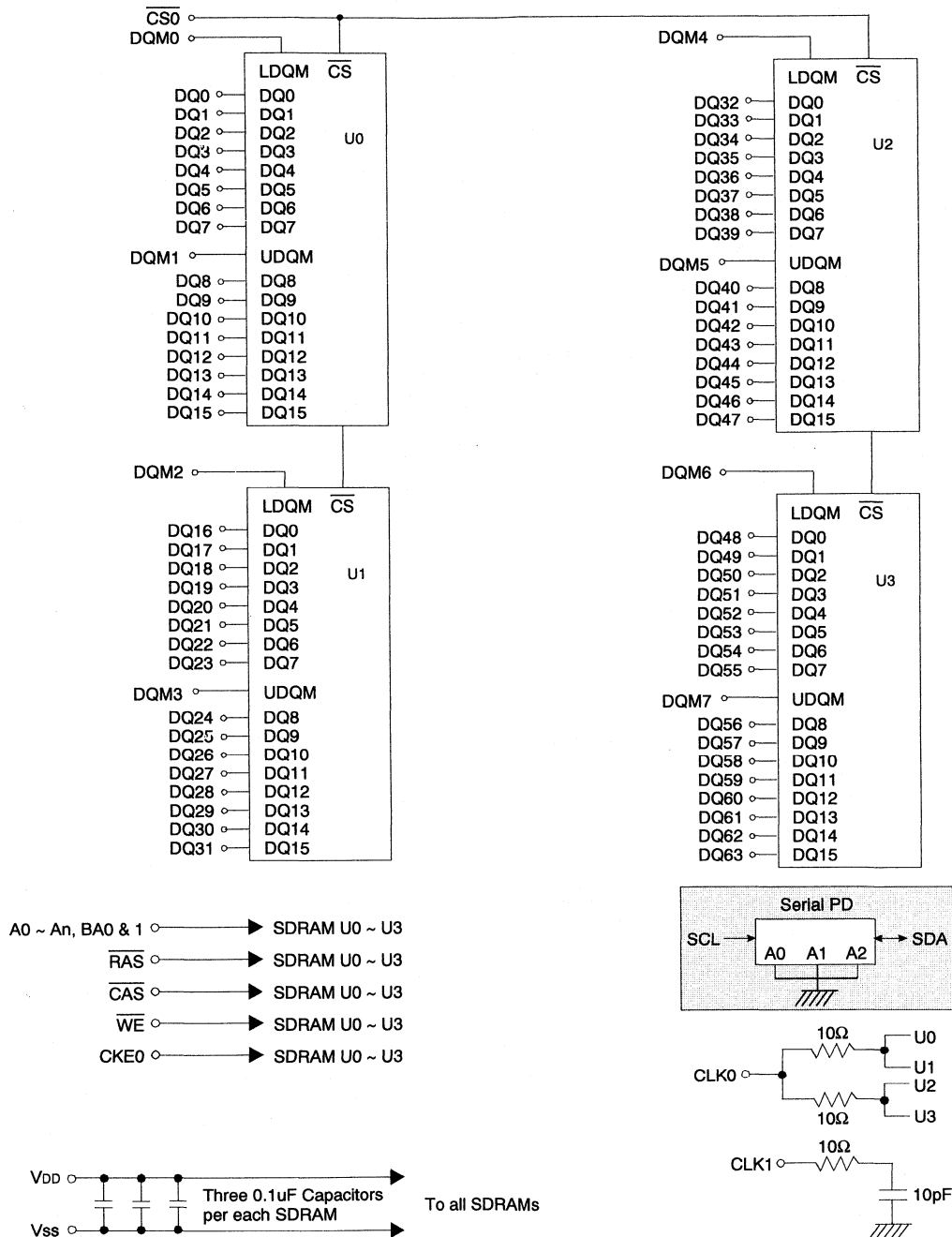
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{CS}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RAO ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	4	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	30	40	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	30	40	pF
Input capacitance (CKE ₀)	C _{IN3}	25	35	pF
Input capacitance (CLK ₀)	C _{IN4}	25	35	pF
Input capacitance ($\overline{\text{CS}}$ ₀)	C _{IN5}	25	35	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	5	15	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	5	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

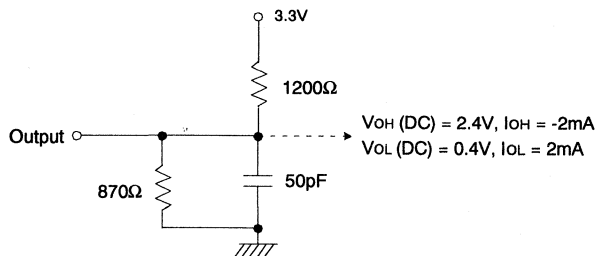
Parameter	Symbol	Test Condition	CAS Latency	Version	Unit	Note
				-10		
Operating current (One bank active)	Icc1	Burst length = 1 $t_{RC} \geq t_{RC}(\text{min})$ $I_{OL} = 0 \text{ mA}$		460	mA	1
Precharge standby current in power-down mode	Icc2P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 15\text{ns}$		4	mA	
	Icc2PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$		4		
Precharge standby current in non power-down mode	Icc2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 15\text{ns}$ Input signals are changed one time during 30ns		60	mA	
	Icc2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable		28		
Active standby current in power-down mode	Icc3P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 15\text{ns}$		20	mA	
	Icc3PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$		20		
Active standby current in non power-down mode (One bank active)	Icc3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 15\text{ns}$ Input signals are changed one time during 30ns		120	mA	
	Icc3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable		80	mA	
Operating current (Burst mode)	Icc4	$I_{OL} = 0 \text{ mA}$ Page burst 2Banks activated $t_{CCD} = 2\text{CLKs}$	3	580	mA	1
			2	540		
Refresh current	Icc5	$t_{RC} \geq t_{RC}(\text{min})$		660	mA	2
Self refresh current	Icc6	$\text{CKE} \leq 0.2\text{V}$		3.2	mA	

Notes : 1. Measured with outputs open.

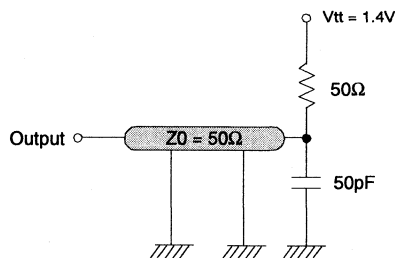
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	$t_{RRD}(\text{min})$	20	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	$t_{RCD}(\text{min})$	24	ns	1
Row precharge time	$t_{RP}(\text{min})$	24	ns	1
Row active time	$t_{RAS}(\text{min})$	50	ns	1
Row cycle time	$t_{RAS}(\text{max})$	100	us	
	$t_{RC}(\text{min})$	80	ns	1
Last data in to row precharge	$t_{RDL}(\text{min})$	12	ns	2
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\text{min})$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\text{min})$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1$ ns.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11, A0 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X	3		
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A0)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A0)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

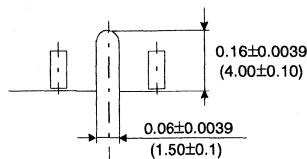
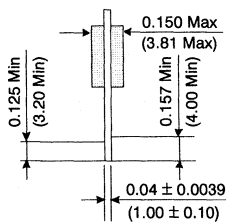
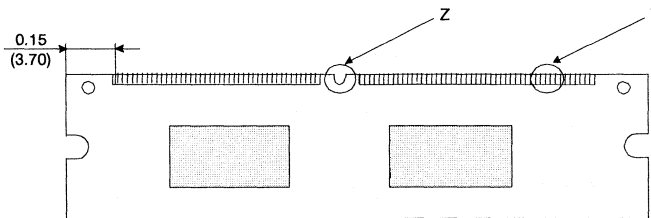
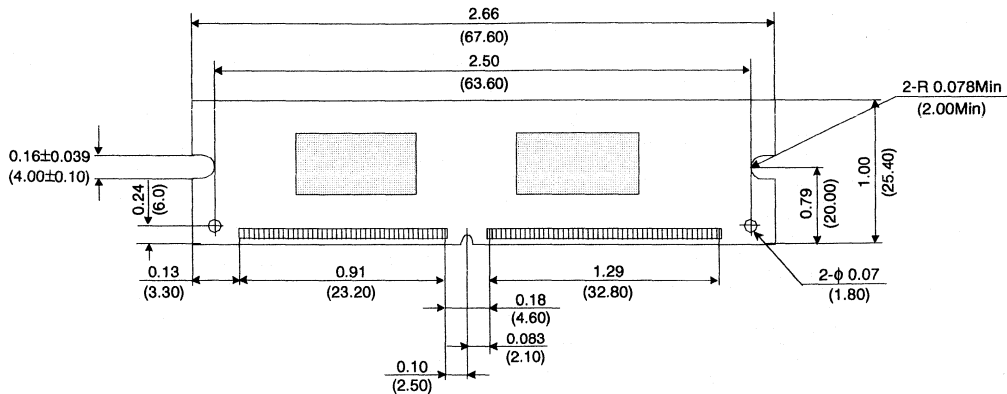
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

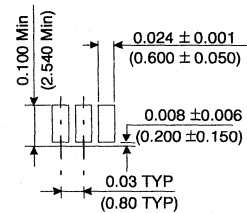
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances :±.005(.13) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
SDRAM Part No. : K4S281632M

M466S0924MT0-L10

- Organization : 8Mx64
- Composition : 8Mx16*4
- Used component part # : K4S281632M-TL10
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraon type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	F4h	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	 Manufacturer part # (Module depth)	9	39h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	M	4Dh	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L	4Ch	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	 Manufacturer revision code (For component)	M-die (1st Gen.)	4Dh	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S1723MT2 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S1723MT2 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S1723MT2 consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S1723MT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S1723MT2-L10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,150mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38					111	A10/AP	112	A11
19	DQ7	20	DQ39	61	CLK0	62	CKE0	113	VDD	114	VDD
21	Vss	22	Vss	63	VDD	64	VDD	115	DQM2	116	DQM6
23	DQM0	24	DQM4	65	RAS	66	CAS	117	DQM3	118	DQM7
25	DQM1	26	DQM5	67	WE	68	*CKE1	119	Vss	120	Vss
27	VDD	28	VDD	69	CS0	70	*A12	121	DQ24	122	DQ56
29	A0	30	A3	71	*CS1	72	*A13	123	DQ25	124	DQ57
31	A1	32	A4	73	DU	74	CLK1	125	DQ26	126	DQ58
33	A2	34	A5	75	Vss	76	Vss	127	DQ27	128	DQ59
35	Vss	36	Vss	77	NC	78	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	79	NC	80	NC	131	DQ28	132	DQ60
39	DQ9	40	DQ41	81	VDD	82	VDD	133	DQ29	134	DQ61
41	DQ10	42	DQ42	83	DQ16	84	DQ48	135	DQ30	136	DQ62
43	DQ11	44	DQ43	85	DQ17	86	DQ49	137	DQ31	138	DQ63
45	VDD	46	VDD	87	DQ18	88	DQ50	139	Vss	140	Vss
47	DQ12	48	DQ44	89	DQ19	90	DQ51	141	**SDA	142	**SCL
49	DQ13	50	DQ45	91	Vss	92	Vss	143	VDD	144	VDD
				93	DQ20	94	DQ52				

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

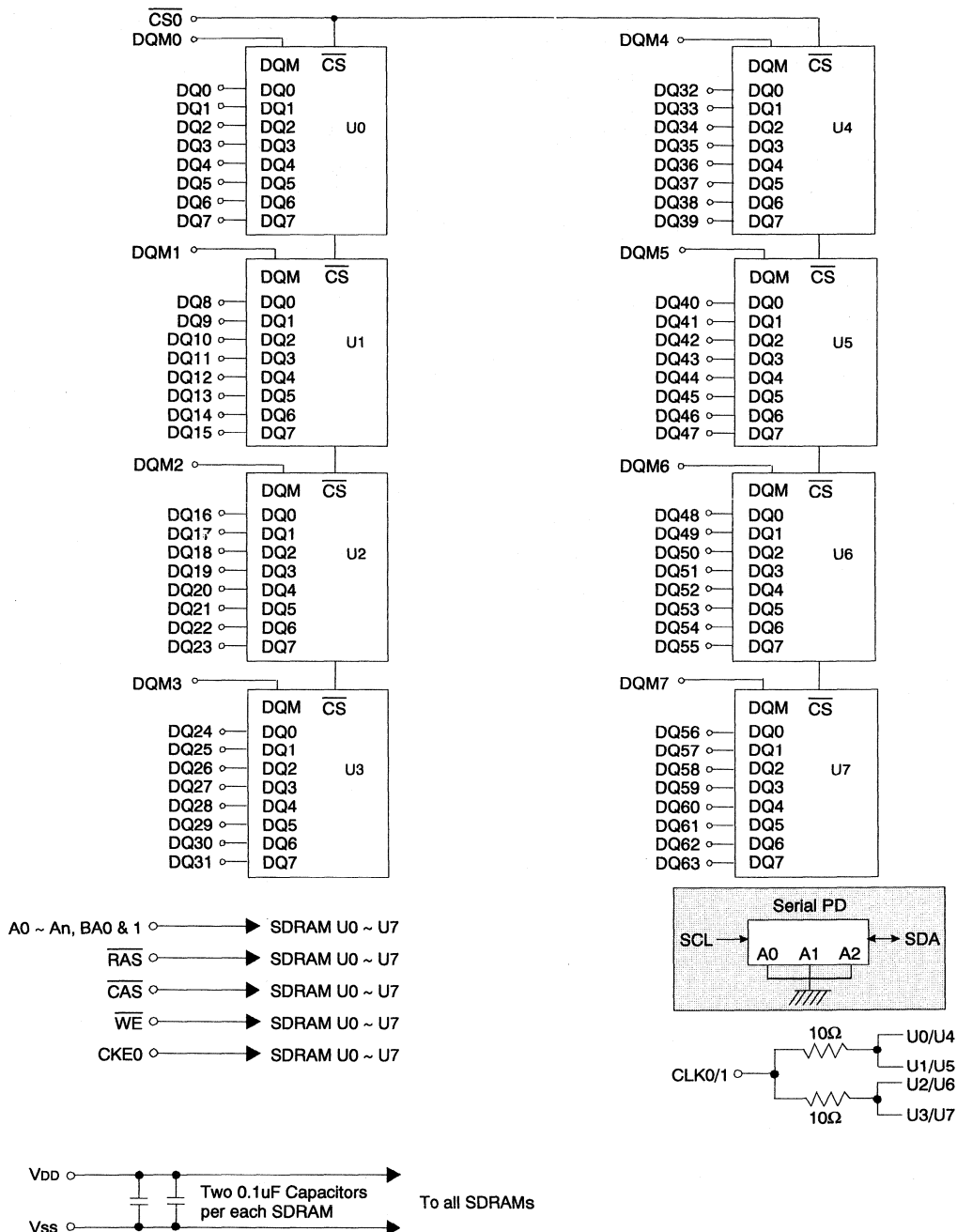
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output HI-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (I _{inputs})	I _{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	40	60	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	40	60	pF
Input capacitance (CKE ₀)	C _{IN3}	35	55	pF
Input capacitance (CLK ₀ ~ CLK ₁)	C _{IN4}	25	35	pF
Input capacitance ($\overline{\text{CS}}$ ₀)	C _{IN5}	35	55	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	5	15	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	5	15	pF

DC CHARACTERISTICS(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

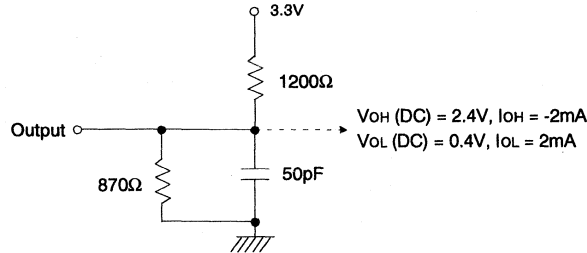
Parameter	Symbol	Test Condition	CAS Latency	Version	Unit	Note
				-10		
Operating current (One bank active)	Icc1	Burst length = 1 $\text{trc} \geq \text{trc}(\text{min})$ $\text{IOL} = 0 \text{ mA}$		840	mA	1
Precharge standby current in power-down mode	Icc2P	$\text{CKE} \leq V_{IL}(\text{max})$, $\text{tcc} = 15\text{ns}$		8	mA	
	Icc2PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$		8		
Precharge standby current in non power-down mode	Icc2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $\text{tcc} = 15\text{ns}$ Input signals are changed one time during 30ns		120	mA	
	Icc2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable		56		
Active standby current in power-down mode	Icc3P	$\text{CKE} \leq V_{IL}(\text{max})$, $\text{tcc} = 15\text{ns}$		40	mA	
	Icc3PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$		40		
Active standby current in non power-down mode (One bank active)	Icc3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $\text{tcc} = 15\text{ns}$ Input signals are changed one time during 30ns		240	mA	
	Icc3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable		160	mA	
Operating current (Burst mode)	Icc4	$\text{IOL} = 0 \text{ mA}$ Page burst 2Banks activated $\text{tCCD} = 2\text{CLKs}$	3	1,000	mA	1
			2	920		
Refresh current	Icc5	$\text{trc} \geq \text{trc}(\text{min})$		1,320	mA	2
Self refresh current	Icc6	$\text{CKE} \leq 0.2\text{V}$		6.4	mA	

Notes : 1. Measured with outputs open.

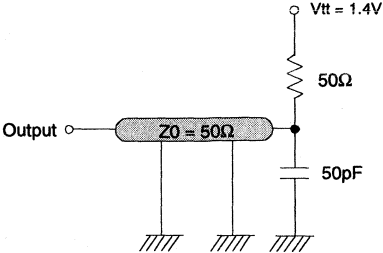
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (V _{Ih} /V _{Il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	tRRD (min)	20	ns	1
RAS to CAS delay	tRCD (min)	24	ns	1
Row precharge time	tRP (min)	24	ns	1
Row active time	tRAS (min)	50	ns	1
	tRAS (max)	100	us	
Row cycle time	tRC (min)	80	ns	1
Last data in to row precharge	tRDL (min)	12	ns	2
Last data in to new col. address delay	tCDL (min)	1	CLK	2
Last data in to burst stop	tBDL (min)	1	CLK	2
Col. address to col. address delay	tCCD (min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

- Notes :**
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(t_r \& t_f) = 1$ ns.If $t_r \& t_f$ is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	X	X		3		
											H	X	X
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto Precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto Precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

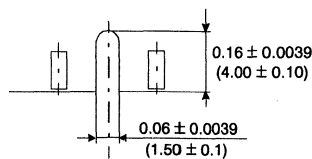
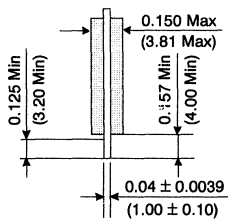
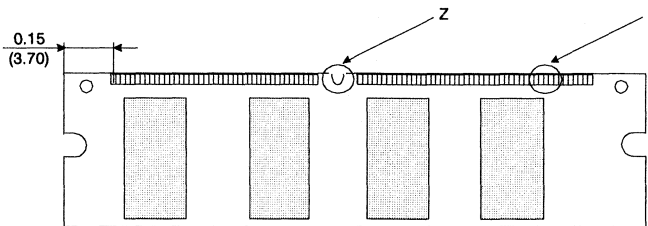
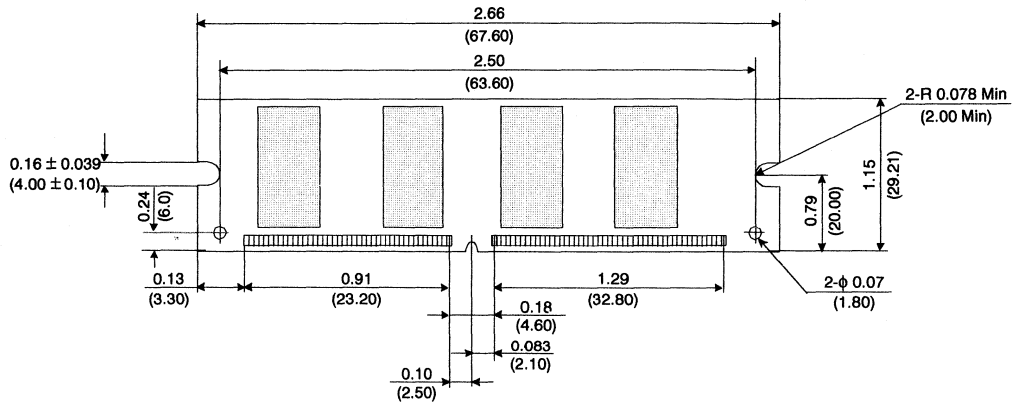
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

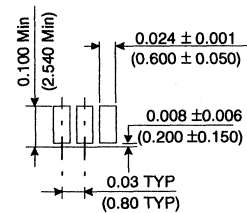
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832M

M466S1723MT2-L10

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832M-TL10
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 128MB	20h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FDh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	M	4Dh	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L	4Ch	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	 Manufacturer revision code (For component)	M-die (1st Gen.)	4Dh	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S1723MT3 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S1723MT3 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S1723MT3 consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S1723MT3 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S1723MT3-L10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,050mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

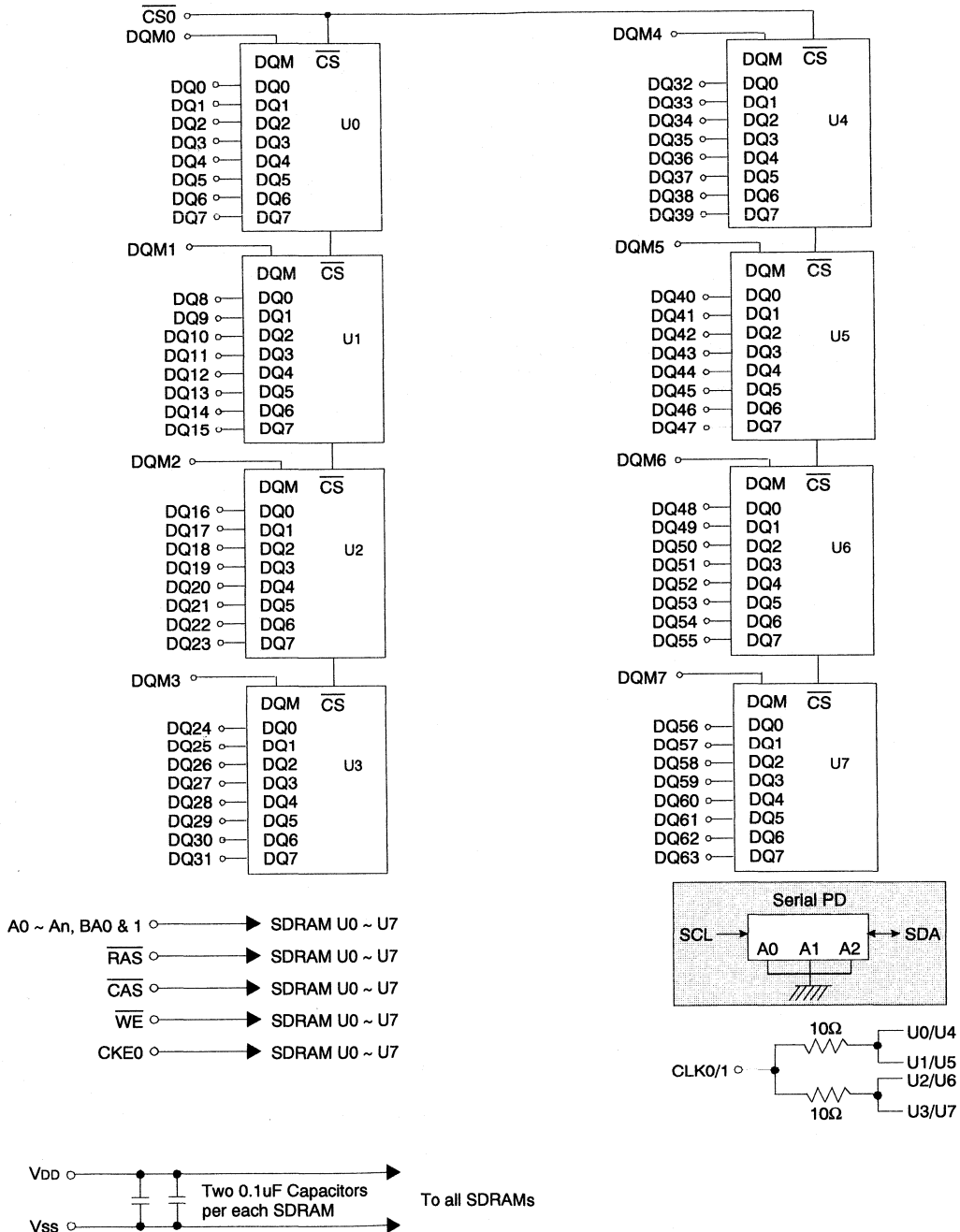
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	40	60	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	40	60	pF
Input capacitance (CKE ₀)	C _{IN3}	35	55	pF
Input capacitance (CLK ₀ ~ CLK ₁)	C _{IN4}	25	35	pF
Input capacitance ($\overline{\text{CS}}$)	C _{IN5}	35	55	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	5	15	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	5	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

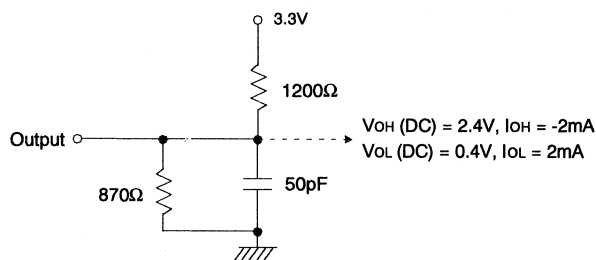
Parameter	Symbol	Test Condition	CAS Latency	Version	Unit	Note
				-10		
Operating current (One bank active)	ICC1	Burst length = 1 $\text{trc} \geq \text{trc}(\text{min})$ $\text{IOL} = 0 \text{ mA}$		540	mA	1
Precharge standby current in power-down mode	ICC2P	$\text{CKE} \leq \text{VIL}(\text{max})$, $\text{tcc} = 15\text{ns}$		8	mA	
	ICC2PS	$\text{CKE} \ \& \ \text{CLK} \leq \text{VIL}(\text{max})$, $\text{tcc} = \infty$		8		
Precharge standby current in non power-down mode	ICC2N	$\text{CKE} \geq \text{VIH}(\text{min})$, $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, $\text{tcc} = 15\text{ns}$ Input signals are changed one time during 30ns		120	mA	
	ICC2NS	$\text{CKE} \geq \text{VIH}(\text{min})$, $\text{CLK} \leq \text{VIL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable		56		
Active standby current in power-down mode	ICC3P	$\text{CKE} \leq \text{VIL}(\text{max})$, $\text{tcc} = 15\text{ns}$		40	mA	
	ICC3PS	$\text{CKE} \ \& \ \text{CLK} \leq \text{VIL}(\text{max})$, $\text{tcc} = \infty$		40		
Active standby current in non power-down mode (One bank active)	ICC3N	$\text{CKE} \geq \text{VIH}(\text{min})$, $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, $\text{tcc} = 15\text{ns}$ Input signals are changed one time during 30ns		240	mA	
	ICC3NS	$\text{CKE} \geq \text{VIH}(\text{min})$, $\text{CLK} \leq \text{VIL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable		160	mA	
Operating current (Burst mode)	ICC4	$\text{IOL} = 0 \text{ mA}$ Page burst 2Banks activated $\text{tCCD} = 2\text{CLKs}$	3	620	mA	1
			2	580		
Refresh current	ICC5	$\text{trc} \geq \text{trc}(\text{min})$		1,320	mA	2
Self refresh current	ICC6	$\text{CKE} \leq 0.2\text{V}$		6.4	mA	

Notes : 1. Measured with outputs open.

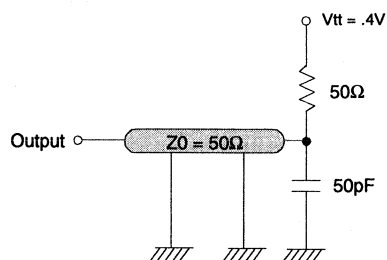
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	$t_{RRD}(\min)$	20	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	24	ns	1
Row precharge time	$t_{RP}(\min)$	24	ns	1
Row active time	$t_{RAS}(\min)$	50	ns	1
	$t_{RAS}(\max)$	100	us	
Row cycle time	$t_{RC}(\min)$	80	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	12	ns	2
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tsac		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	toH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tss	2.5		ns	3
Input hold time		tSH	1,5		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tshZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(t_r \text{ \& } t_f) = 1$ ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	L		3									
		Exit	L	H	L	H	H	H	X	X			3
													H
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X	X			
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

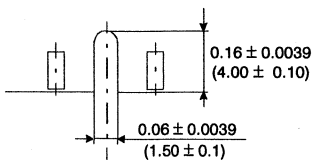
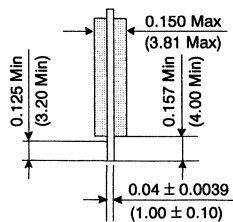
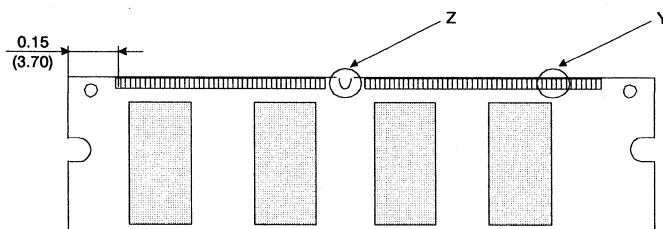
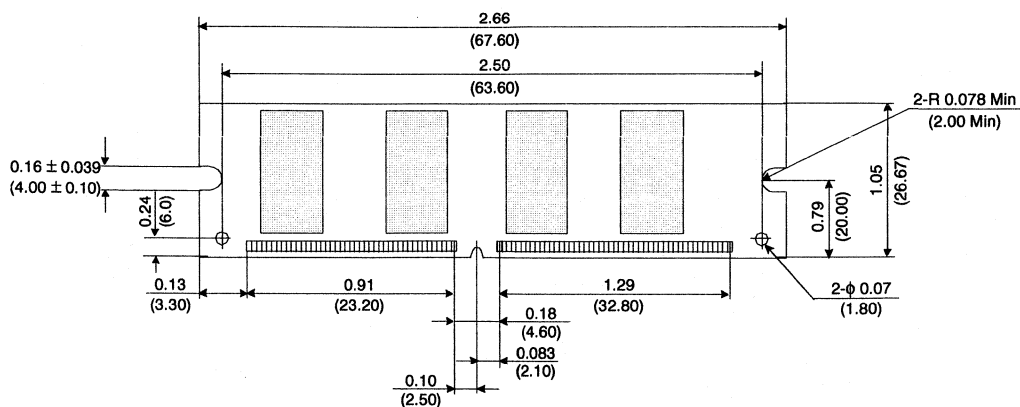
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

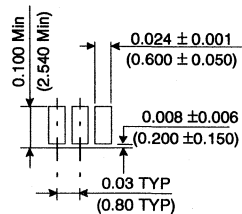
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ±0.005(.13) unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832M

M466S1723MT3-L10

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832M-TL10
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,050mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 128MB	20h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FDh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	M	4Dh	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	3	33h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L	4Ch	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	3	33h	
92	 Manufacturer revision code (For component)	M-die (1st Gen.)	4Dh	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S1724MT2 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S1724MT2 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S1724MT2 consists of eight CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S1724MT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S1724MT2-L10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,150mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS1	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

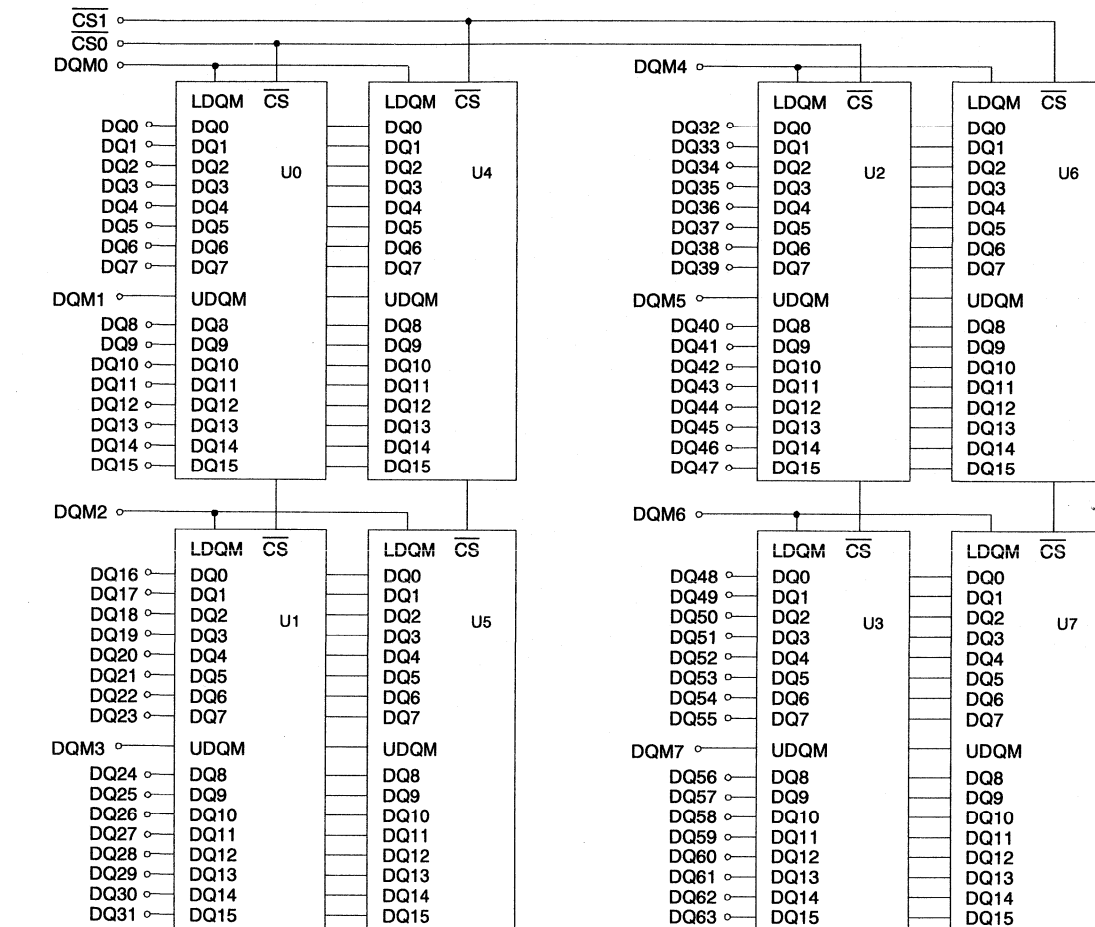
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

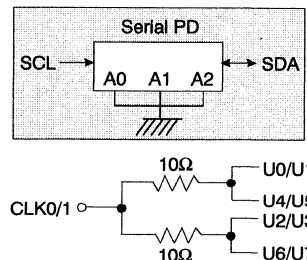
Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



A0 ~ An, BA0 & 1 → SDRAM U0 ~ U7
 $\overline{\text{RAS}}$ → SDRAM U0 ~ U7
 $\overline{\text{CAS}}$ → SDRAM U0 ~ U7
 $\overline{\text{WE}}$ → SDRAM U0 ~ U7
 CKE0 → SDRAM U0 ~ U3
 CKE1 → SDRAM U4 ~ U7

VDD → Two 0.1uF Capacitors → To all SDRAMs
 VSS →



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-8	-	8	µA	3
Input leakage current (I/O pins)	I _{IL}	-3	-	3	µA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	40	60	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	40	60	pF
Input capacitance (CKE ₀ ~ CKE ₁)	C _{IN3}	25	35	pF
Input capacitance (CLK ₀ ~ CLK ₁)	C _{IN4}	25	35	pF
Input capacitance (CS ₀ ~ CS ₁)	C _{IN5}	25	35	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	15	25	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	5	15	pF

DC CHARACTERISTICS

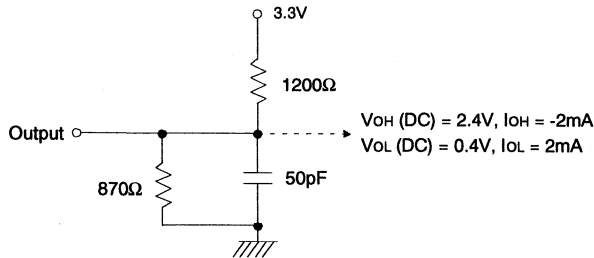
(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version	Unit	Note
				-10		
Operating current (One bank active)	ICC1	Burst length = 1 $\text{trc} \geq \text{trc}(\text{min})$ $\text{IOL} = 0 \text{ mA}$		580	mA	1
Precharge standby current in power-down mode	ICC2P	$\text{CKE} \leq \text{VIL}(\text{max})$, $\text{tcc} = 15\text{ns}$		8	mA	
	ICC2PS	$\text{CKE} \& \text{CLK} \leq \text{VIL}(\text{max})$, $\text{tcc} = \infty$		8		
Precharge standby current in non power-down mode	ICC2N	$\text{CKE} \geq \text{VIH}(\text{min})$, $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, $\text{tcc} = 15\text{ns}$ Input signals are changed one time during 30ns		120	mA	
	ICC2NS	$\text{CKE} \geq \text{VIH}(\text{min})$, $\text{CLK} \leq \text{VIL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable		56		
Active standby current in power-down mode	ICC3P	$\text{CKE} \leq \text{VIL}(\text{max})$, $\text{tcc} = 15\text{ns}$		40	mA	
	ICC3PS	$\text{CKE} \& \text{CLK} \leq \text{VIL}(\text{max})$, $\text{tcc} = \infty$		40		
Active standby current in non power-down mode (One bank active)	ICC3N	$\text{CKE} \geq \text{VIH}(\text{min})$, $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, $\text{tcc} = 15\text{ns}$ Input signals are changed one time during 30ns		240	mA	
	ICC3NS	$\text{CKE} \geq \text{VIH}(\text{min})$, $\text{CLK} \leq \text{VIL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable		160	mA	
Operating current (Burst mode)	ICC4	$\text{IOL} = 0 \text{ mA}$ Page burst 2 Banks activated $\text{tCCD} = 2\text{CLKs}$	3	700	mA	1
			2	660		
Refresh current	ICC5	$\text{trc} \geq \text{trc}(\text{min})$		1,320	mA	2
Self refresh current	ICC6	$\text{CKE} \leq 0.2\text{V}$		6.4	mA	

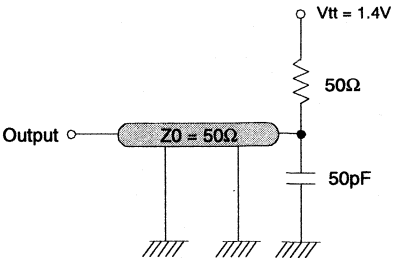
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	tRRD(min)	20	ns	1
RAS to CAS delay	tRCD(min)	24	ns	1
Row precharge time	tRP(min)	24	ns	1
Row active time	tRAS(min)	50	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	80	ns	1
Last data in to row precharge	tRDL(min)	12	ns	2
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

- Notes :** 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tsac		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	toH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tss	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
 If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
 i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

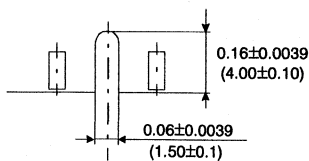
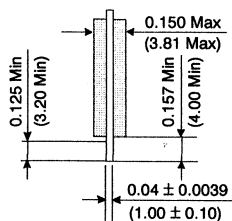
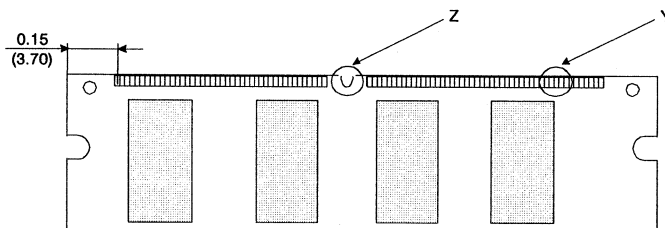
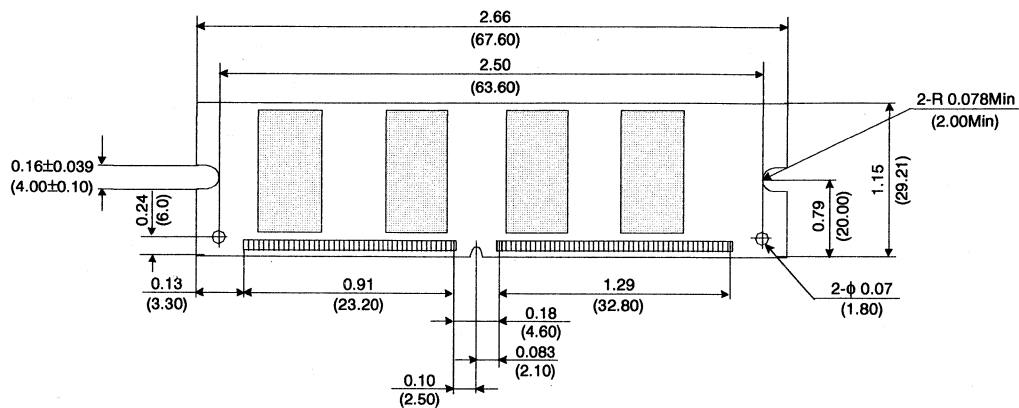
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

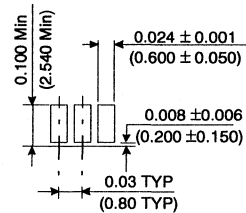
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ±0.005(.13) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
SDRAM Part No. : K4S281632M

M466S1724MT2-L10

- Organization : 16Mx64
- Composition : 8Mx16 *8
- Used component part # : K4S281632M-TL10
- # of banks in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=TRP)	24ns	18h	
28	Minimum row active to row active delay (TRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=TRCD)	24ns	18h	
30	Minimum activate precharge time (=TRAS)	50ns	32h	
31	Module Row density	2 Rows of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	F5h	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	M	4Dh	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L	4Ch	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	 Manufacturer revision code (For component)	M-die (1st Gen.)	4Dh	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S1723AT2 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S1723AT2 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S1723AT2 consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S1723AT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S1723AT2-L10/C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,150mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

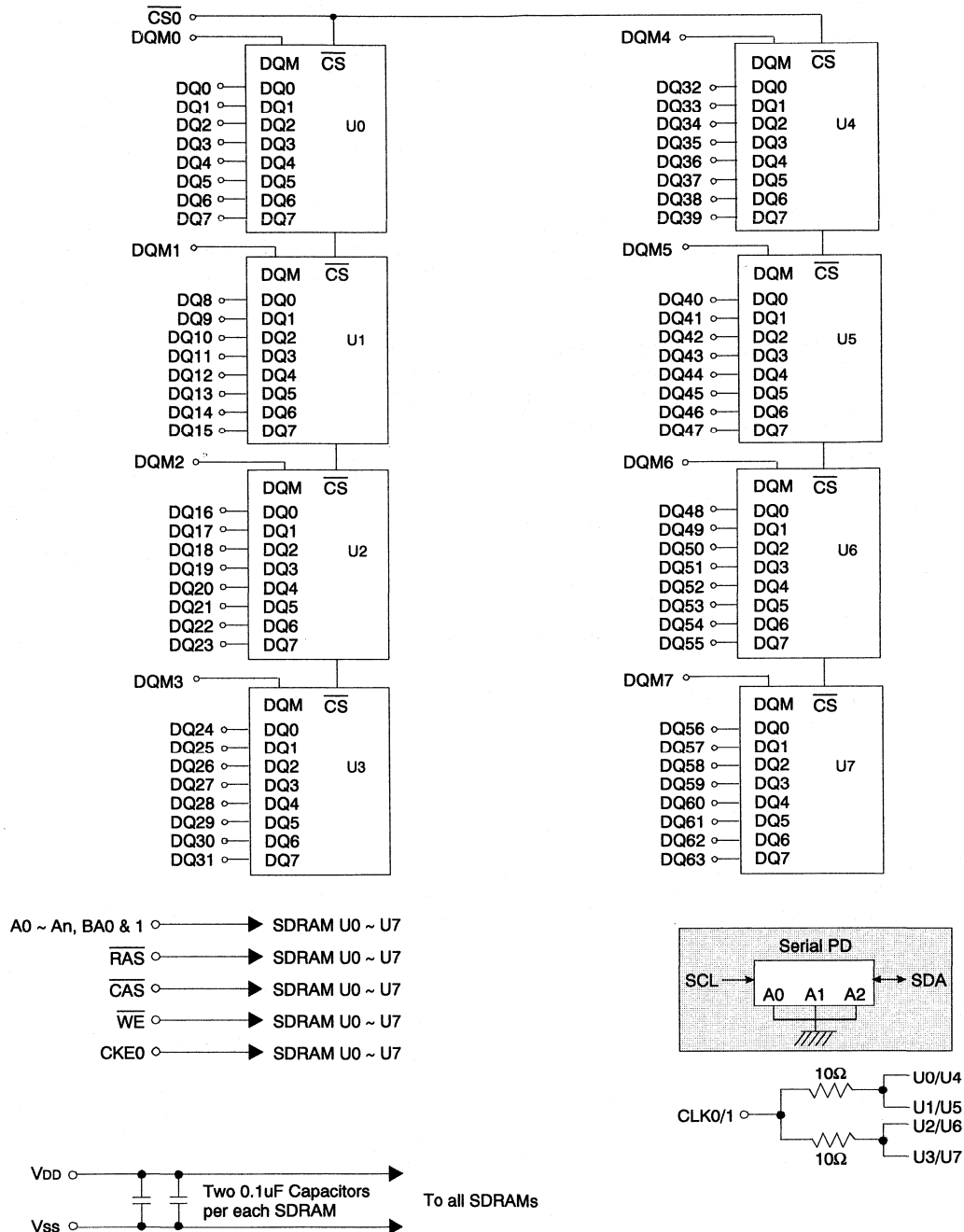
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	25	45	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	25	45	pF
Input capacitance (CKE0)	C _{IN3}	25	45	pF
Input capacitance (CLK0 ~ CLK1)	C _{IN4}	15	21	pF
Input capacitance ($\overline{\text{CS0}}$)	C _{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	8	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	I _{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}(\text{min})$ $I_O = 0 \text{ mA}$	880	mA	1
Precharge standby current in power-down mode	I _{CC2P}	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	8	mA	
	I _{CC2PS}	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	8		
Precharge standby current in non power-down mode	I _{CC2N}	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	160	mA	
	I _{CC2NS}	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	56		
Active standby current in power-down mode	I _{CC3P}	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	40	mA	
	I _{CC3PS}	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	40		
Active standby current in non power-down mode (One bank active)	I _{CC3N}	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	240	mA	
	I _{CC3NS}	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	160	mA	
Operating current (Burst mode)	I _{CC4}	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	1,000	mA	1
Refresh current	I _{CC5}	$t_{RC} \geq t_{RC}(\text{min})$	1,680	mA	2
Self refresh current	I _{CC6}	$\text{CKE} \leq 0.2\text{V}$	C	12	mA
			L	6.4	mA

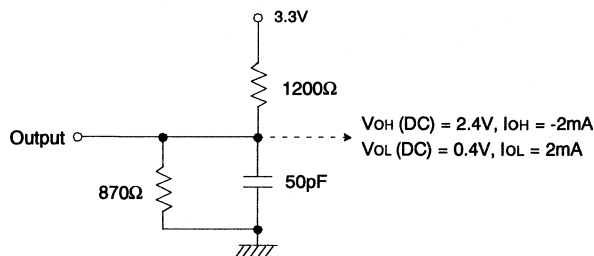
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

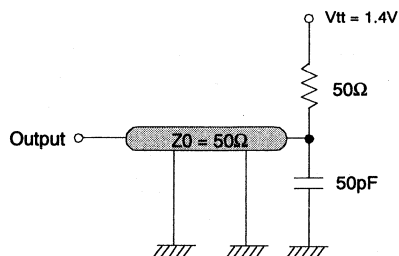
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	$t_{RRD}(\min)$	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	$t_{RCD}(\min)$	24	ns	1
Row precharge time	$t_{RP}(\min)$	24	ns	1
Row active time	$t_{RAS}(\min)$	50	ns	1
Row cycle time	$t_{RAS}(\max)$	100	us	
	$t_{RC}(\min)$	80	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2,5
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20ns	-	5
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -10, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .

SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tsAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	toH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tss	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

- Notes :
- 1. Parameters depend on programmed CAS latency.
 - 2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
 - 3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto Precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto Precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

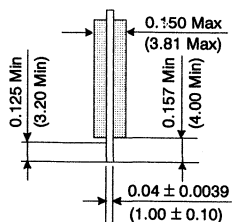
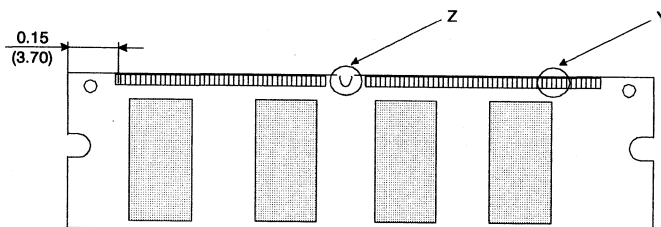
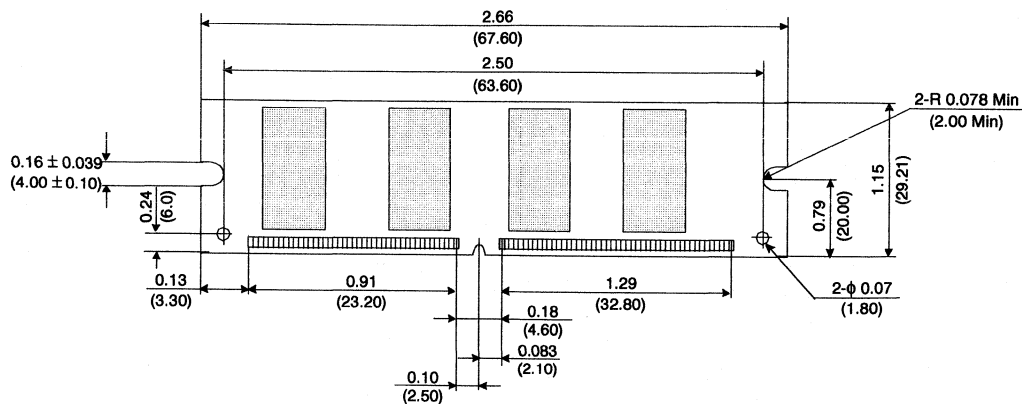
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

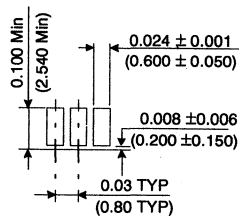
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
 SDRAM Part No. : K4S280832A

M466S1723AT2-L10, C10

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832A-TL10, C10
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 128MB	20h	
32-61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FDh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S1723AT3 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S1723AT3 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S1723AT3 consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S1723AT3 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S1723AT3-L10 /C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,050mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

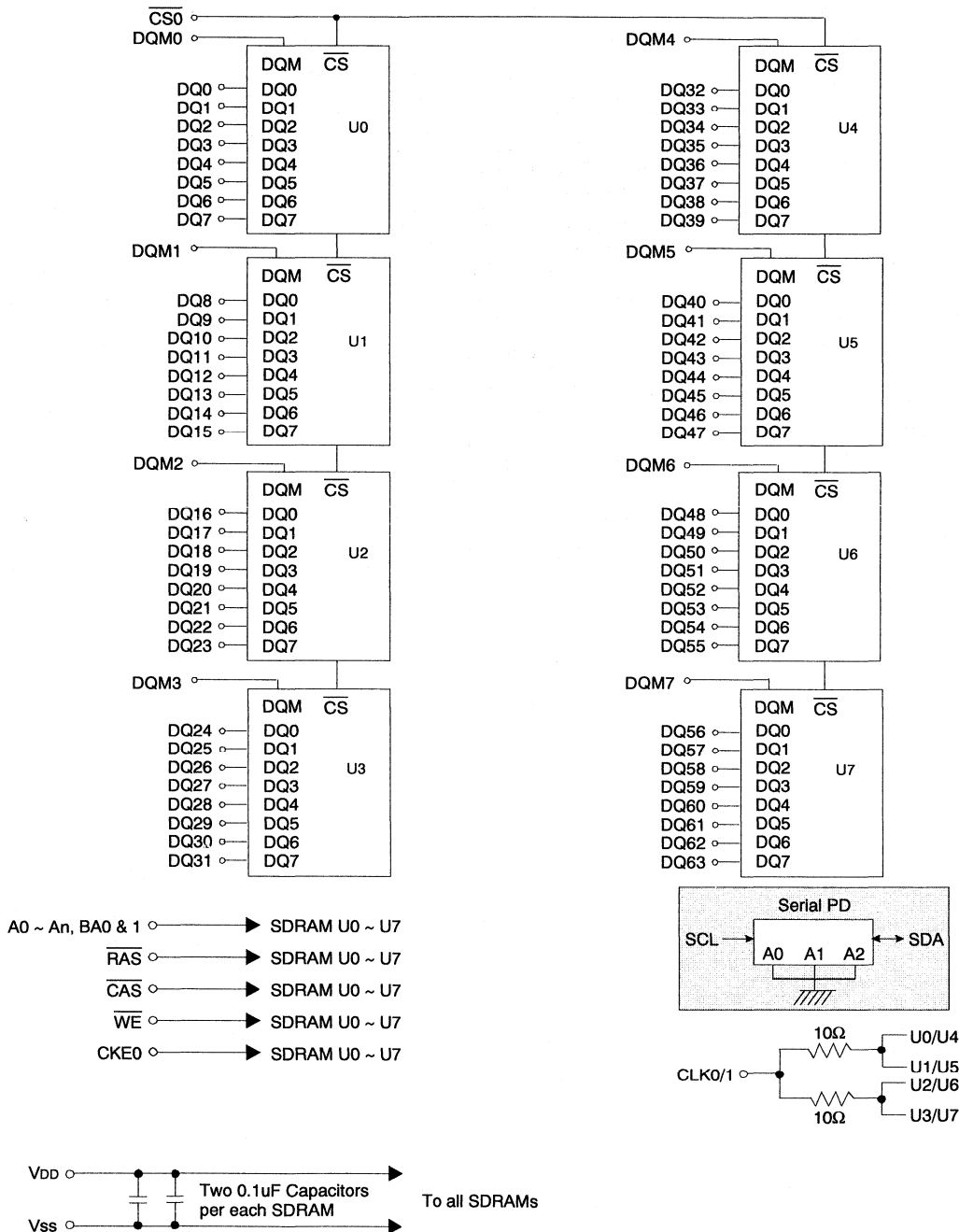
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{CS}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	25	45	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	25	45	pF
Input capacitance (CKE ₀)	C _{IN3}	25	45	pF
Input capacitance (CLK ₀ ~ CLK ₁)	C _{IN4}	15	21	pF
Input capacitance (CS ₀)	C _{IN5}	15	25	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	8	12	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\min)$ $I_O = 0 \text{ mA}$	880	mA	1
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	8	mA	
	ICC2PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	8		
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	160	mA	
	ICC2NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	56		
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	40	mA	
	ICC3PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	40		
Active standby current in non power-down mode (One bank active)	ICC3N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	240	mA	
	ICC3NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	160	mA	
Operating current (Burst mode)	ICC4	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2CLKs$	1,000	mA	1
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\min)$	1,680	mA	2
Self refresh current	ICC6	$CKE \leq 0.2V$	C	12	mA
			L	6.4	mA

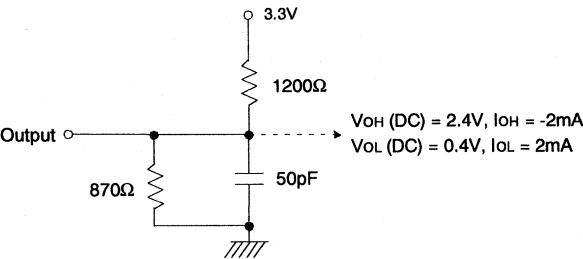
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

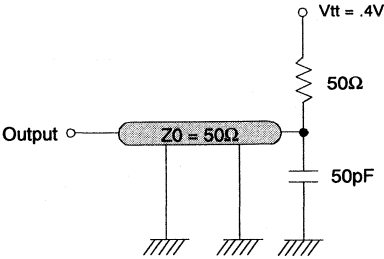
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (V _{ih} /V _{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	tRRD(min)	20	ns	1
RAS to CAS delay	tRCD(min)	24	ns	1
Row precharge time	tRP(min)	24	ns	1
Row active time	tRAS(min)	50	ns	1
Row cycle time	tRAS(max)	100	us	
	tRC(min)	80	ns	1
Last data in to row precharge	tRDL(min)	2	CLK	2,5
Last data in to Active delay	tDAL(min)	2 CLK + 20ns	-	5
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

- Notes :
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.
 - 5. For -10, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tsac		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	toH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tss	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1$ ns.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

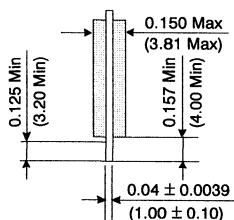
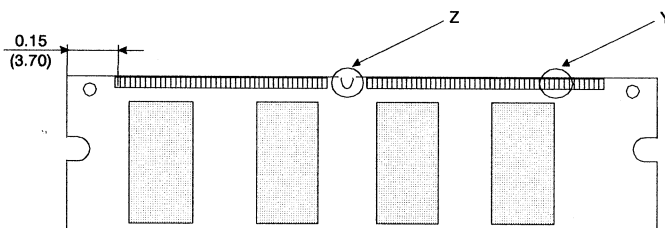
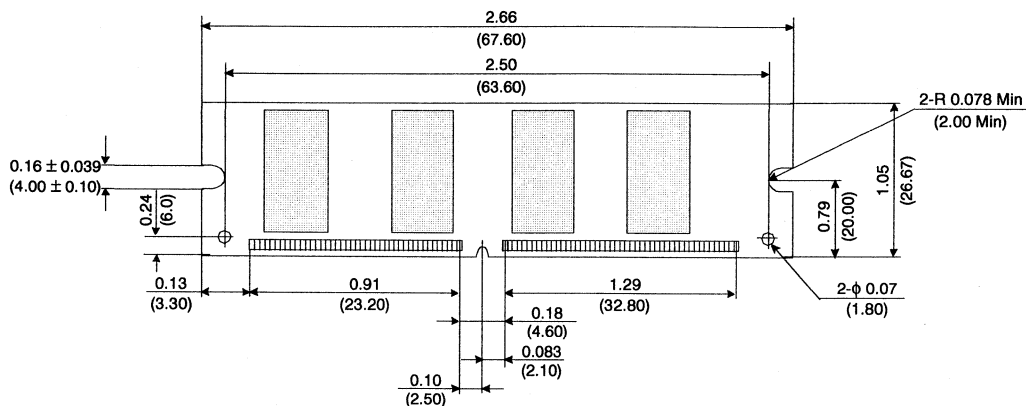
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

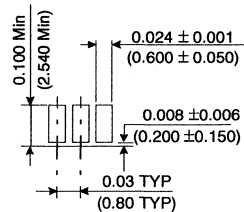
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ±0.005(.13) unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832A

M466S1723AT3-L10, C10

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832A-TL10, C10
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,050mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 128MB	20h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FDh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	3	33h	
86	Manufacturer part # (Hyphen)	" _ "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	3	33h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S0924BT0 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S0924BT0 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0924BT0 consists of four CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0924BT0 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S0924BT0-L10/C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,000mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

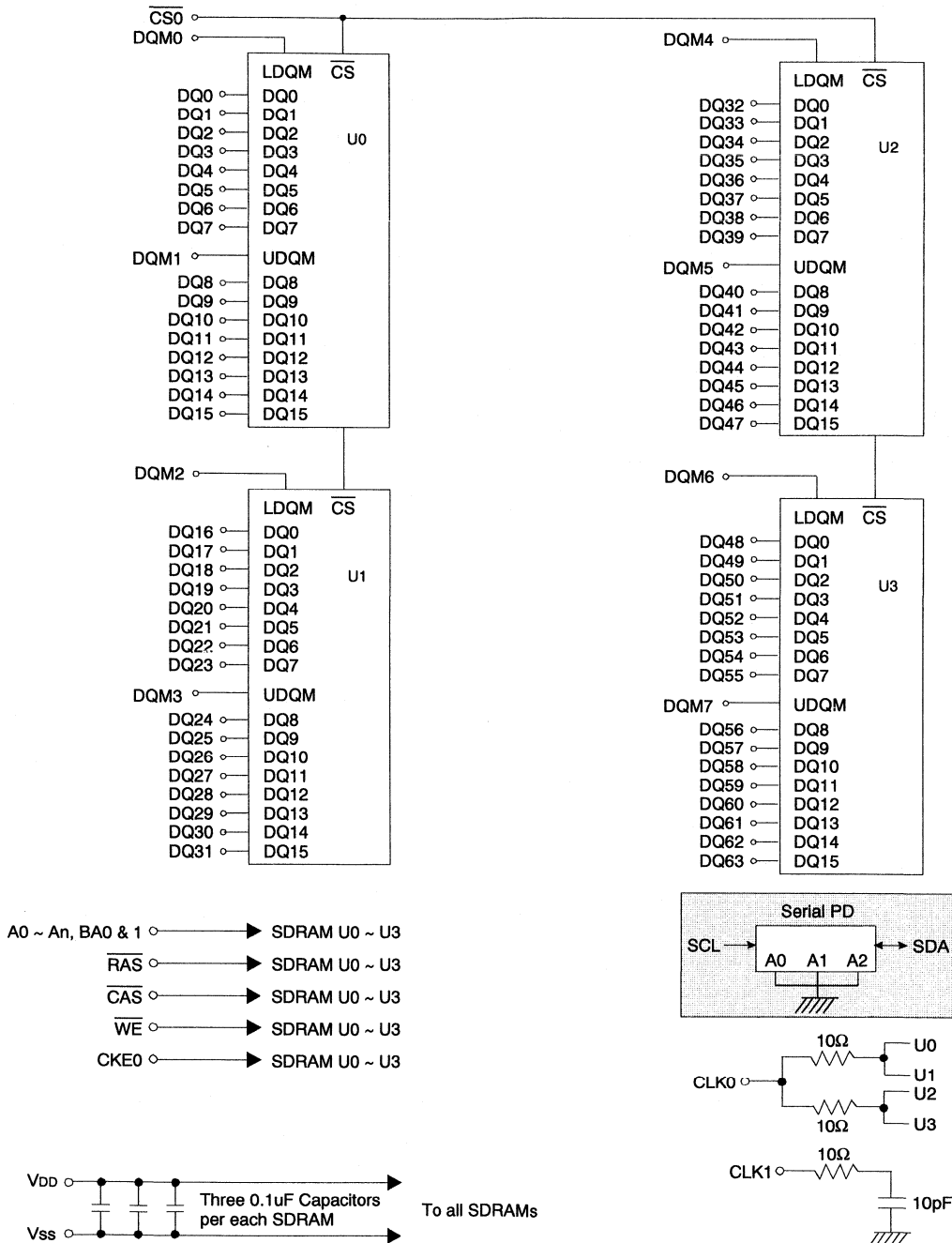
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	4	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	15	25	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	15	25	pF
Input capacitance (CKE0)	C _{IN3}	15	25	pF
Input capacitance (CLK0)	C _{IN4}	15	21	pF
Input capacitance (CS0)	C _{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	10	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	10	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	ICC1	Burst length = 1 $\text{trc} \geq \text{trc}(\text{min})$ $I_O = 0 \text{ mA}$	560	mA	1
Precharge standby current in power-down mode	ICC2P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	4	mA	
	ICC2PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	4		
Precharge standby current in non power-down mode	ICC2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	80	mA	
	ICC2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	28		
Active standby current in power-down mode	ICC3P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	20	mA	
	ICC3PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	20		
Active standby current in non power-down mode (One bank active)	ICC3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	120	mA	
	ICC3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	80	mA	
Operating current (Burst mode)	ICC4	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	580	mA	1
Refresh current	ICC5	$\text{trc} \geq \text{trc}(\text{min})$	840	mA	2
Self refresh current	ICC6	$\text{CKE} \leq 0.2V$	C	6	mA
			L	3.2	mA

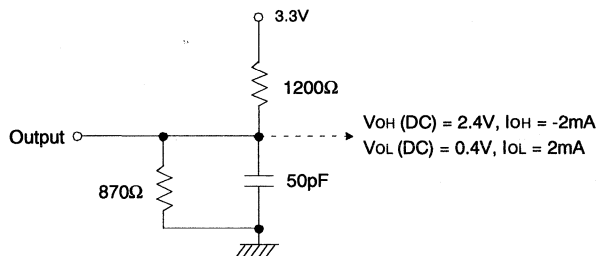
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

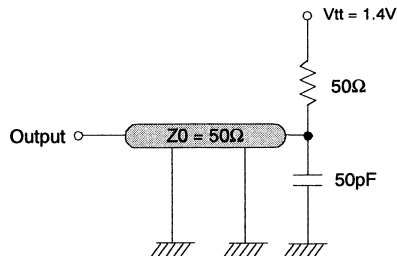
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	$t_{RRD}(\min)$	20	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	24	ns	1
Row precharge time	$t_{RP}(\min)$	24	ns	1
Row active time	$t_{RAS}(\min)$	50	ns	1
Row cycle time	$t_{RAS}(\max)$	100	us	
	$t_{RC}(\min)$	80	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2,5
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20ns	-	5
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -10, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .
SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tsac		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	toH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tch	3.5		ns	3
CLK low pulse width		tcl	3.5		ns	3
Input setup time		tss	2.5		ns	3
Input hold time		tsh	1.5		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tshZ		7	ns	
	CAS latency=2			7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
 If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
 i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Exit	L	H	X	X	X	X	X	X			
					X	X	X	X					
		Entry	H	L	H	X	X	X	X				
					L	H	H	H					
Exit		L	H	H	X	X	X	X					
				L	V	V	V						
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

Notes : 1. OP Code : Operand code

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

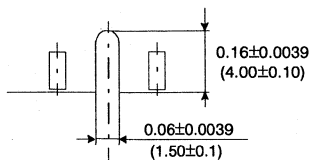
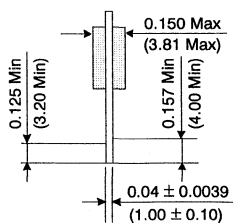
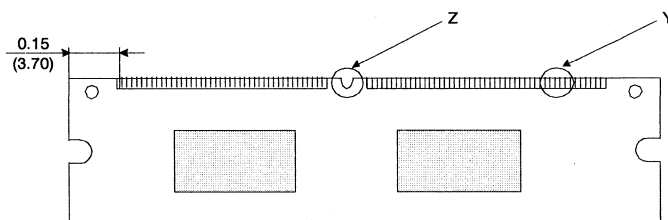
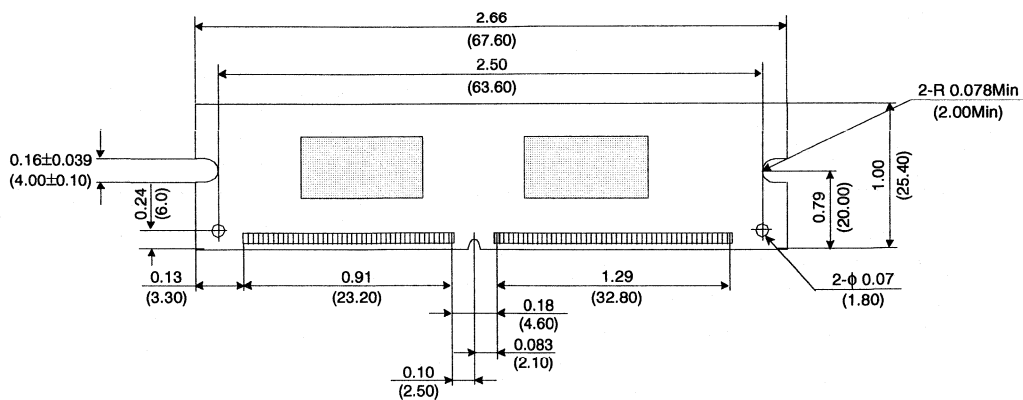
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

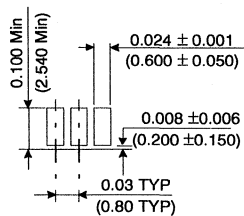
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ±0.005(.13) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
SDRAM Part No. : K4S281632B

M466S0924BT0-L10. C10

- Organization : 8Mx64
- Composition : 8Mx16*4
- Used component part # : K4S281632B-TL10, C10
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1 CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	F4h	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	 Manufacturer part # (Module depth)	9	39h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S1723BT2 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S1723BT2 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S1723BT2 consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S1723BT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S1723BT2-L10/C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,150mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38					111	A10/AP	112	A11
19	DQ7	20	DQ39	61	CLK0	62	CKE0	113	VDD	114	VDD
21	Vss	22	Vss	63	VDD	64	VDD	115	DQM2	116	DQM6
23	DQM0	24	DQM4	65	RAS	66	CAS	117	DQM3	118	DQM7
25	DQM1	26	DQM5	67	WE	68	*CKE1	119	Vss	120	Vss
27	VDD	28	VDD	69	CS0	70	*A12	121	DQ24	122	DQ56
29	A0	30	A3	71	*CS1	72	*A13	123	DQ25	124	DQ57
31	A1	32	A4	73	DU	74	CLK1	125	DQ26	126	DQ58
33	A2	34	A5	75	Vss	76	Vss	127	DQ27	128	DQ59
35	Vss	36	Vss	77	NC	78	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	79	NC	80	NC	131	DQ28	132	DQ60
39	DQ9	40	DQ41	81	VDD	82	VDD	133	DQ29	134	DQ61
41	DQ10	42	DQ42	83	DQ16	84	DQ48	135	DQ30	136	DQ62
43	DQ11	44	DQ43	85	DQ17	86	DQ49	137	DQ31	138	DQ63
45	VDD	46	VDD	87	DQ18	88	DQ50	139	Vss	140	Vss
47	DQ12	48	DQ44	89	DQ19	90	DQ51	141	**SDA	142	**SCL
49	DQ13	50	DQ45	91	Vss	92	Vss	143	VDD	144	VDD
				93	DQ20	94	DQ52				

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

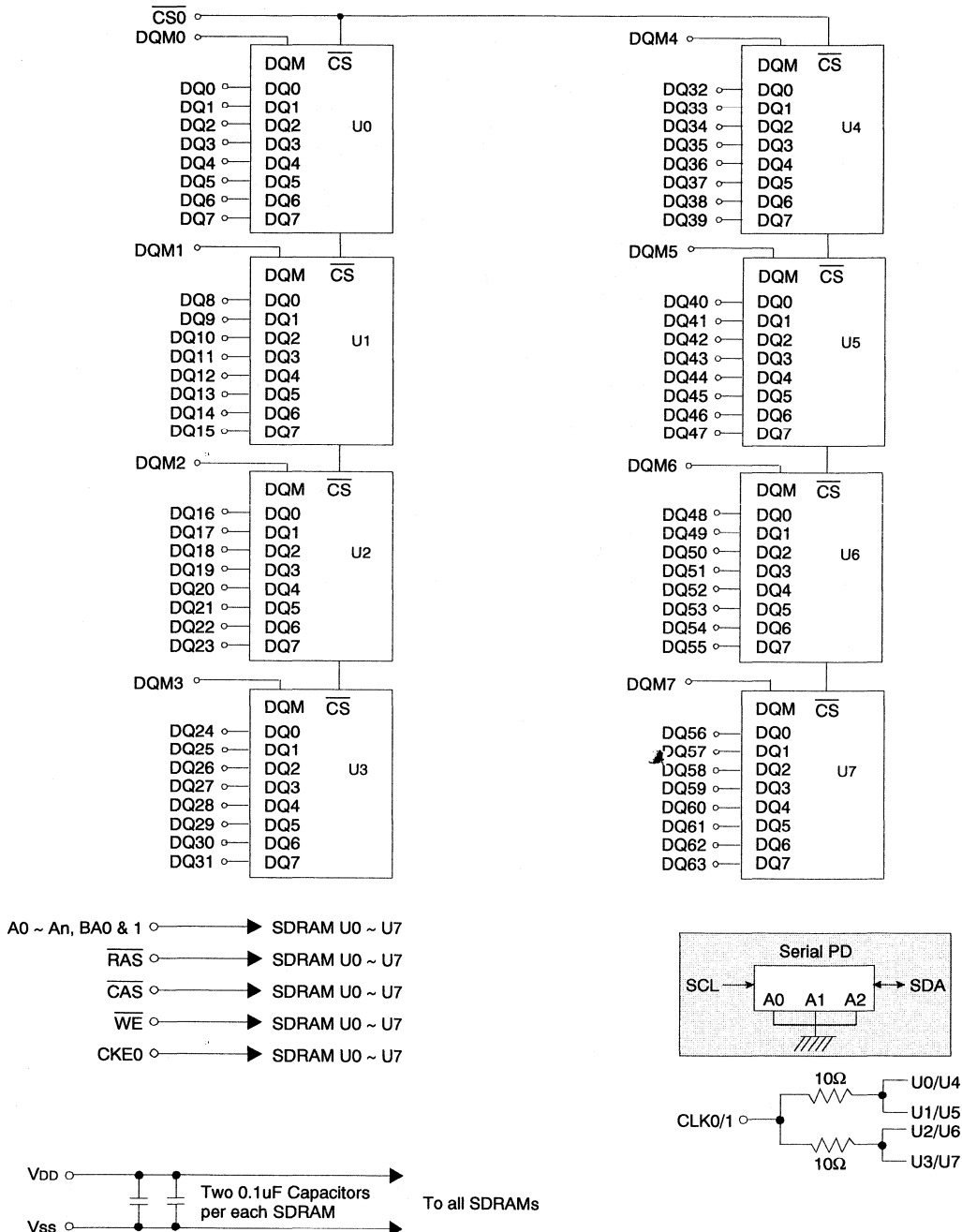
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	25	45	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	25	45	pF
Input capacitance (CKE ₀)	C _{IN3}	25	45	pF
Input capacitance (CLK ₀ ~ CLK ₁)	C _{IN4}	15	21	pF
Input capacitance (CS ₀)	C _{IN5}	15	25	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	8	12	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	880	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	8	mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	8		
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 10ns Input signals are changed one time during 20ns	160	mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	56		
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	40	mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	40		
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 10ns Input signals are changed one time during 20ns	240	mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	160	mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,000	mA	1
Refresh current	Icc5	trc ≥ trc(min)	1,680	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	C	12	mA
			L	6.4	mA

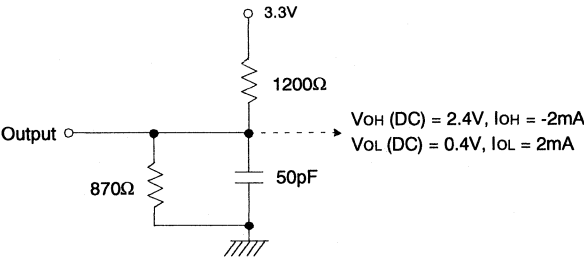
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

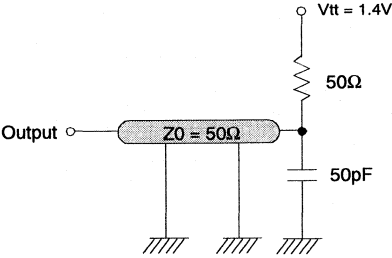
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (V _{ih} /V _{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	t _{RRD} (min)	20	ns	1
RAS to CAS delay	t _{RCD} (min)	24	ns	1
Row precharge time	t _{RP} (min)	24	ns	1
Row active time	t _{RAS} (min)	50	ns	1
Row cycle time	t _{RAS} (max)	100	us	
	t _{RC} (min)	80	ns	1
Last data in to row precharge	t _{RD} (min)	2	CLK	2,5
Last data in to Active delay	t _{DAL} (min)	2 CLK + 20ns	-	5
Last data in to new col. address delay	t _C DL(min)	1	CLK	2
Last data in to burst stop	t _B DL(min)	1	CLK	2
Col. address to col. address delay	t _{CCD} (min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

- Notes :** 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -10, t_{RD}L=1CLK and t_DAL=1CLK+20ns is also supported .
- SAMSUNG recommends t_{RD}L=2CLK and t_DAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tsac		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	toH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
 If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
 i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto Precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto Precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

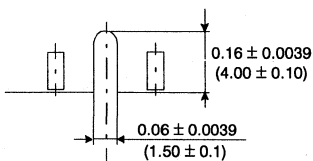
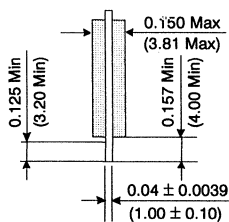
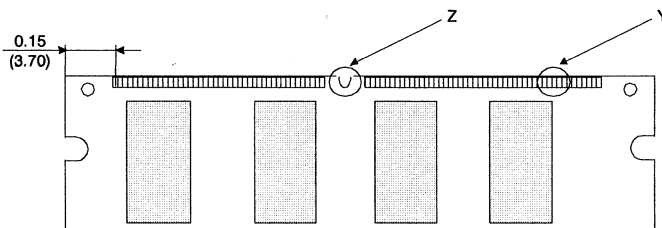
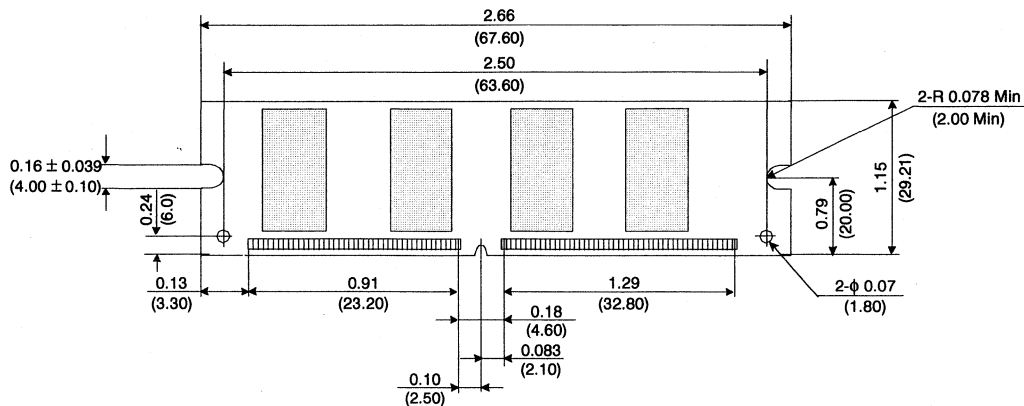
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

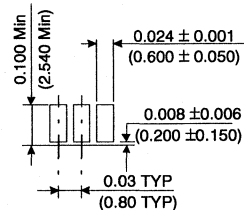
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832B

M466S1723BT2-L10, C10

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832B-TL10, C10
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 128MB	20h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FDh	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S1723BT3 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S1723BT3 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S1723BT3 consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S1723BT3 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S1723BT3-L10 /C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,050mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

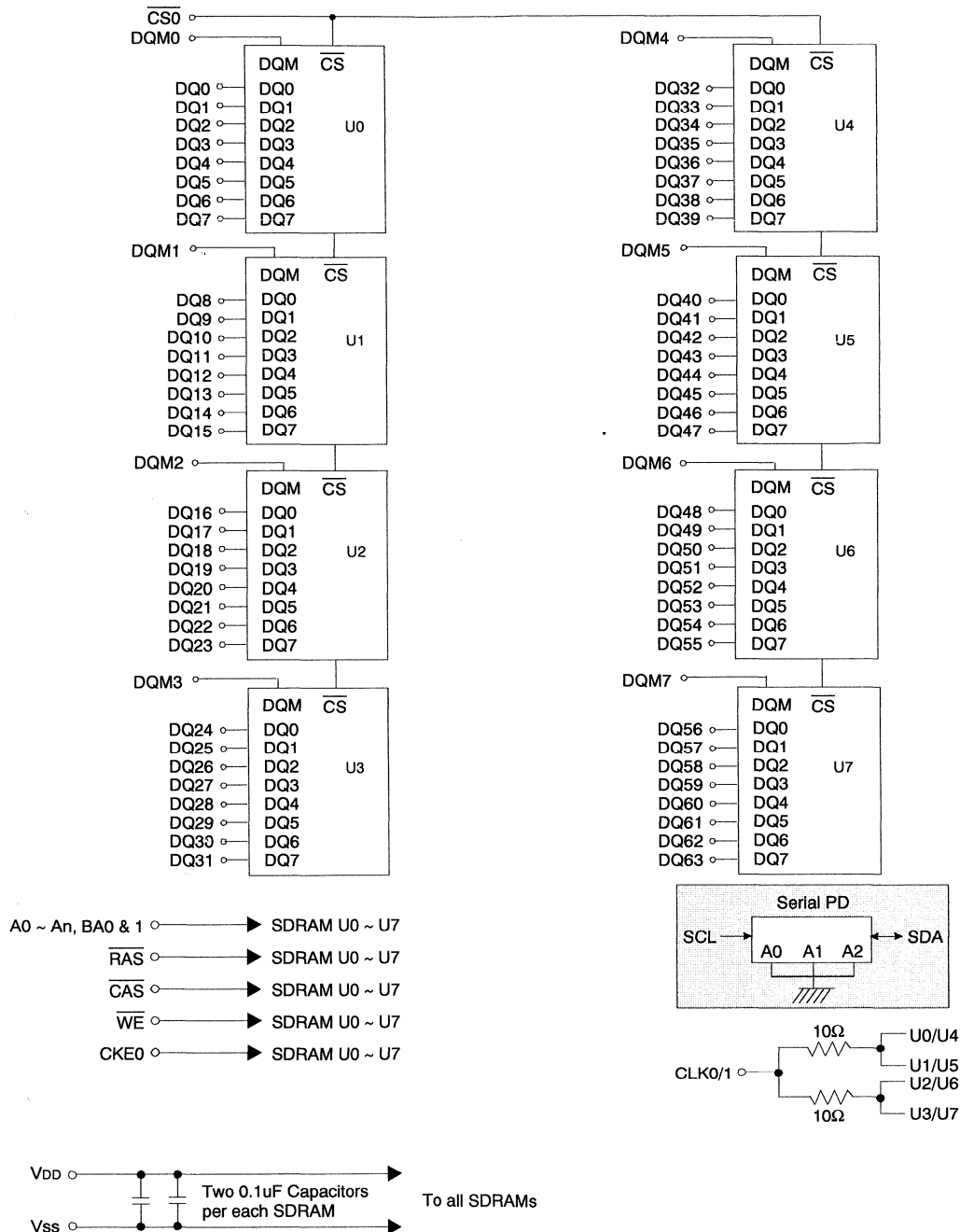
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	25	45	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	25	45	pF
Input capacitance (CKE0)	C _{IN3}	25	45	pF
Input capacitance (CLK0 ~ CLK1)	C _{IN4}	15	21	pF
Input capacitance ($\overline{\text{CS}}$ 0)	C _{IN5}	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	8	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	I _{CC1}	Burst length = 1 t _{RC} ≥ t _{RC} (min) I _O = 0 mA	880	mA	1
Precharge standby current in power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), t _{CC} = 10ns	8	mA	
	I _{CC2PS}	CKE & CLK ≤ V _{IL} (max), t _{CC} = ∞	8		
Precharge standby current in non power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(\min)$, t _{CC} = 10ns Input signals are changed one time during 20ns	160	mA	
	I _{CC2NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), t _{CC} = ∞ Input signals are stable	56		
Active standby current in power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), t _{CC} = 10ns	40	mA	
	I _{CC3PS}	CKE & CLK ≤ V _{IL} (max), t _{CC} = ∞	40		
Active standby current in non power-down mode (One bank active)	I _{CC3N}	CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(\min)$, t _{CC} = 10ns Input signals are changed one time during 20ns	240	mA	
	I _{CC3NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), t _{CC} = ∞ Input signals are stable	160	mA	
Operating current (Burst mode)	I _{CC4}	I _O = 0 mA Page burst 4Banks activated t _{CCD} = 2CLKs	1,000	mA	1
Refresh current	I _{CC5}	t _{RC} ≥ t _{RC} (min)	1,680	mA	2
Self refresh current	I _{CC6}	CKE ≤ 0.2V	C	12	mA
			L	6.4	mA

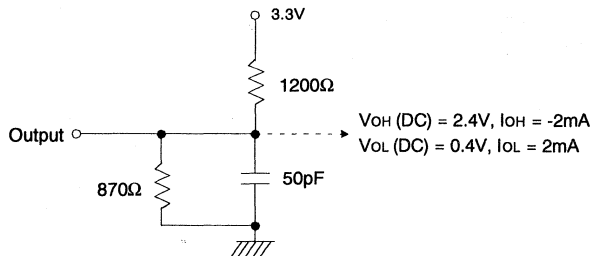
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

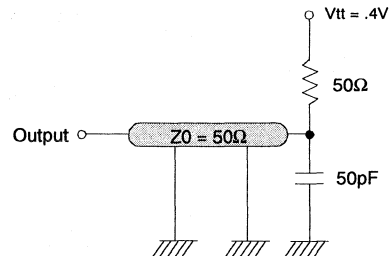
3. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	$t_{RRD}(\min)$	20	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	24	ns	1
Row precharge time	$t_{RP}(\min)$	24	ns	1
Row active time	$t_{RAS}(\min)$	50	ns	1
Row cycle time	$t_{RAS}(\max)$	100	us	
	$t_{RC}(\min)$	80	ns	1
	$t_{RDL}(\min)$	2	CLK	2,5
Last data in to row precharge	$t_{DAL}(\min)$	2 CLK + 20ns	-	5
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -10, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .

SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1$ ns.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA _{0,1}	A ₁₀ /AP	A ₁₁ , A ₉ ~ A ₀	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L	L	L	L	H	X	X		3	
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X		X		3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A ₀ ~ A ₉)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A ₀ ~ A ₉)	4
	Auto precharge enable										H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

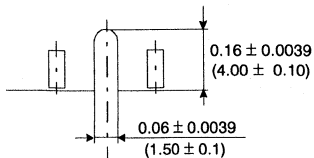
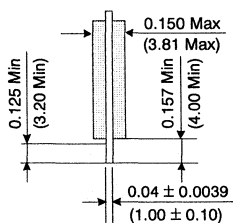
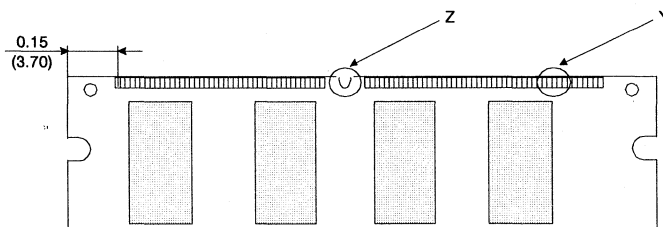
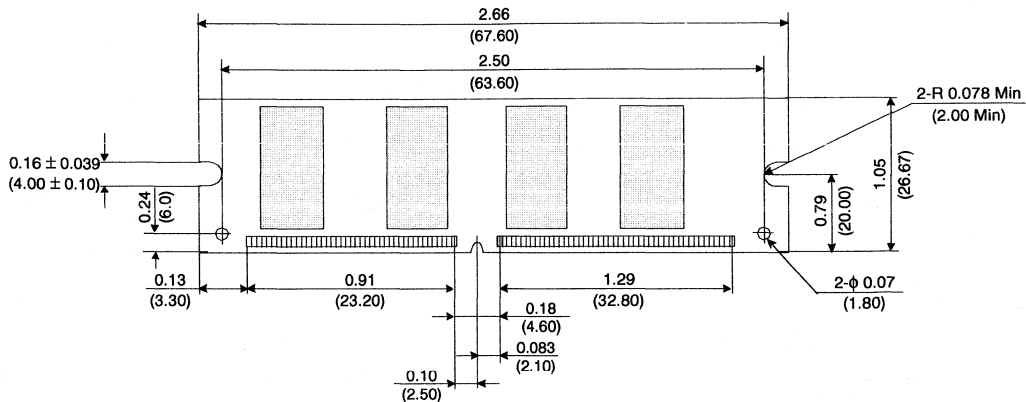
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

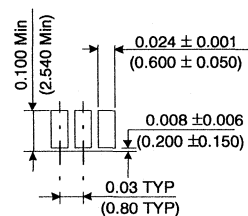
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832B

M466S1723BT3-L10, C10

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832B-TL10, C10
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,050mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 128MB	20h	
32-61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	FDh	

SERIAL PRESENCE DETECT

PC66 SODIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	3	33h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	3	33h	
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year.

4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsung 's own purpose.

M466S1724BT2 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M466S1724BT2 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S1724BT2 consists of eight CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S1724BT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M466S1724BT2-L10/C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,150mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS1	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

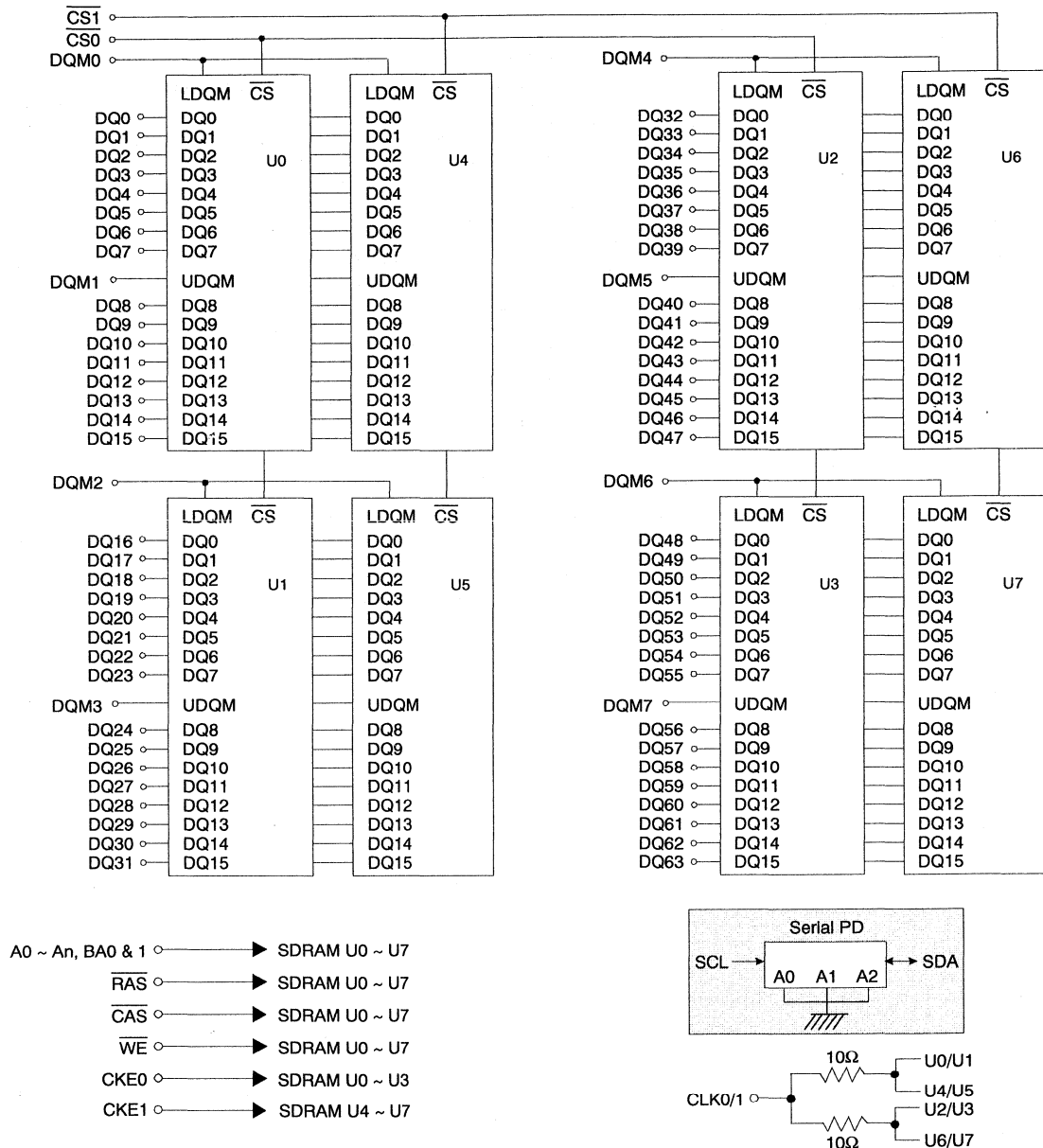
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	25	45	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	25	45	pF
Input capacitance (CKE ₀ ~ CKE ₁)	C _{IN3}	15	25	pF
Input capacitance (CLK ₀ ~ CLK ₁)	C _{IN4}	15	21	pF
Input capacitance ($\overline{\text{CS0}}$ ~ $\overline{\text{CS1}}$)	C _{IN5}	15	25	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	10	12	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	10	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-10		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC(min)}$ $I_O = 0 \text{ mA}$	680	mA	1
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL(max)}$, $t_{CC} = 10\text{ns}$	8	mA	
	ICC2PS	$CKE \& CLK \leq V_{IL(max)}$, $t_{CC} = \infty$	8		
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH(min)}$, $\overline{CS} \geq V_{IH(min)}$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	160	mA	
	ICC2NS	$CKE \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$, $t_{CC} = \infty$ Input signals are stable	56		
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL(max)}$, $t_{CC} = 10\text{ns}$	40	mA	
	ICC3PS	$CKE \& CLK \leq V_{IL(max)}$, $t_{CC} = \infty$	40		
Active standby current in non power-down mode (One bank active)	ICC3N	$CKE \geq V_{IH(min)}$, $\overline{CS} \geq V_{IH(min)}$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	240	mA	
	ICC3NS	$CKE \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$, $t_{CC} = \infty$ Input signals are stable	160	mA	
Operating current (Burst mode)	ICC4	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2CLKs$	700	mA	1
Refresh current	ICC5	$t_{RC} \geq t_{RC(min)}$	960	mA	2
Self refresh current	ICC6	$CKE \leq 0.2V$	C	12	mA
			L	6.4	mA

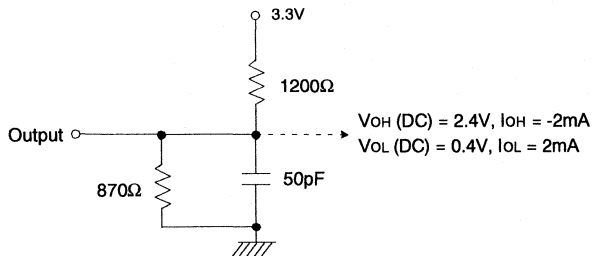
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

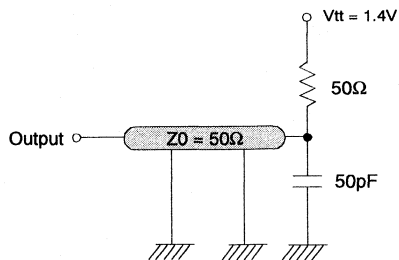
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	$t_{RRD}(\text{min})$	20	ns	1
RAS to $\overline{\text{CAS}}$ delay	$t_{RCD}(\text{min})$	24	ns	1
Row precharge time	$t_{RP}(\text{min})$	24	ns	1
Row active time	$t_{RAS}(\text{min})$	50	ns	1
Row cycle time	$t_{RAS}(\text{max})$	100	us	
	$t_{RC}(\text{min})$	80	ns	1
Last data in to row precharge	$t_{RDL}(\text{min})$	2	CLK	2,5
Last data in to Active delay	$t_{DAL}(\text{min})$	2 CLK + 20ns	-	5
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\text{min})$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\text{min})$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -10, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .
SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tsac		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	toH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tss	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
 If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
 i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set		H	X	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	L		3									
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

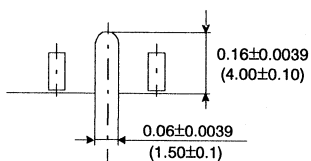
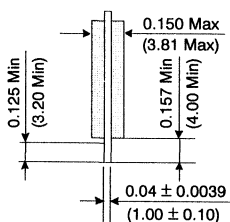
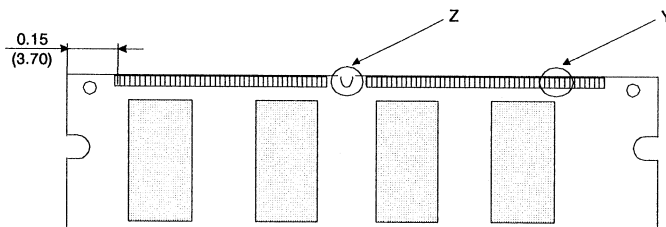
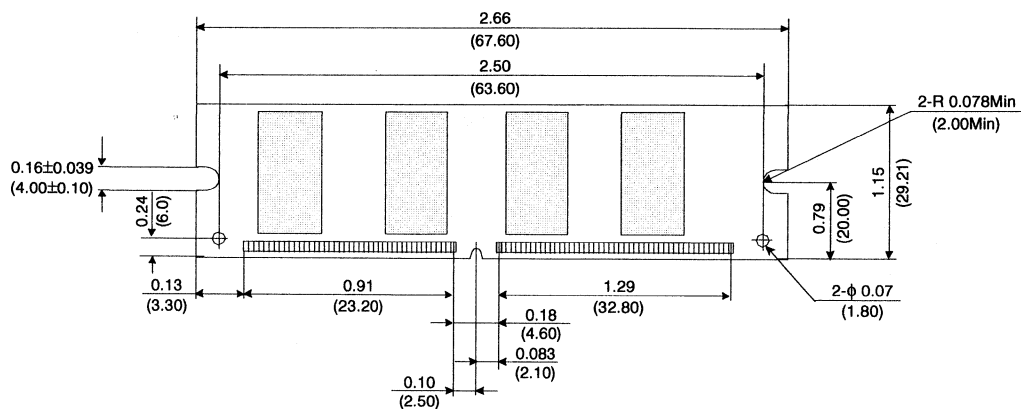
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

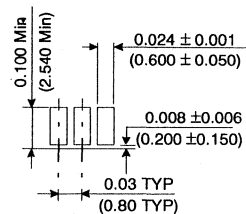
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ±0.005(.13) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
SDRAM Part No. : K4S281632B

M466S1724BT2-L10, C10

- Organization : 16Mx64
- Composition : 8Mx16 *8
- Used component part # : K4S281632B-TL10, C10
- # of banks in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	24ns	18h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	18h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	2 Rows of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	F5h	

Byte #	Function Described	Function Supported	Hex value	Note
		-10	-10	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

Module Specification

3

PC100 SODIMM

M464S0924MT1 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M464S0924MT1 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S0924MT1 consists of four CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S0924MT1 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M464S0924MT1-L1H	100MHz (10ns @ CL=2)
M464S0924MT1-L1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,000mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37	61	CLK0	62	CKE0	109	A9	110	BA1
17	DQ6	18	DQ38	63	VDD	64	VDD	111	A10/AP	112	A11
19	DQ7	20	DQ39	65	RAS	66	CAS	113	VDD	114	VDD
21	Vss	22	Vss	67	WE	68	*CKE1	115	DQM2	116	DQM6
23	DQM0	24	DQM4	69	CS0	70	*A12	117	DQM3	118	DQM7
25	DQM1	26	DQM5	71	*CS1	72	*A13	119	Vss	120	Vss
27	VDD	28	VDD	73	DU	74	*CLK1	121	DQ24	122	DQ56
29	A0	30	A3	75	Vss	76	Vss	123	DQ25	124	DQ57
31	A1	32	A4	77	NC	78	NC	125	DQ26	126	DQ58
33	A2	34	A5	79	NC	80	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	81	VDD	82	VDD	129	VDD	130	VDD
37	DQ8	38	DQ40	83	DQ16	84	DQ48	131	DQ28	132	DQ60
39	DQ9	40	DQ41	85	DQ17	86	DQ49	133	DQ29	134	DQ61
41	DQ10	42	DQ42	87	DQ18	88	DQ50	135	DQ30	136	DQ62
43	DQ11	44	DQ43	89	DQ19	90	DQ51	137	DQ31	138	DQ63
45	VDD	46	VDD	91	Vss	92	Vss	139	Vss	140	Vss
47	DQ12	48	DQ44	93	DQ20	94	DQ52	141	**SDA	142	**SCL
49	DQ13	50	DQ45					143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

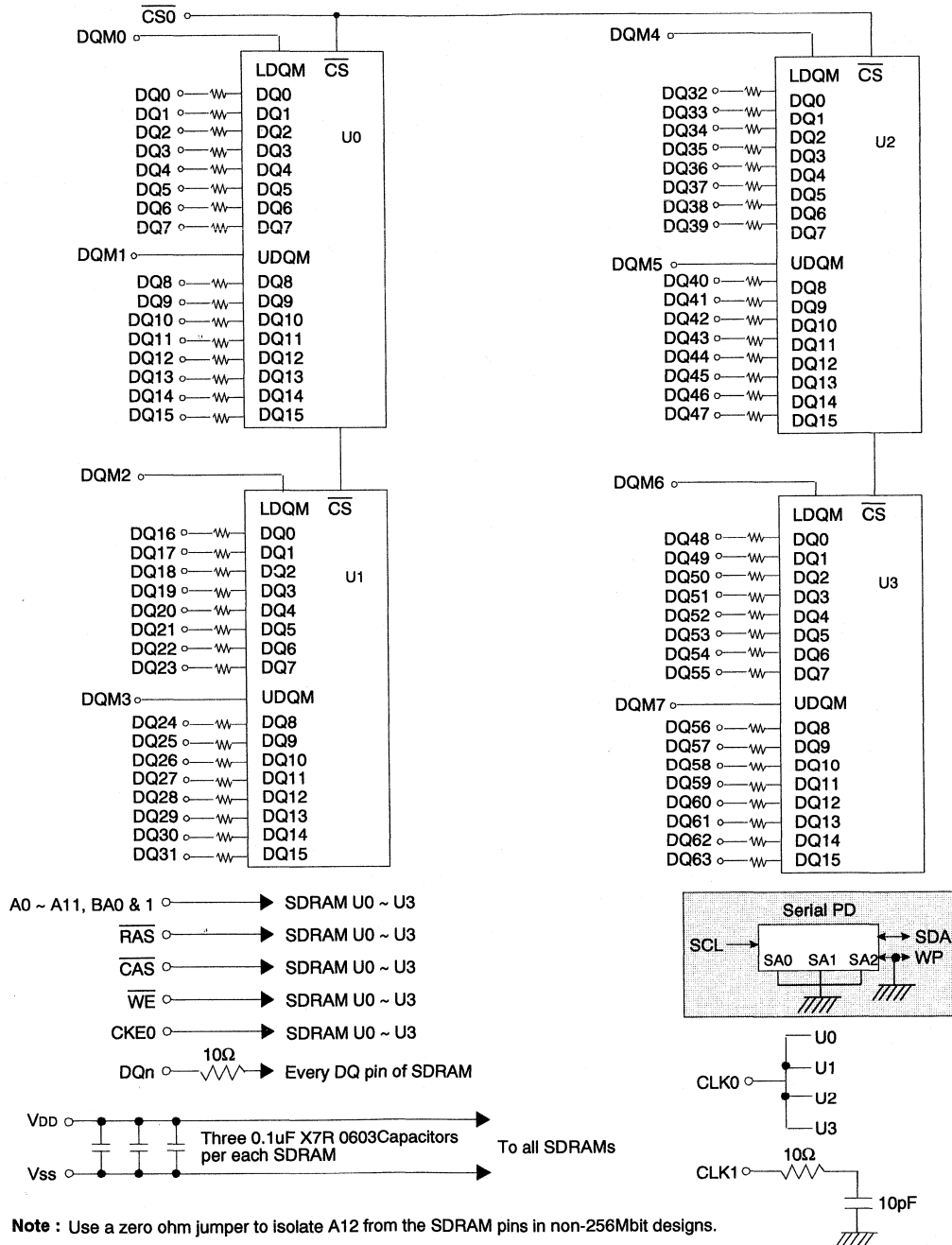
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	4	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C _{IN1}	20	30	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	20	30	pF
Input capacitance (CKE ₀)	C _{IN3}	20	30	pF
Input capacitance (CLK ₀)	C _{IN4}	20	26	pF
Input capacitance (CS ₀)	C _{IN5}	20	30	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	12	15	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	14	17	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

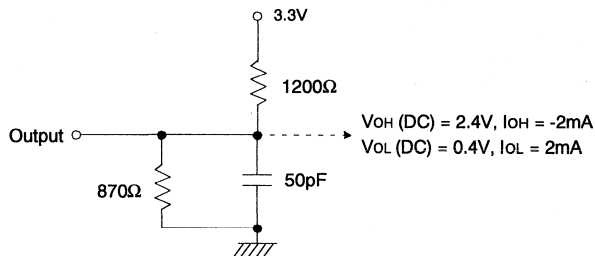
Parameter	Symbol	Test Condition	CAS Latency	Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	I _{CC1}	Burst length = 1 trc ≥ trc(min) IoL = 0 mA		480	480	mA	1
Precharge standby current in power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), tcc = 15ns		4		mA	
	I _{CC2PS}	CKE & CLK ≤ V _{IL} (max), tcc = ∞		4			
Precharge standby current in non power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), CS ≥ V _{IH} (min), tcc = 15ns Input signals are changed one time during 30ns		60		mA	
	I _{CC2NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), tcc = ∞ Input signals are stable		28			
Active standby current in power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), tcc = 15ns		20		mA	
	I _{CC3PS}	CKE & CLK ≤ V _{IL} (max), tcc = ∞		20			
Active standby current in non power-down mode (One bank active)	I _{CC3N}	CKE ≥ V _{IH} (min), CS ≥ V _{IH} (min), tcc = 15ns Input signals are changed one time during 30ns		120		mA	
	I _{CC3NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), tcc = ∞ Input signals are stable		80		mA	
Operating current (Burst mode)	I _{CC4}	IoL = 0 mA Page burst 2Banks activated tccd = 2CLKs	3	580	580	mA	1
			2	580	540		
Refresh current	I _{CC5}	trc ≥ trc(min)		800		mA	2
Self refresh current	I _{CC6}	CKE ≤ 0.2V		3.2		mA	

Notes : 1. Measured with outputs open.

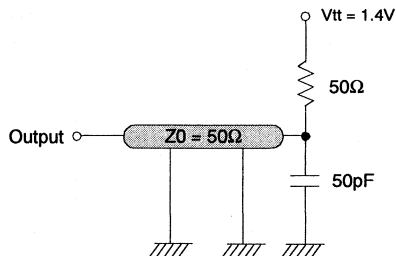
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	1		CLK	2
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3	
	Entry		L									3	
	Self refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable									H		4,5	
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable									H		4,5	
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X		
	All banks								X	H			
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

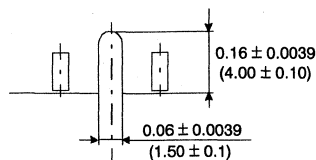
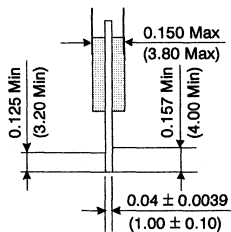
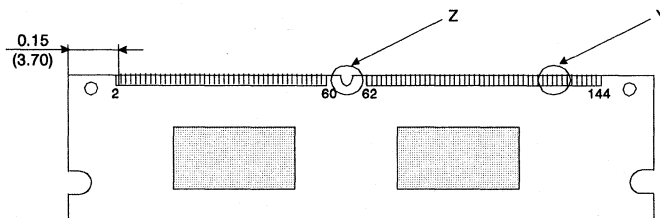
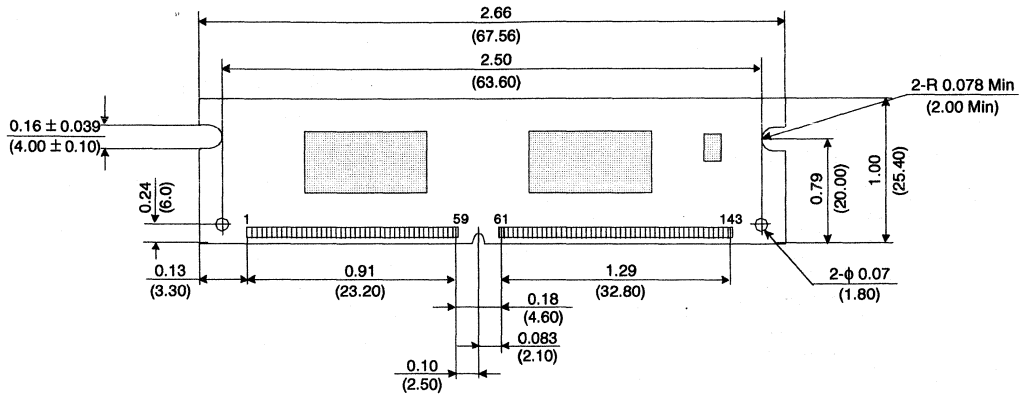
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

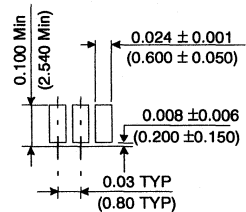
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ± 0.006(.15) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
 SDRAM Part No. : K4S281632M

SERIAL PRESENCE DETECT

PC100 SODIMM

M464S0924MT1-L1H/L1L

- Organization : 8MX64
- Composition : 8MX16 *4
- Used component part # : K4S281632M-TL1H/L1L
- # of banks in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,000 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	9		09h		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	64 bits		40h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	Non parity		00h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x16		10h		
14	Error checking SDRAM width	None		00h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing		00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 64MB		10h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		0Dh	3Dh	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	6		36h		
77	 Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	0		30h		
80	 Manufacturer part # (Module depth)	9		39h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	M		4Dh		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	1		31h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	L		4Ch		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	1		31h		
92	 Manufacturer revision code (For component)	M-die (1st Gen.)		4Dh		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~12	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M464S1724MT1 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 8Mx16,4Banks,4K Refresh,3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M464S1724MT1 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S1724MT1 consists of eight CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S1724MT1 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M464S1724MT1-L1H	100MHz (10ns @ CL=2)
M464S1724MT1-L1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,250mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS1	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

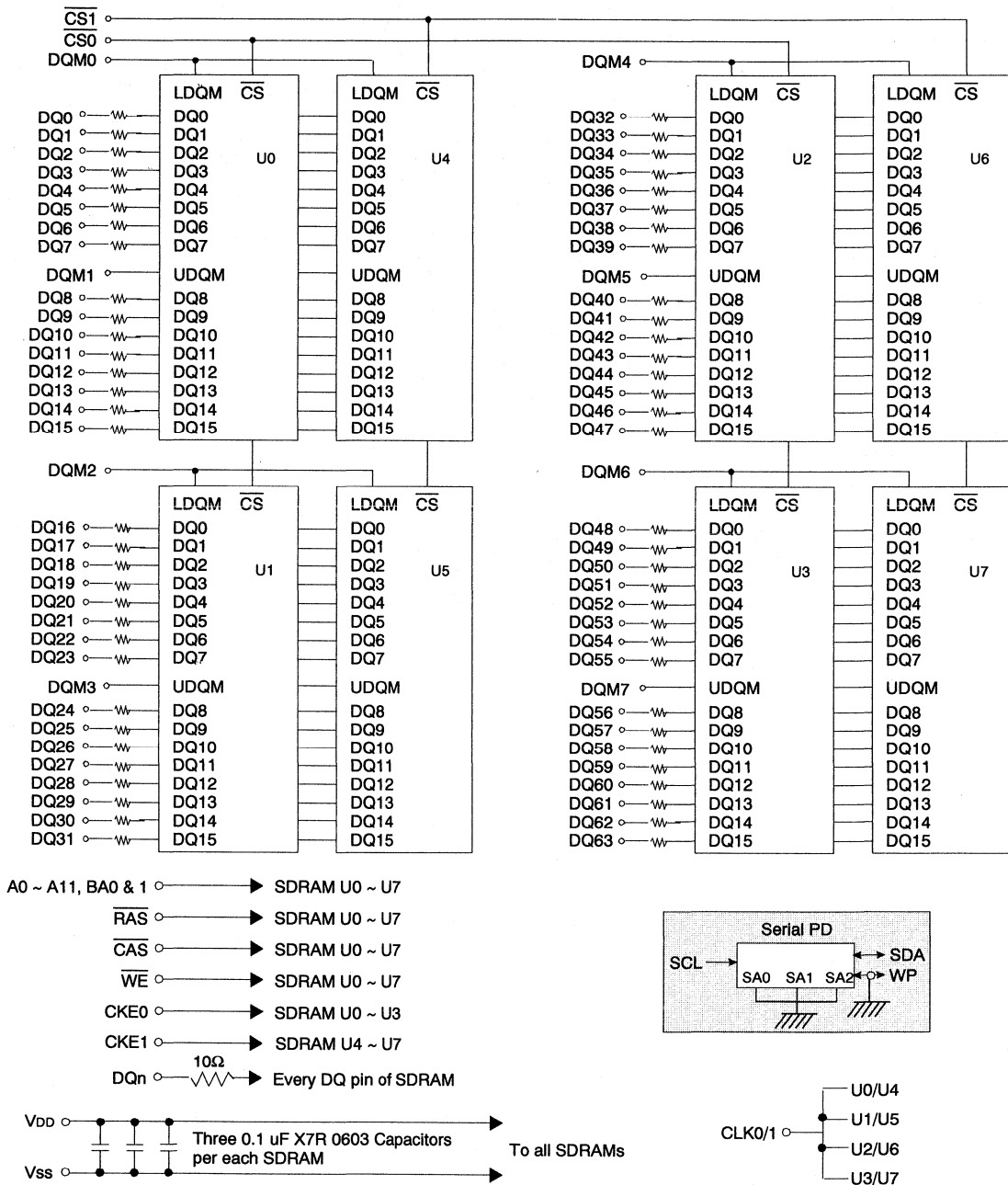
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I _{IL}	-3	-	3	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	30	50	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	30	50	pF
Input capacitance (CKE ₀ ~ CKE ₁)	C _{IN3}	20	30	pF
Input capacitance (CLK ₀ ~ CLK ₁)	C _{IN4}	20	26	pF
Input capacitance ($\overline{\text{CS}}$ ₀ ~ CS ₁)	C _{IN5}	20	30	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	15	20	pF
Data Input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	18	23	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

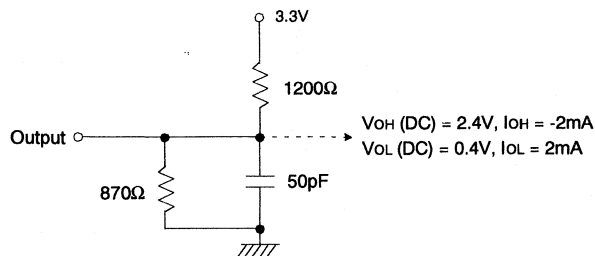
Parameter	Symbol	Test Condition	CAS Latency	Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		600	600	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		8		mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		8			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 15ns Input signals are changed one time during 30ns		120		mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		56			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		40		mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		40			
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 15ns Input signals are changed one time during 30ns		240		mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		160		mA	
Operating current (Burst mode)	ICC4	IOL = 0 mA Page burst 2Banks activated tccd = 2CLKs	3	700	700	mA	1
			2	700	660		
Refresh current	ICC5	trc ≥ trc(min)		1600		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V		6.4		mA	

Notes : 1. Measured with outputs open.

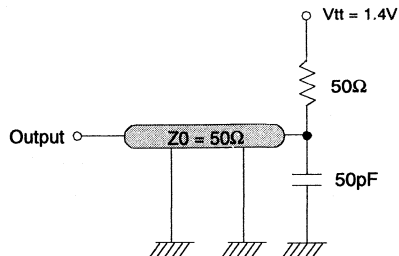
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	1		CLK	2
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3	2			ea	4
	CAS latency=2	1				

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1$ ns.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X	X			
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X	X			
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

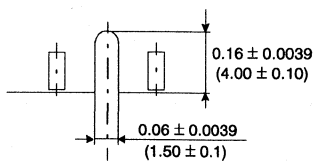
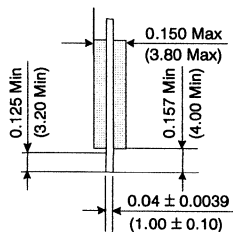
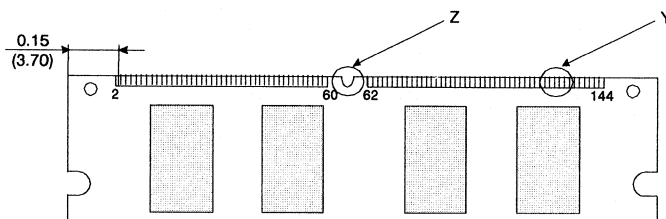
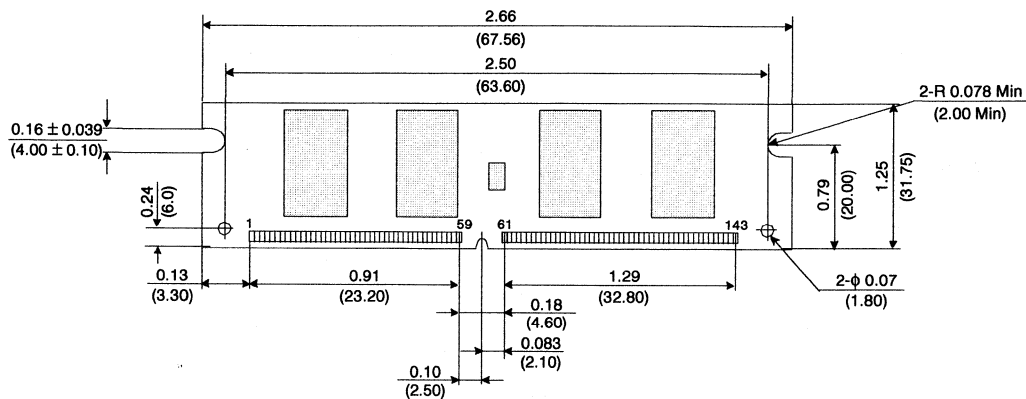
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

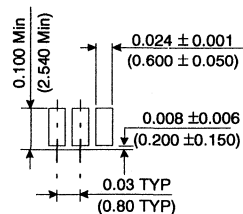
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : $\pm 0.006(.15)$ unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
SDRAM Part No. : K4S281632M

M464S1724MT1-L1H/L1L

- Organization : 16MX64
- Composition : 8MX16 *8
- Used component part # : K4S281632M-TL1H/L1L
- # of banks in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,250 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	9		09h		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	64 bits		40h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	Non parity		00h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x16		10h		
14	Error checking SDRAM width	None		00h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing		00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 64MB		10h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		0Eh	3Eh	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	6		36h		
77	 Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	 Manufacturer part # (Module depth)	7		37h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	M		4Dh		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	1		31h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	L		4Ch		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	1		31h		
92	 Manufacturer revision code (For component)	M-die (1st Gen.)		4Dh		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M464S0924BT1 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M464S0924BT1 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S0924BT1 consists of four CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S0924BT1 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M464S0924BT1-L1H /C1H	100MHz (10ns @ CL=2)
M464S0924BT1-L1L / C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address storbe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

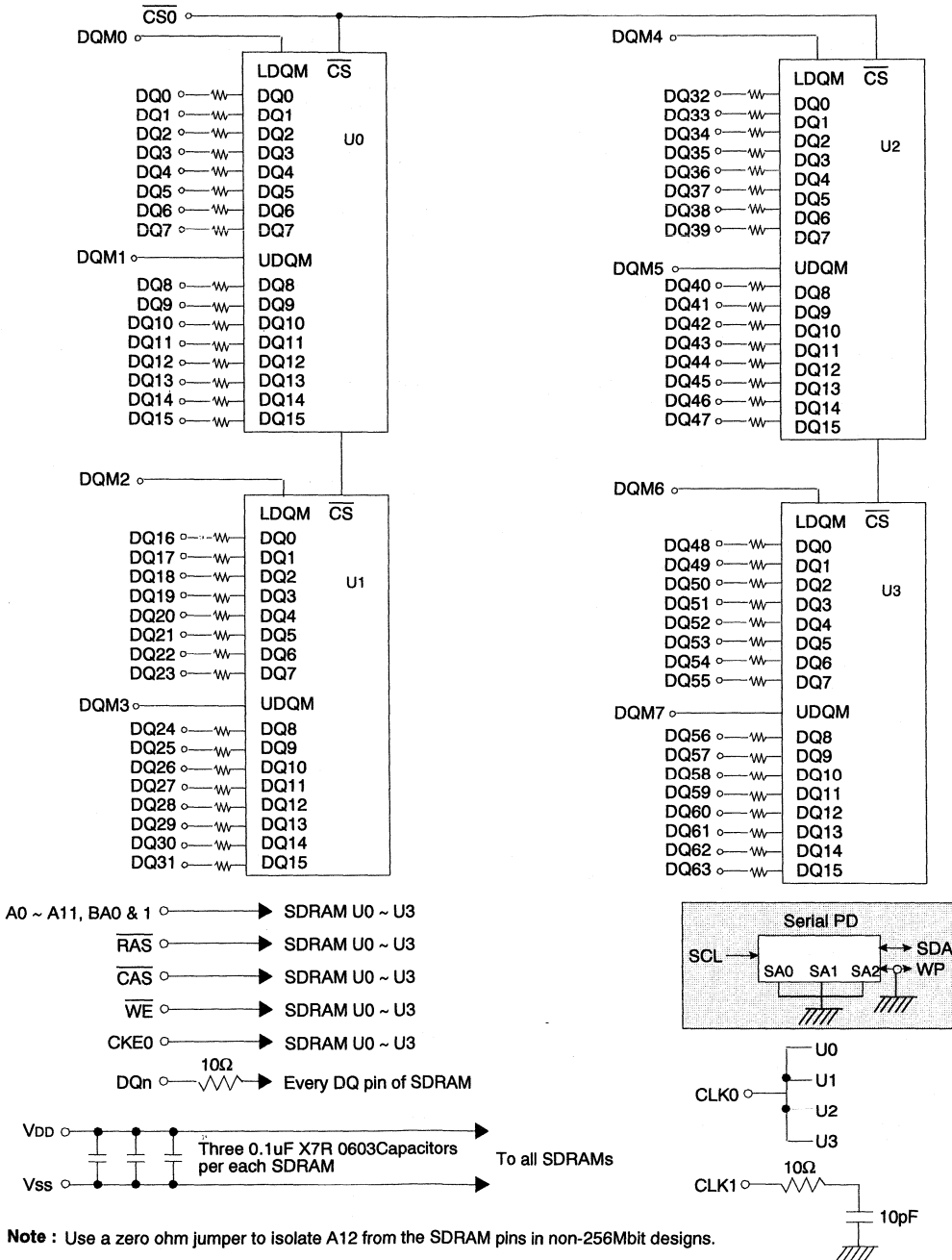
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{CS}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	4	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	15	25	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	15	25	pF
Input capacitance (CKE ₀)	C _{IN3}	15	25	pF
Input capacitance (CLK ₀)	C _{IN4}	15	21	pF
Input capacitance (CS ₀)	C _{IN5}	15	25	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	10	12	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	10	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	560		mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	4		mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	4			
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	80		mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	28			
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	20		mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	20			
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	120		mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	80		mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	580		mA	1
Refresh current	Icc5	trc ≥ trc(min)	840		mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	C	6	mA	
			L	3.2	mA	

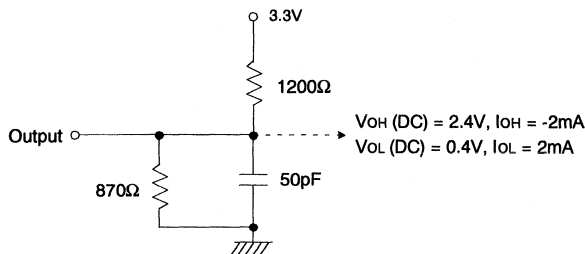
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

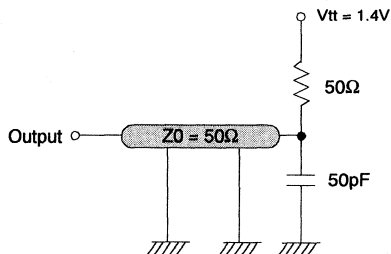
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -1H/1L, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported.
SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(t_r \& t_f) = 1$ ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA _{0,1}	A _{10/AP}	A ₁₁ , A ₉ ~ A ₀	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	X	X	X	X	3	
												H	X
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A ₀ ~ A ₉)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A ₀ ~ A ₉)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A_{10/AP} is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

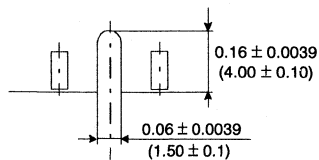
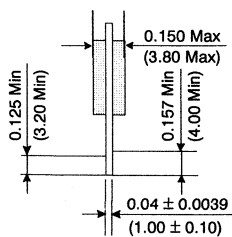
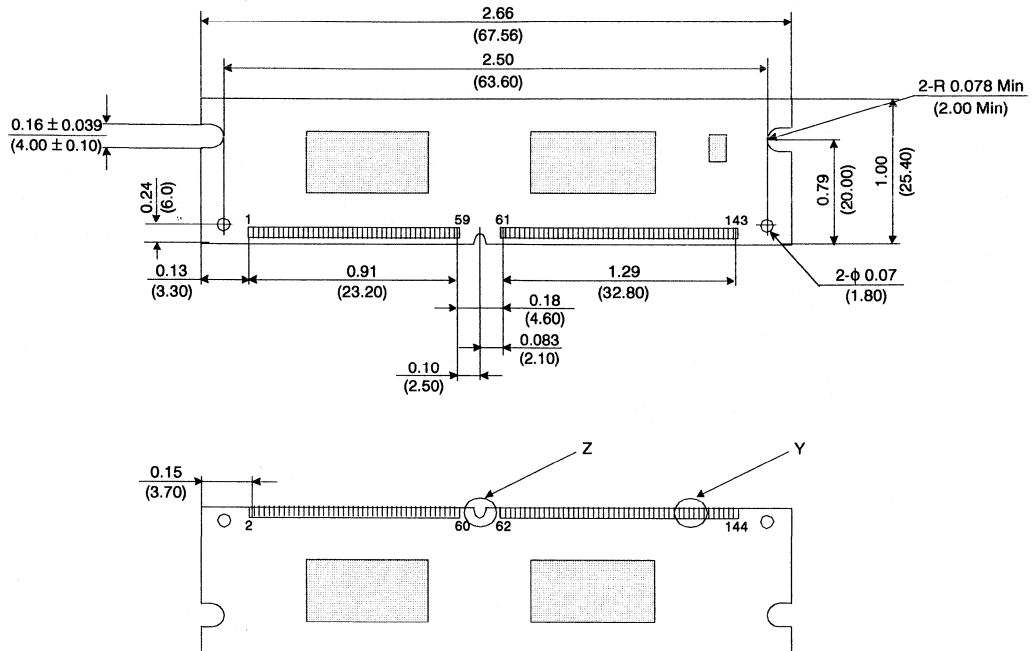
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

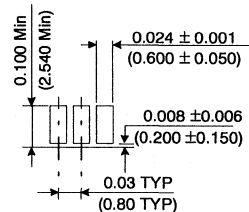
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ± 0.006(.15) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
 SDRAM Part No. : K4S281632B

M464S0924BT1-L1H/L1L, C1H/C1L

- Organization : 8MX64
- Composition : 8MX16 *4
- Used component part # : K4S281632B-TL1H/L1L, C1H/C1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,000 mil height & double sided component
- Refresh : 4K/64ms
- **Contents :**

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	9		09h		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	64 bits		40h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraon type	Non parity		00h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x16		10h		
14	Error checking SDRAM width	None		00h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing		00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 64MB		10h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		0Dh	3Dh	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	6		36h		
77	 Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	0		30h		
80	 Manufacturer part # (Module depth)	9		39h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	B		42h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	1		31h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	L / C		4Ch / 43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	1		31h		
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)		42h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~12	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M464S1724BT1 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 8Mx16,4Banks,4K Refresh,3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M464S1724BT1 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S1724BT1 consists of eight CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S1724BT1 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M464S1724BT1-L1H/C1H	100MHz (10ns @ CL=2)
M464S1724BT1-L1L/C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,250mil) , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37	61	CLK0	62	CKE0	109	A9	110	BA1
17	DQ6	18	DQ38	63	VDD	64	VDD	111	A10/AP	112	A11
19	DQ7	20	DQ39	65	RAS	66	CAS	113	VDD	114	VDD
21	Vss	22	Vss	67	WE	68	CKE1	115	DQM2	116	DQM6
23	DQM0	24	DQM4	69	CS0	70	*A12	117	DQM3	118	DQM7
25	DQM1	26	DQM5	71	CS1	72	*A13	121	DQ24	122	DQ56
27	VDD	28	VDD	73	DU	74	CLK1	123	DQ25	124	DQ57
29	A0	30	A3	75	Vss	76	Vss	125	DQ26	126	DQ58
31	A1	32	A4	77	NC	78	NC	127	DQ27	128	DQ59
33	A2	34	A5	79	NC	80	NC	129	VDD	130	VDD
35	Vss	36	Vss	81	VDD	82	VDD	131	DQ28	132	DQ60
37	DQ8	38	DQ40	83	DQ16	84	DQ48	133	DQ29	134	DQ61
39	DQ9	40	DQ41	85	DQ17	86	DQ49	135	DQ30	136	DQ62
41	DQ10	42	DQ42	87	DQ18	88	DQ50	137	DQ31	138	DQ63
43	DQ11	44	DQ43	89	DQ19	90	DQ51	139	Vss	140	Vss
45	VDD	46	VDD	91	Vss	92	Vss	141	**SDA	142	**SCL
47	DQ12	48	DQ44	93	DQ20	94	DQ52	143	VDD	144	VDD
49	DQ13	50	DQ45								

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS1	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

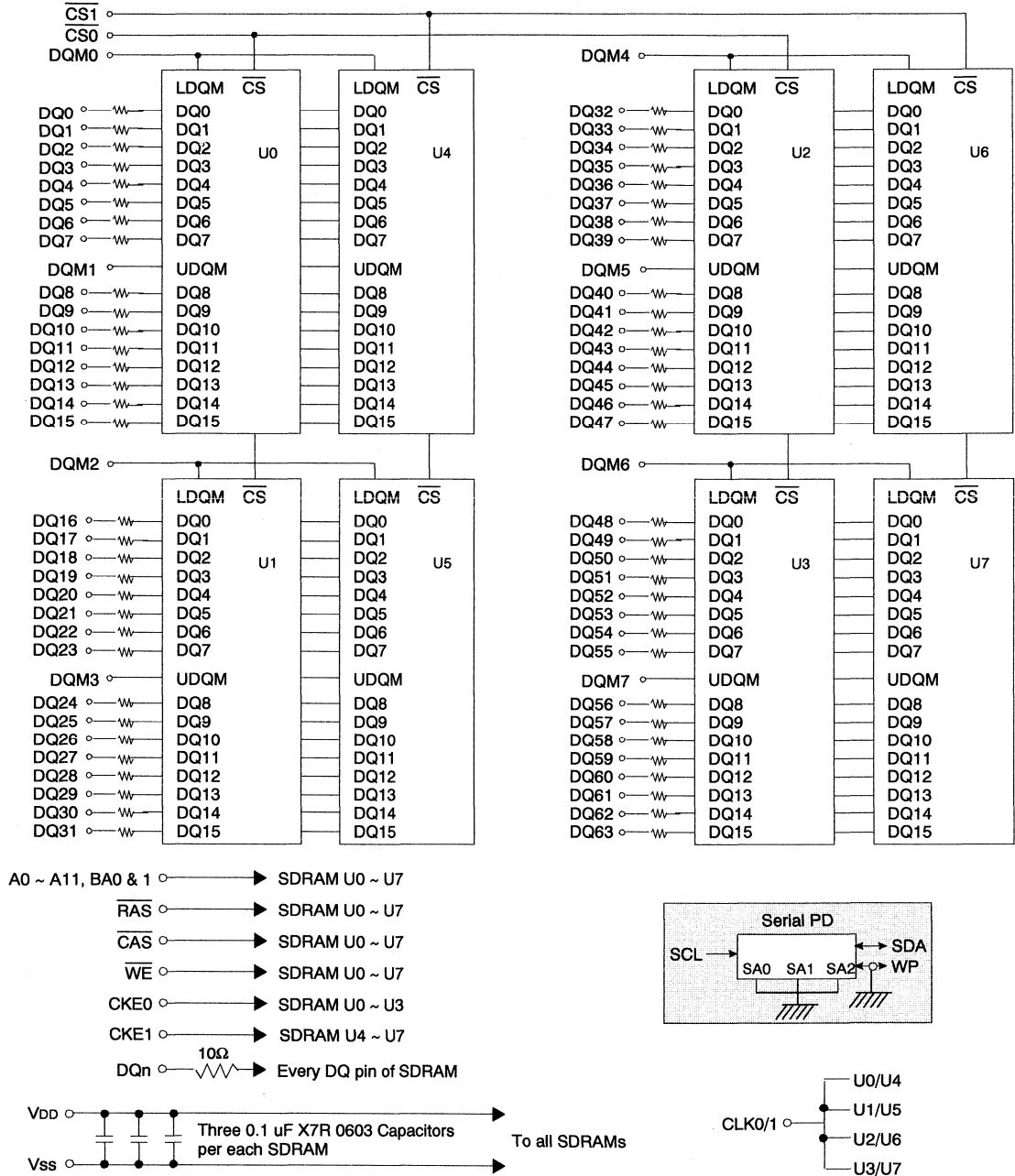
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	25	45	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	25	45	pF
Input capacitance (CKE ₀ ~ CKE ₁)	C _{IN3}	15	25	pF
Input capacitance (CLK ₀ ~ CLK ₁)	C _{IN4}	15	21	pF
Input capacitance ($\overline{\text{CS0}}$ ~ $\overline{\text{CS1}}$)	C _{IN5}	15	25	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	10	12	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	10	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition		Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	I _{CC1}	Burst length = 1 trc ≥ trc(min) Io = 0 mA		680		mA	1
Precharge standby current in power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), tcc = 10ns		8		mA	
	I _{CC2PS}	CKE & CLK ≤ V _{IL} (max), tcc = ∞		8			
Precharge standby current in non power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), $\overline{CS}$ ≥ V _{IH} (min), tcc = 10ns Input signals are changed one time during 20ns		160		mA	
	I _{CC2NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), tcc = ∞ Input signals are stable		56			
Active standby current in power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), tcc = 10ns		40		mA	
	I _{CC3PS}	CKE & CLK ≤ V _{IL} (max), tcc = ∞		40			
Active standby current in non power-down mode (One bank active)	I _{CC3N}	CKE ≥ V _{IH} (min), $\overline{CS}$ ≥ V _{IH} (min), tcc = 10ns Input signals are changed one time during 20ns		240		mA	
	I _{CC3NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), tcc = ∞ Input signals are stable		160		mA	
Operating current (Burst mode)	I _{CC4}	Io = 0 mA Page burst 4Banks activated tccD = 2CLKs		700		mA	1
Refresh current	I _{CC5}	trc ≥ trc(min)		960		mA	2
Self refresh current	I _{CC6}	CKE ≤ 0.2V	C	12		mA	
			L	6.4		mA	

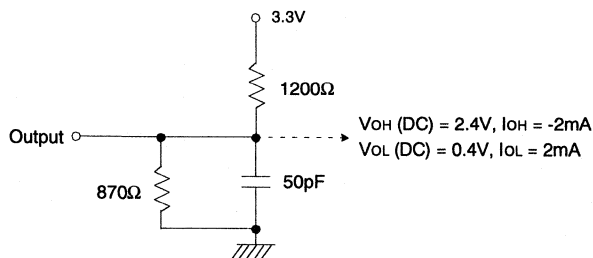
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

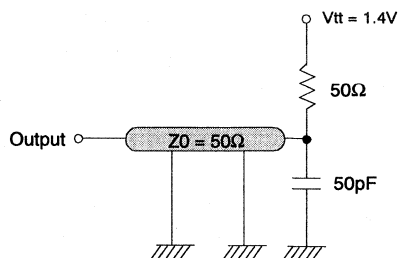
3. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -1H/1L, $t_{RD}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .
SAMSUNG recommends $t_{RD}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	toH	3		3		ns	2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

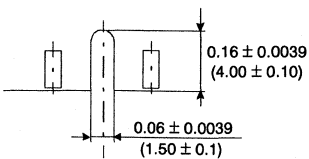
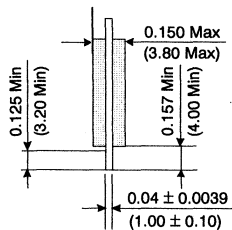
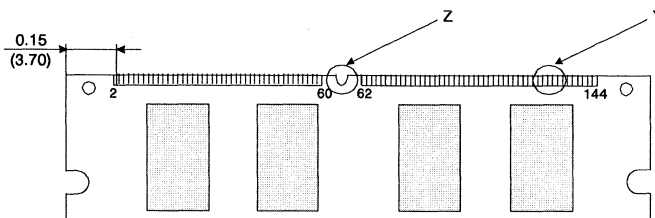
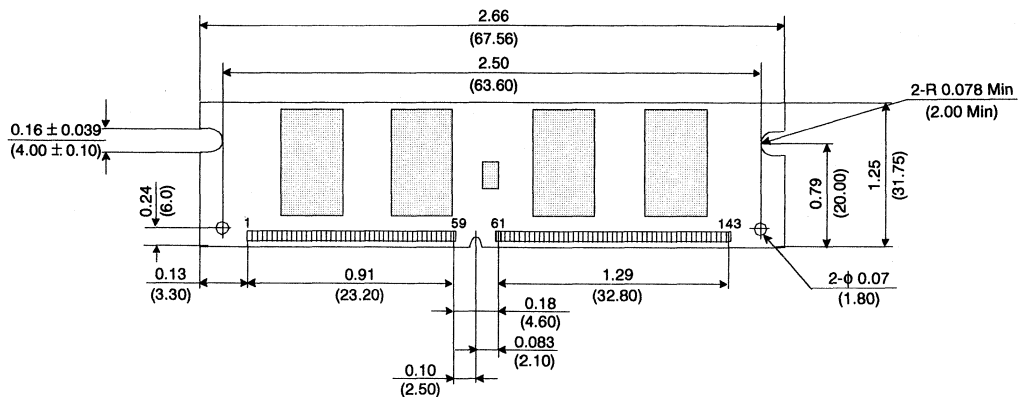
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

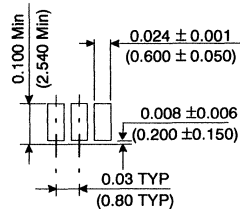
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ±0.006(.15) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
 SDRAM Part No. : K4S281632B

M464S1724BT1-L1H/L1L, C1H/C1L

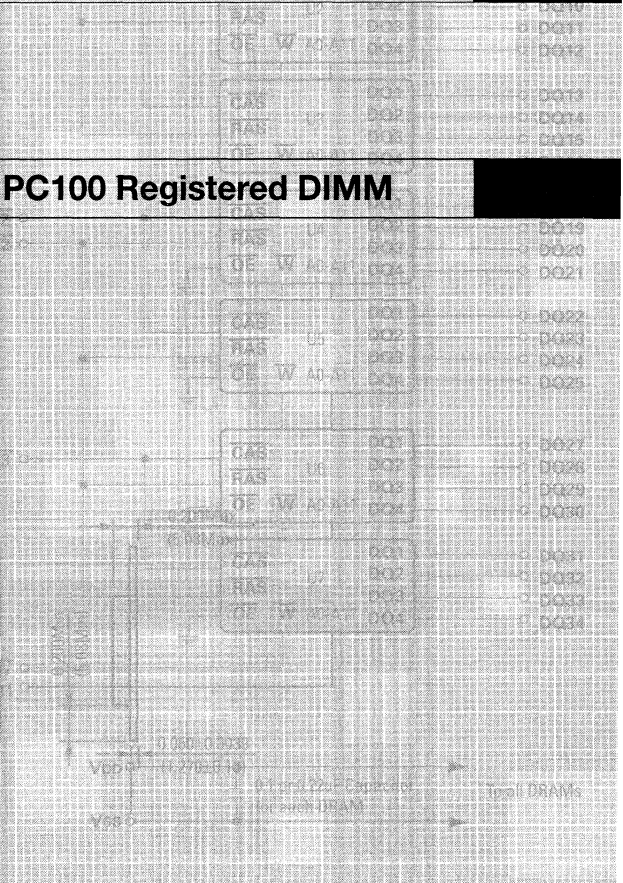
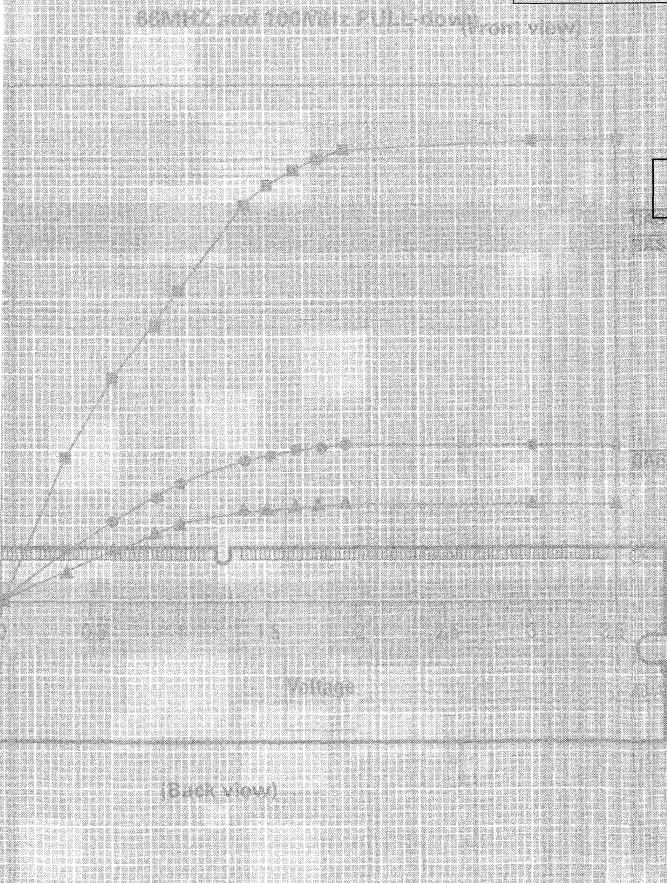
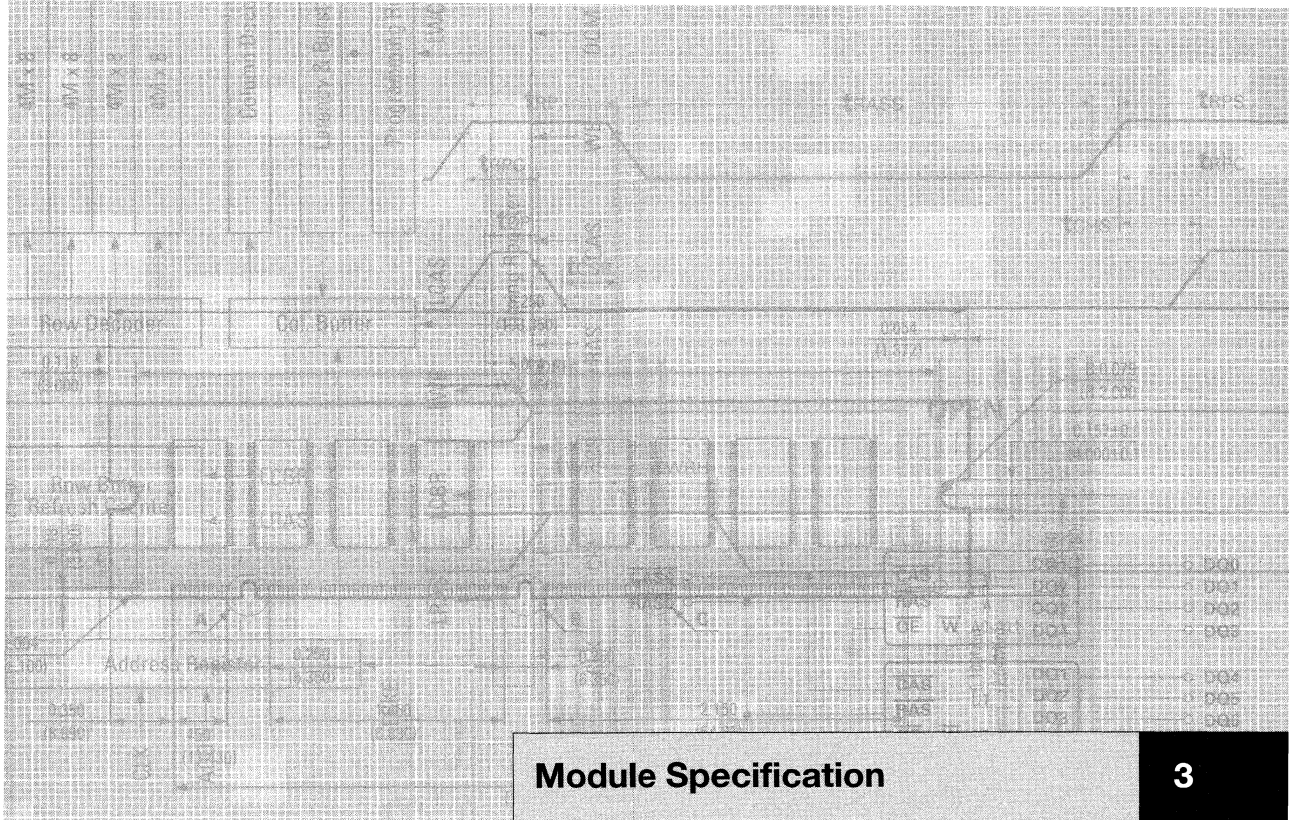
- Organization : 16MX64
- Composition : 8MX16 *8
- Used component part # : K4S281632B-TL1H/L1L, C1H/C1L
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,250 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	9		09h		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	64 bits		40h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	Non parity		00h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x16		10h		
14	Error checking SDRAM width	None		00h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing		00h		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 64MB		10h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		0Eh	3Eh	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	6		36h		
77	 Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	 Manufacturer part # (Module depth)	7		37h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	B		42h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	1		31h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	L / C		4Ch / 43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	1		31h		
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)		42h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.



M377S1723MT3 SDRAM DIMM (Intel 1.2 ver Base)

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S1723MT3 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S1723MT3 consists of nine CMOS 16Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S1723MT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S1723MT3-C1H	100MHz (10ns @ CL=2)
M377S1723MT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,500mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

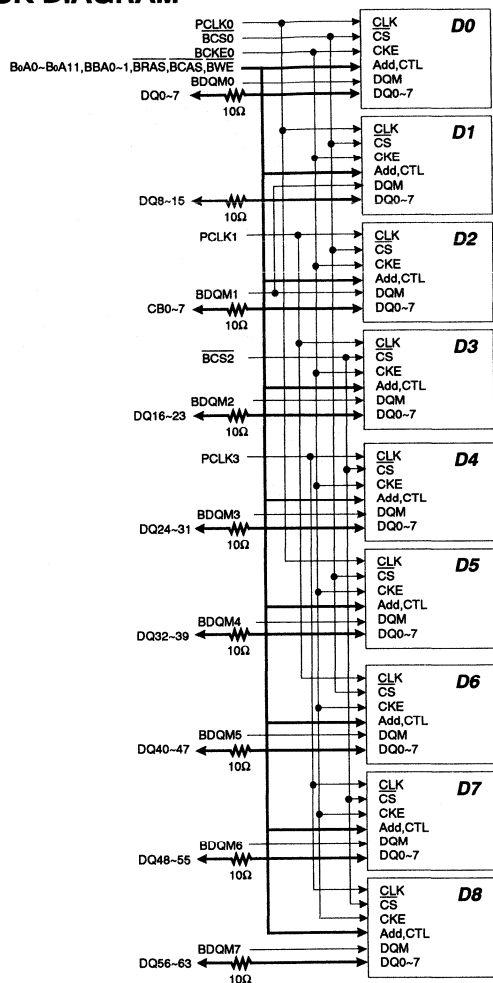
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

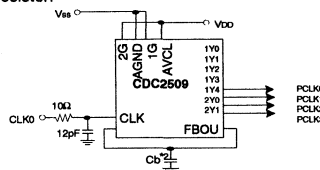
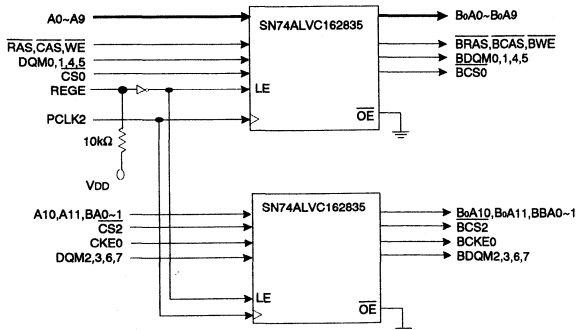
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM

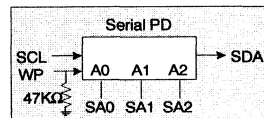


Notes : Address/Control Signals are connected to D2 through 100 ohms resistor.

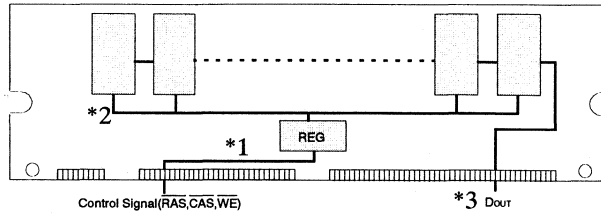
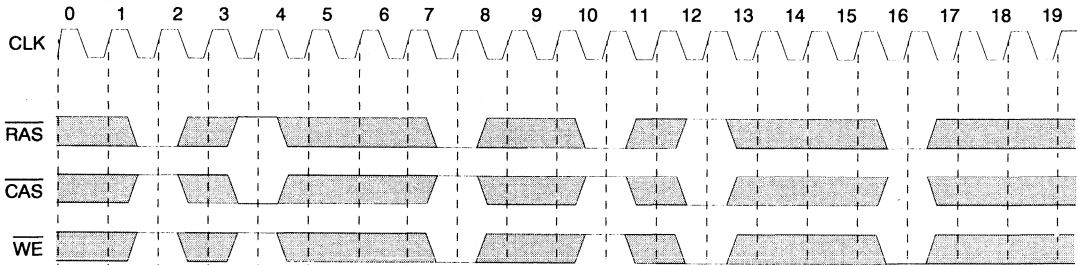
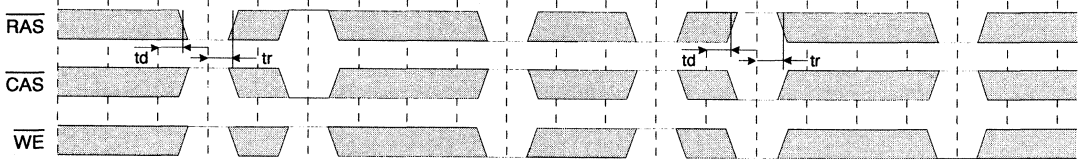
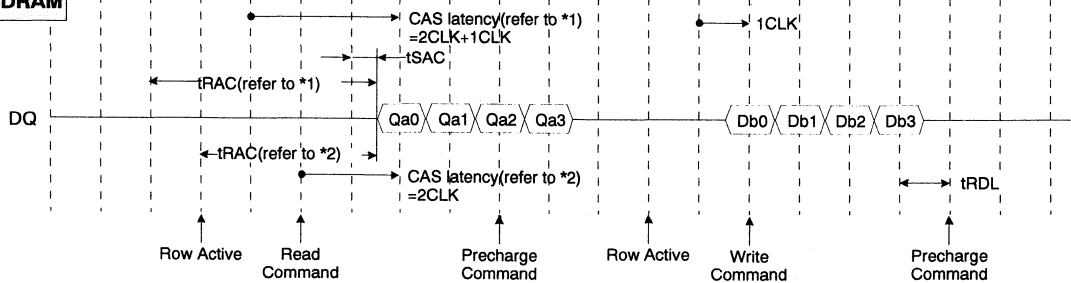


Note

1. Unused clock termination : 10 Ω and 12pF
2. The actual values of Cb will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

t_d , t_r = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-2	-	2	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ VDDQ

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

4. Dout is disabled, 0V ≤ V_{OUT} ≤ VDDQ

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C _{IN1}	-	16	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	-	16	pF
Input capacitance (CKE0)	C _{IN3}	-	16	pF
Input capacitance (CLK0)	C _{IN4}	-	40	pF
Input capacitance ($\overline{\text{CS0}}$, $\overline{\text{CS2}}$)	C _{IN5}	-	16	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	16	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	16	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	17	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	17	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		1,140		mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		10		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		10			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		136		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		64			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		46		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		46			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		270		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		180		mA	3
Operating current (Burst mode)	ICC4	IOL = 0mA Page burst 2Banks activated tccd=2CLK	3	1,270	1,270	mA	1
			2	1,270	1,180		
Refresh current	ICC5	trc ≥ trc(min)		1,800		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V		15		mA	3

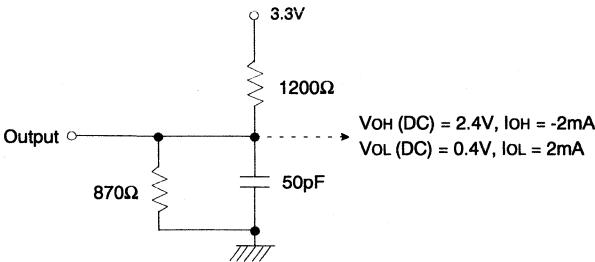
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

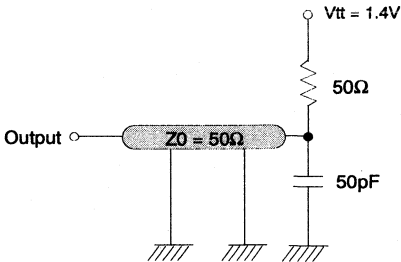
3. Measured with 1 PLL & 2 Drive ICs.

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version		Unit	Note
		-1H	-1L		
Row active to row active delay	tRRD(min)	20	20	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	tRCD(min)	20	20	ns	1
Row precharge time	tRP(min)	20	20	ns	1
Row active time	tRAS(min)	50	50	ns	1
	tRAS(max)	100		us	
Row cycle time	tRC(min)	70	70	ns	1
Last data in to new col. address delay	tCDL(min)	1		CLK	2
Last data in to row precharge	tRDL(min)	1		CLK	2
Last data in to burst stop	tBDL(min)	1		CLK	2
Col. address to col. address delay	tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3	2		ea	4
	CAS latency=2	1			

- Notes :
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	toH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3
	Self refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X	X		3
					H	X	X	X			3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks								X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X		
					L	V	V	V				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X		
					L	H	H	H				
		Exit	L	H	H	X	X	X	X			
					L	V	V	V				
DQM		H	X					V	X		7	
No operation command		H	X	H	X	X	X	X	X			
				L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

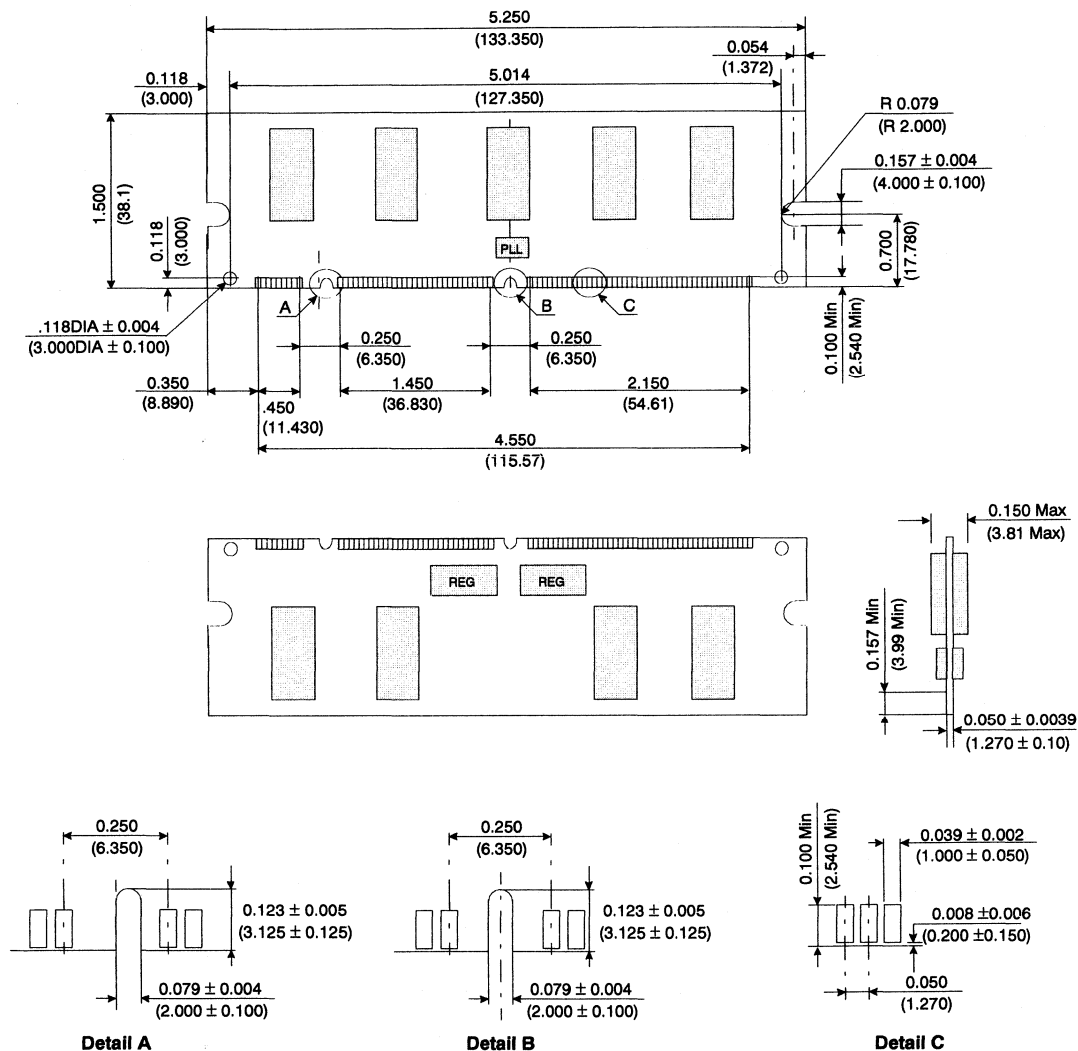
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832M

M377S1723MT3-C1H/C1L (1.2ver)

- Organization : 16MX72
- Composition : 16MX8 *9
- Used component part # : K4S280832M-TC1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 , 8 and full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		47h	77h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	 Manufacturer part # (Module depth)	7		37h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	M		4Dh		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	M-die (1st Gen.)		4Dh		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S3320MT3 SDRAM DIMM (Intel 1.2 ver Base)

32Mx72 SDRAM DIMM with PLL & Register based on 32Mx4, 4Banks, 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S3320MT3 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S3320MT3 consists of eighteen CMOS 32Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.002uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S3320MT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S3320MT3-C1H	100MHz (10ns @ CL=2)
M377S3320MT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4 & 8 page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	*CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	*SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	*SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

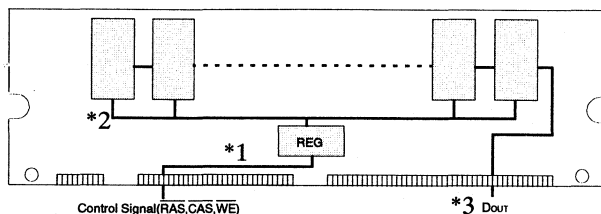
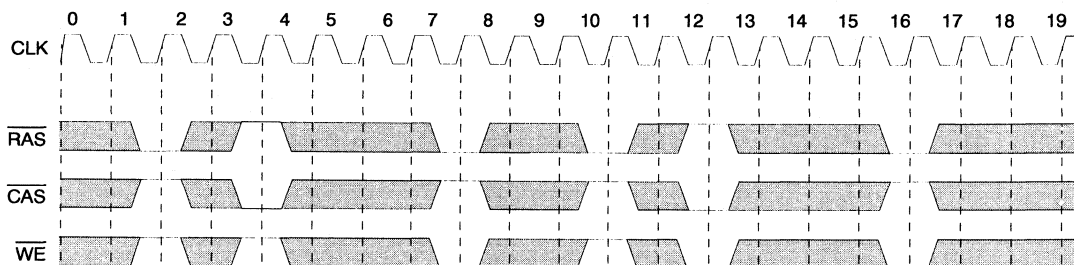
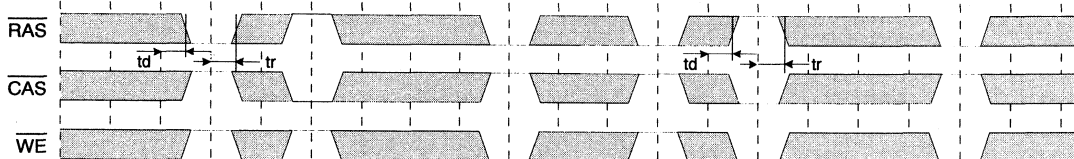
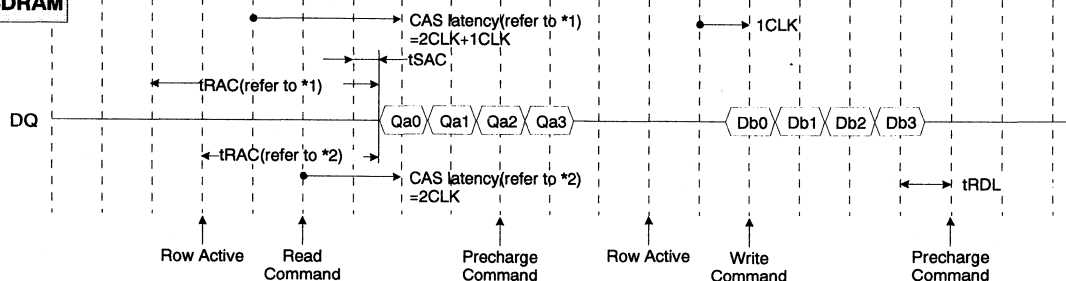
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write Protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-3	-	3	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C _{IN1}	-	20	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	-	20	pF
Input capacitance (CKE0)	C _{IN3}	-	20	pF
Input capacitance (CLK0)	C _{IN4}	-	26	pF
Input capacitance (CS0, CS2)	C _{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	17	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	17	pF

DC CHARACTERISTICS

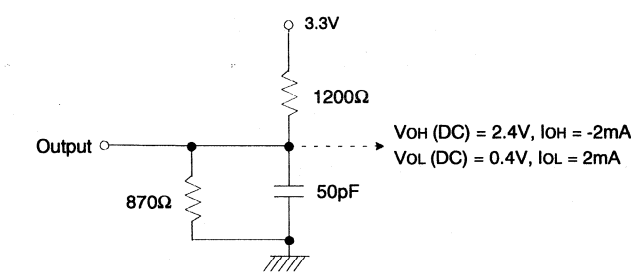
(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		2,180	2,180	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		20		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		20			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 15ns Input signals are changed one time during 30ns		272		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		128			
Active Standby Current in Power-down Mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		92		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		92			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 15ns Input signals are changed one time during 30ns		540		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		360		mA	3
Operating current (Burst mode)	ICC4	IOL = 0mA Page burst 2 Banks activated tccd=2CLK	3	2,270	2,270	mA	1
			2	2,270	2,090		
Refresh current	ICC5	trc ≥ trc(min)		3,800		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V		29		mA	3

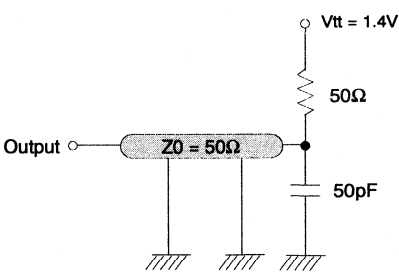
- Notes :** 1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Measured with 1 PLL & 3 Drive ICs.

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	1		CLK	2
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3	2		ea	4	
	CAS latency=2	1				

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(t_r \text{ \& } t_f) = 1$ ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA _{0,1}	A ₁₀ /AP	A ₁₁ , A ₉ ~ A ₀	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A ₀ ~ A ₉ , A ₁₁)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A ₀ ~ A ₉ , A ₁₁)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

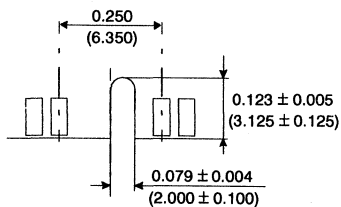
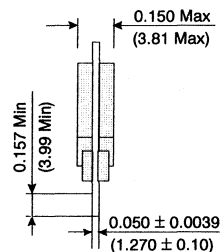
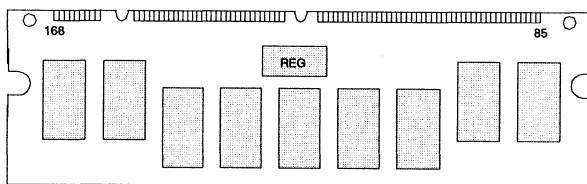
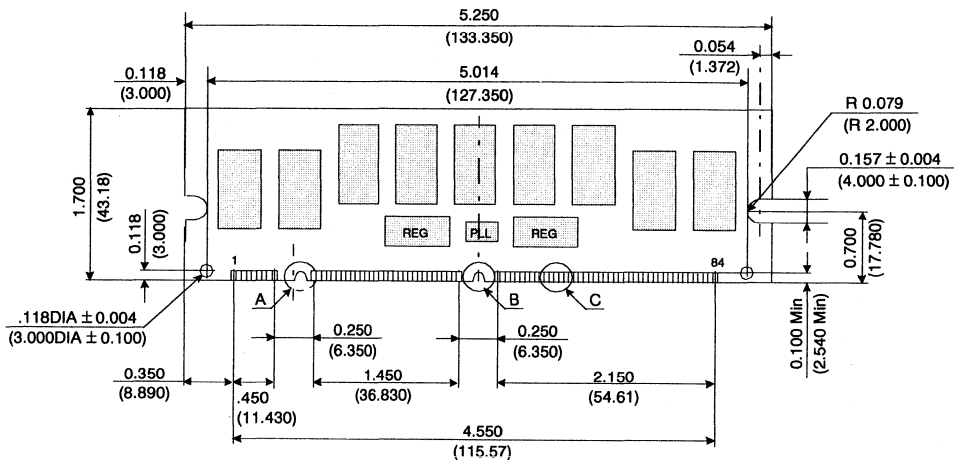
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

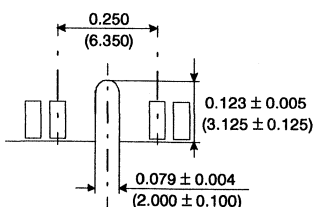
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

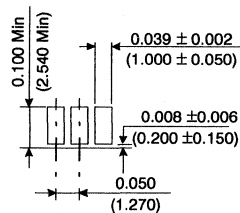
Units : Inches (Millimeters)



Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 32Mx4 SDRAM, TSOP
SDRAM Part No. : K4S280432M

SERIAL PRESENCE DETECT

PC100 Registered DIMM

M377S3320MT3-C1H/C1L (1.2ver)

- Organization : 32MX72
- Composition : 32MX4 *18
- Used component part # : K4S280432M-TC1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	11		0Bh		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1 CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 & 8 page		0Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 256MB		40h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		E0h	10h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	3		33h		
80	 Manufacturer part # (Module depth)	3		33h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	0		30h		
83	Manufacturer part # (Component revision)	M		4Dh		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	M-die (1st Gen.)		4Dh		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S3323MT0 SDRAM DIMM (Intel 1.2 ver. Base)

32Mx72 SDRAM DIMM with PLL & Register based on 16Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S3323MT0 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S3323MT0 consists of eighteen CMOS 16Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S3323MT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock-cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S3323MT0-C1H	100MHz (10ns) @CL=2
M377S3323MT0-C1L	100MHz (10ns) @CL=3

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

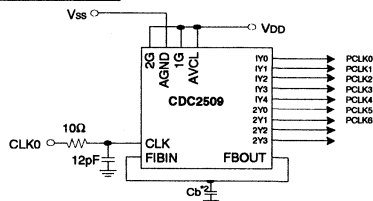
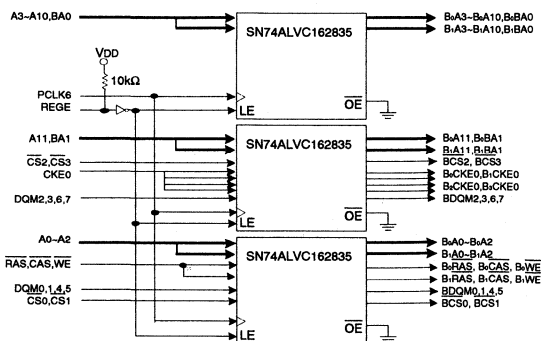
* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

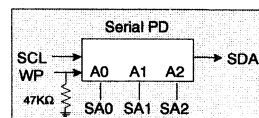
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System Clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip Select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock Enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank Select Address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row Address Strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column Address Strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write Enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data Input/Output Mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data Input/Output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write Protection</i>	WP pin is connected to Vcc. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power Supply/Ground</i>	Power and ground for the input buffers and the core logic.

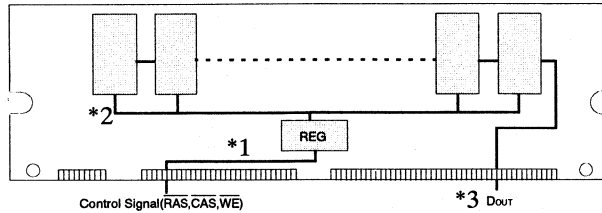
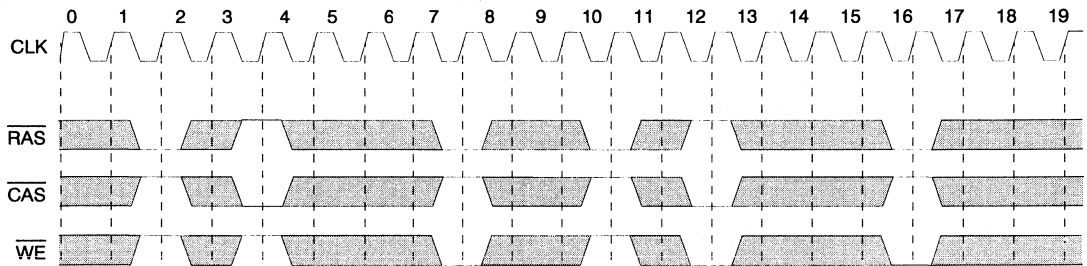
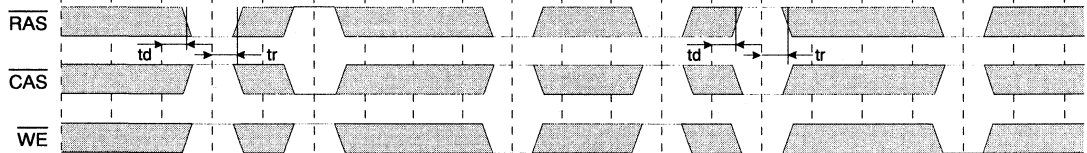
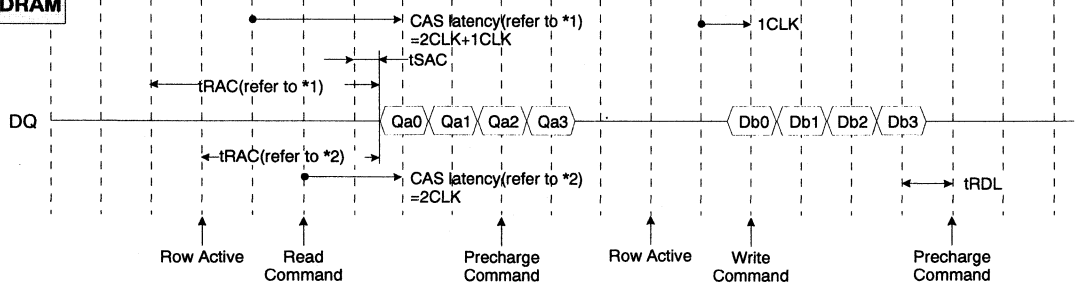


Note

1. Unused clock termination : $10\ \Omega$ and 12pF
2. The actual values of C_b will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER(CL=2,BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

t_d, t_r = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

 : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current(Inputs)	I _{IL}	-2	-	2	uA	3
Input leakage current (I/O pins)	I _{IL}	-3	-	3	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C _{IN1}	-	22	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	22	pF
Input capacitance (CKE0)	C _{IN3}	-	22	pF
Input capacitance (CLK0)	C _{IN4}	-	28	pF
Input capacitance ($\overline{\text{CS0}}$ ~ $\overline{\text{CS3}}$)	C _{IN5}	-	16	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	16	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	22	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	20	pF
Data input/output capacitance (CB0~CB7)	C _{OUT1}	-	20	pF

DC CHARACTERISTICS

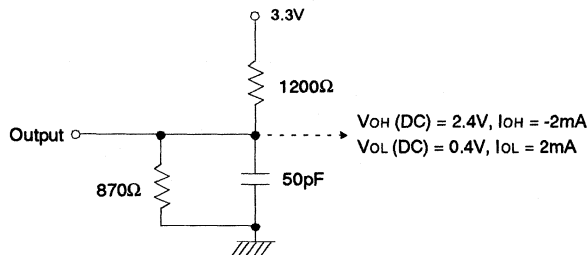
(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	ICC1	Burst length =1 trc ≥ trc(min) IOL = 0 mA		1,450	1,450	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		20		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		20			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		270		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		128			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		90		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		90			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		540		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		360		mA	3
Operating current (Burst mode)	ICC4	IOL = 0mA Page Burst 2 Banks activated tccd=2CLK	3	1,590	1,590	mA	1
			2	1,590	1,500		
Refresh current	ICC5	trc ≥ trc(min)		3,600		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V		28		mA	3

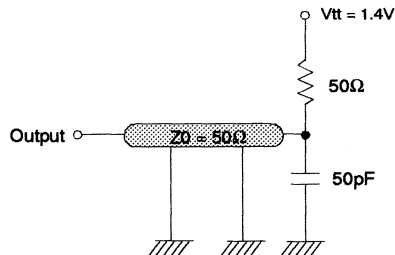
- Notes :** 1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Measured with 1 PLL & 3 Drive ICs.

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3	2			ea	4
	CAS latency=2	1				

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1, 2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1, 2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(t_r \& t_f) = 1$ ns.If $t_r \& t_f$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3	
	Self refresh	Entry		L									3	
		Exit	L	H	L	H	H	H	X	X			3	
					H	X	X	X					3	
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable										H		4,5	
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable										H		4,5	
Burst stop			H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X		
	All banks									X	H			
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X				
					L	V	V	V						
Precharge power down mode		Entry	H	L	H	X	X	X	X	X				
					L	H	H	H						
		Exit	L	H	H	X	X	X	X					
					L	V	V	V						
DQM			H	X					V	X			7	
No operation command			H	X	H	X	X	X	X	X				
					L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

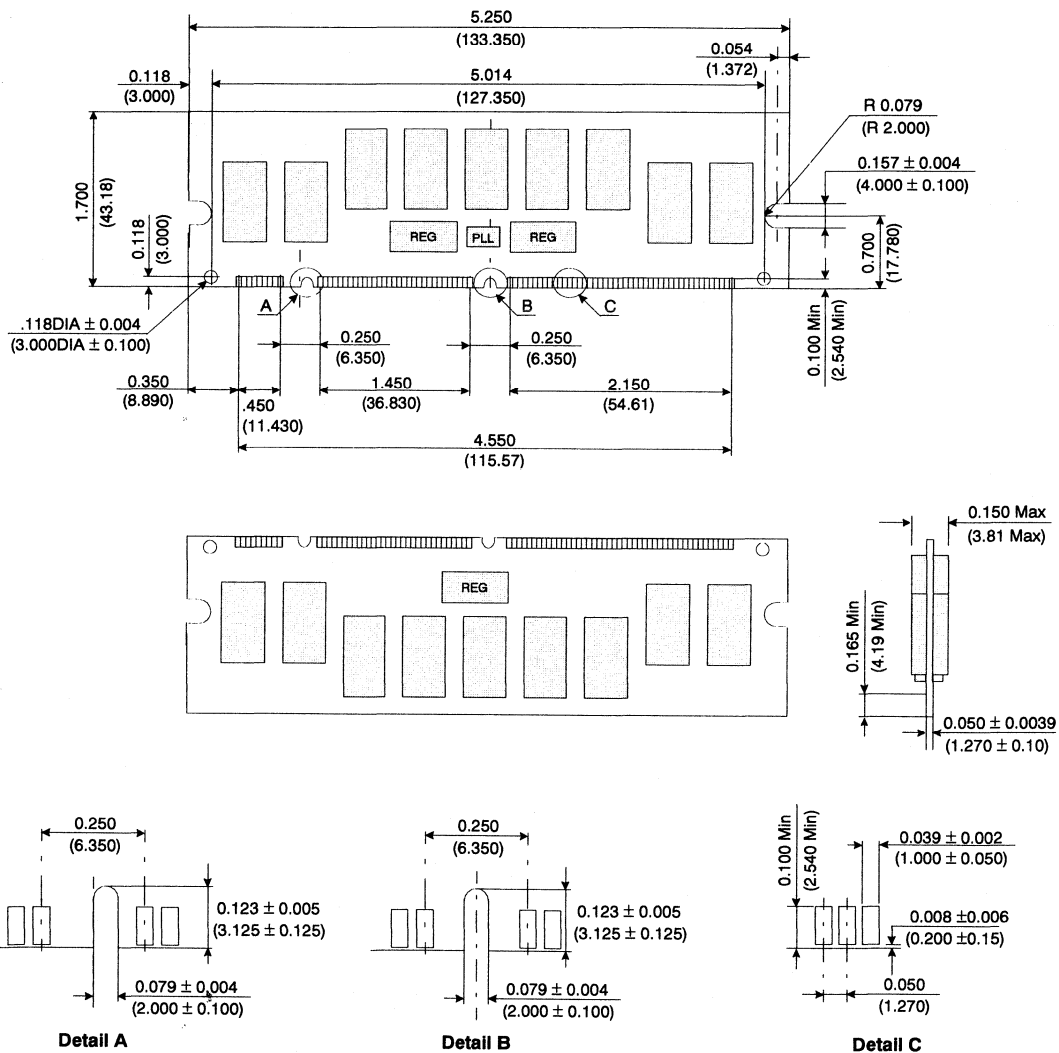
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances :± 0.005(.13) unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832M

M377S3323MT0-C1H/C1L

- Organization : 32MX72
- Composition : 16MX8 *18
- Used component part # : K4S280832M-TC1H/C1L
- # of banks in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On- card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		48h	78h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	3		33h		
80	 Manufacturer part # (Module depth)	3		33h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	M		4Dh		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	0		30h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	0		30h		
92	 Manufacturer revision code (For component)	M-die (1st Gen.)		4Dh		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M377S6428MT3 SDRAM DIMM (Intel 1.2 ver Base)

64Mx72 SDRAM DIMM with PLL & Register based on Stacked 64Mx4, 4Banks, 4K Ref., 3.3V SDRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S6428MT3 is a 64M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S6428MT3 consists of eighteen CMOS Stacked 64Mx4 bit Synchronous DRAMs in two TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S6428MT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S6428MT3-C1H	100MHz (10ns @ CL=2)
M377S6428MT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4 & 8 page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,700mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50		
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51		
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd		
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52		
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC		
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF		
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE		
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss		
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53		
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54		
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55		
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss		
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56		
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57		
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58		
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59		
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	CS3	157	Vdd		
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60		
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61		
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62		
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63		
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss		
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3		
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC		
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0		
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1		
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2		
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd		

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

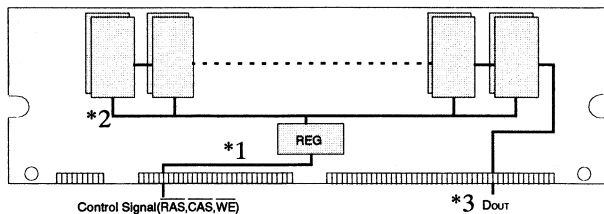
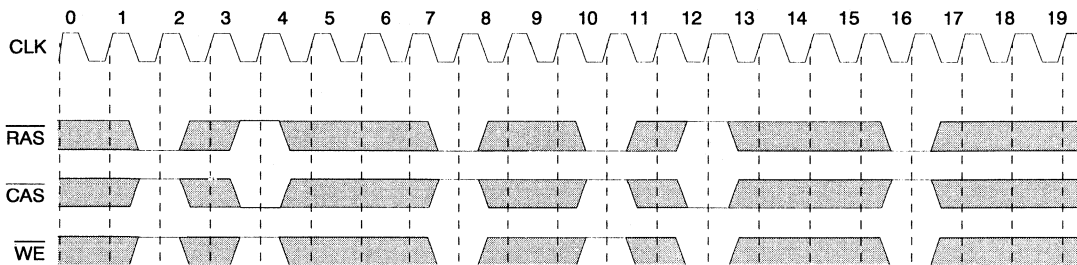
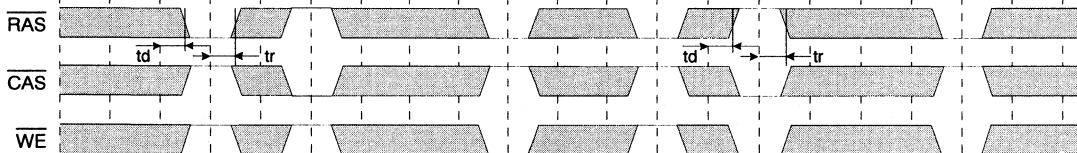
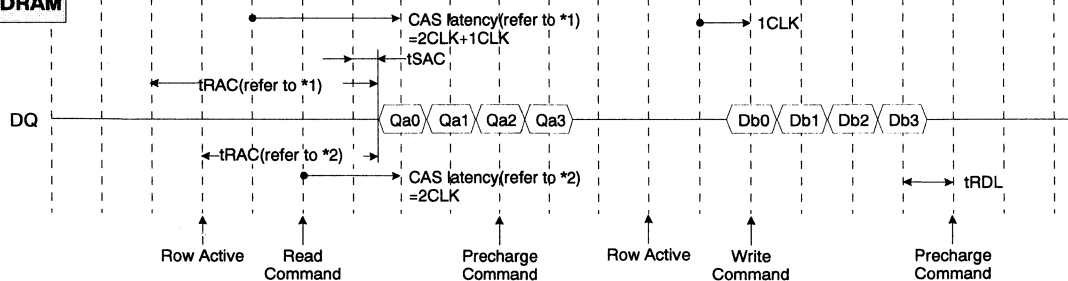
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	P _D	27	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I _{IL}	-3	-	3	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, 0V ≤ V_{OUT} ≤ VDDQ

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C _{IN1}	-	20	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	-	20	pF
Input capacitance (CKE0)	C _{IN3}	-	30	pF
Input capacitance (CLK0)	C _{IN4}	-	26	pF
Input capacitance ($\overline{\text{CS0}}$ ~ $\overline{\text{CS3}}$)	C _{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	20	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	20	pF

DC CHARACTERISTICS

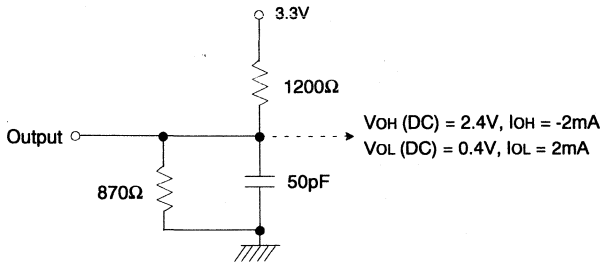
(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version		Unit	Note
				-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IoL = 0 mA		2,450	2,450	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		38		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		38			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		542		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		272			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		182		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		182			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		902		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		632		mA	3
Operating current (Burst mode)	ICC4	IoL = 0mA Page burst 2Banks activated tccd=2CLK	3	2,540	2,540	mA	1
			2	2,540	2,360		
Refresh current	ICC5	trc ≥ trc(min)		3,780		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V		56		mA	3

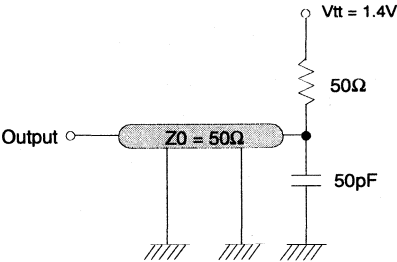
- Notes :**
1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Measured with 1 PLL & 3 Drive ICs.

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tsac		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	toH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3
	Self refresh	L		L	L	H	X	X	X	X	3	
		Exit	L	H	H	H	H	X	X	X	3	
					H	X	X	X	X	X	3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H		4,5
Write & Column Address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks								X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X		
					L	V	V	V				
Exit		L	H	X	X	X	X	X	X			
Precharge power down mode		Entry	H	L	H	X	X	X	X	X		
					L	H	H	H				
		Exit	L	H	H	X	X	X	X			
					L	V	V	V				
DQM		H	X					V	X		7	
No operation command		H	X	H	X	X	X	X	X			
				L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

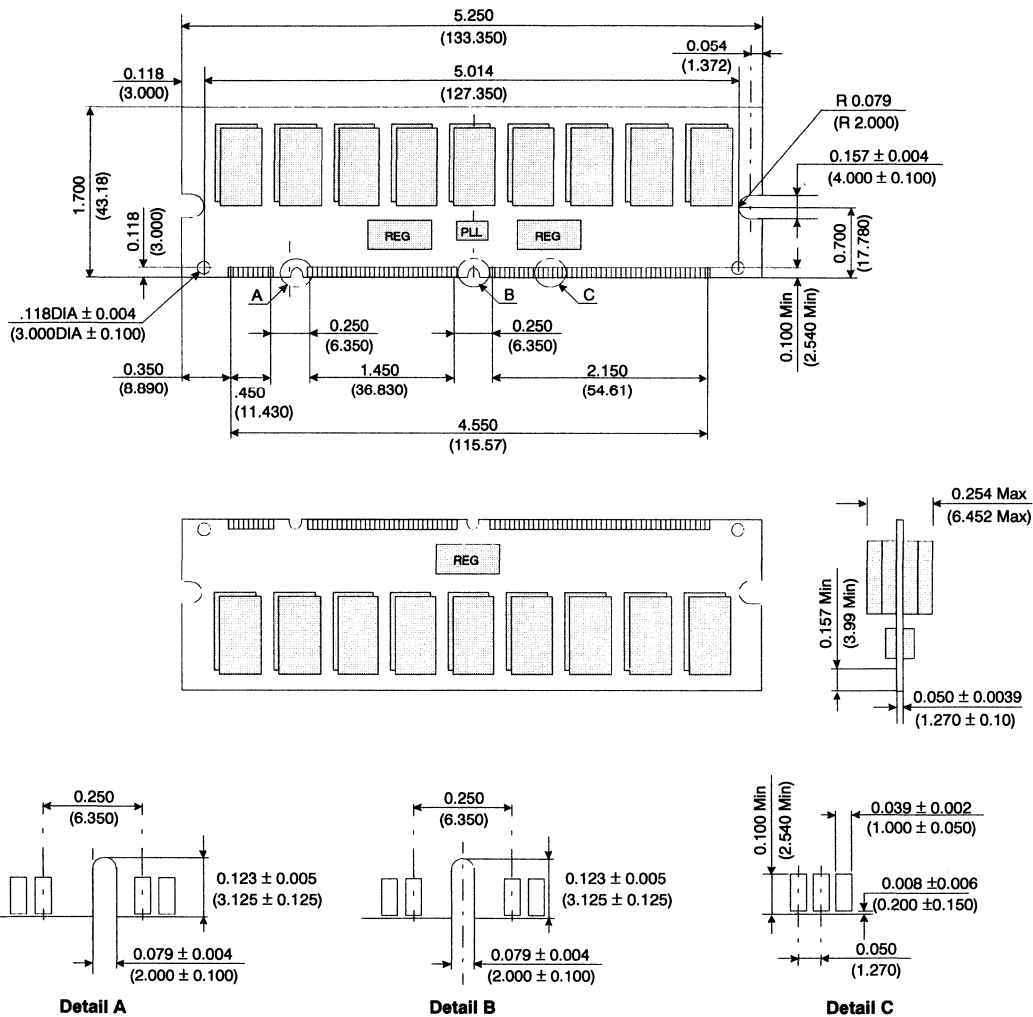
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 64Mx4 SDRAM, TSOP
SDRAM Part No. : K4S560632M

M377S6428MT3-C1H/C1L (1.2ver)

- Organization : 64MX72
- Composition : 64MX4 *18
- Used component part # : K4S560632M-TC1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	11		0Bh		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 & 8 page		0Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 256MB		40h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		E1h	11h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	6		36h		
80	 Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	8		38h		
83	Manufacturer part # (Component revision)	M		4Dh		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	M-die (1st Gen.)		4Dh		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M377S1723AT3 SDRAM DIMM (Intel 1.2 ver Base)

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S1723AT3 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S1723AT3 consists of nine CMOS 16Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S1723AT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S1723AT3-C1H	100MHz (10ns @ CL=2)
M377S1723AT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,500mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

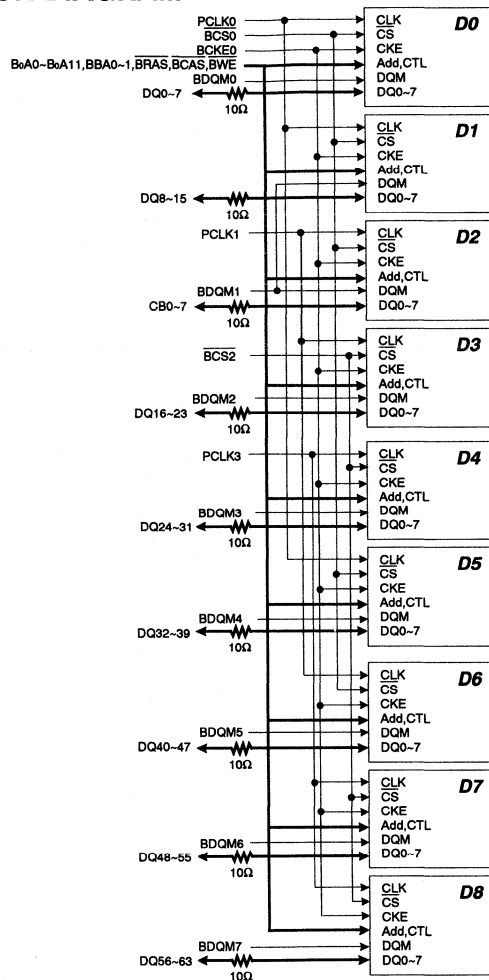
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

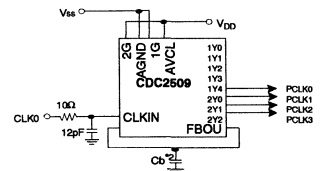
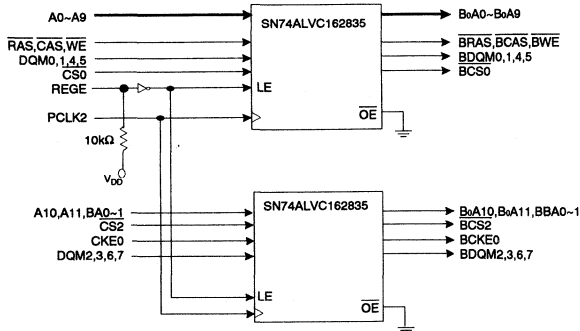
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V _{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V _{DD} /Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM

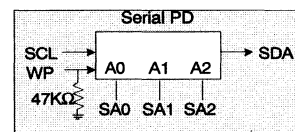


Notes : Address/Control Signals are connected to D2 through 100 ohms resistor.

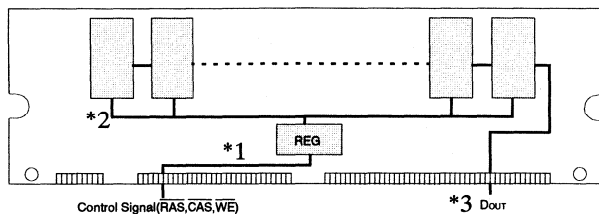
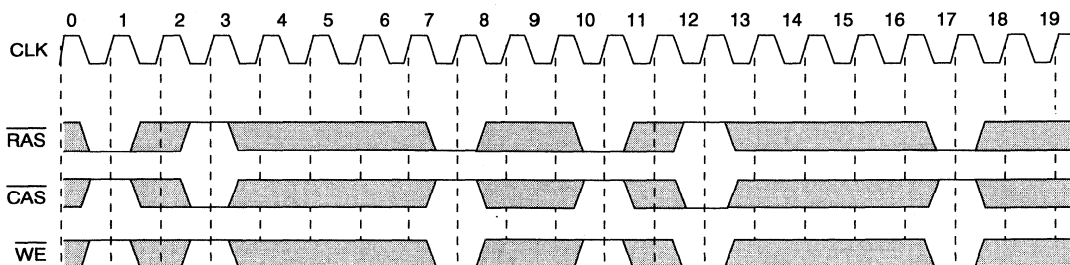
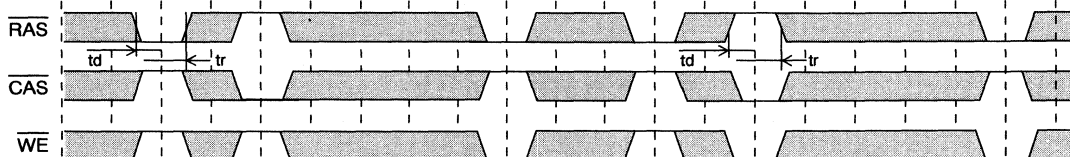
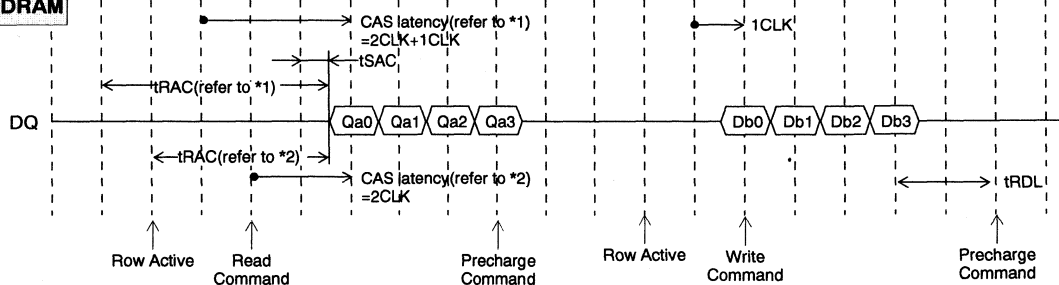


* Note

1. Unused clock termination : 10Ω and 12pF
2. The actual values of Cb will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

td, tr = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C _{IN1}	-	12	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	12	pF
Input capacitance (CKE0)	C _{IN3}	-	12	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance (CS0, CS2)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	12	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	12	pF

DC CHARACTERISTICS

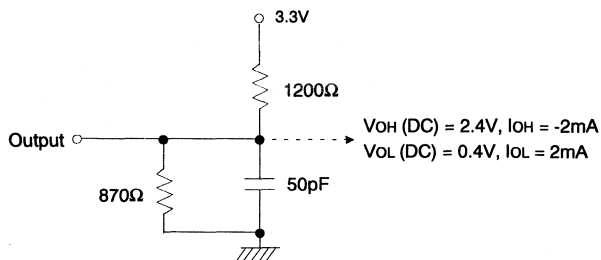
(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,490		mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	359		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	11			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	530		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	65			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	395		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	47			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	620		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	182		mA	3
Operating current (Burst mode)	ICC4	Io = 0mA Page burst 4Banks activated tCCD=2CLK	1,625		mA	1
Refresh current	ICC5	trc ≥ trc(min)	2,390		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	364		mA	3

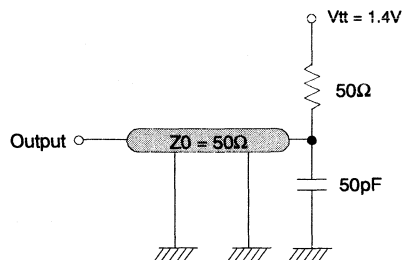
- Notes :**
1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Measured with 1 PLL & 2 Drive ICs.
 4. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -1H/1L, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .
SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3	
	L		X			3							
	Self refresh	Entry	L	H	H	H	X	X			3		
								Exit	H	X	X	3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable									H		4,5	
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable									H		4,5	
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X		
	All banks								X	H			
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

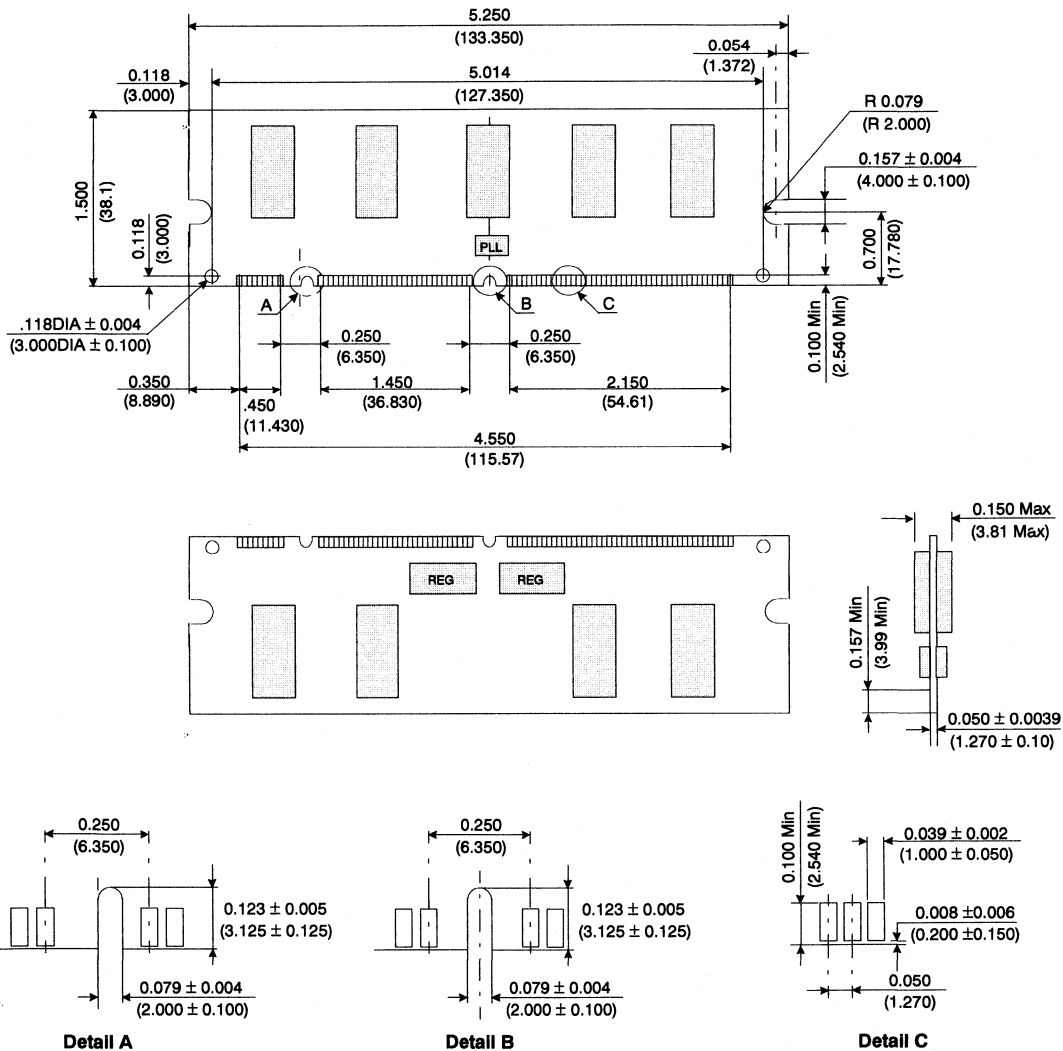
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC100 Registered DIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832A

M377S1723AT3-C1H/C1L (1.2ver)

- Organization : 16MX72
- Composition : 16MX8 *9
- Used component part # : K4S280832A-TC1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1 CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 and full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		47h	77h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	 Manufacturer part # (Module depth)	7		37h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S3320AT3 SDRAM DIMM (Intel 1.2 ver Base)

32Mx72 SDRAM DIMM with PLL & Register based on 32Mx4, 4Banks, 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S3320AT3 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S3320AT3 consists of eighteen CMOS 32Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S3320AT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S3320AT3-C1H	100MHz (10ns @ CL=2)
M377S3320AT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4 & 8 page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,700mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	*CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	*CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

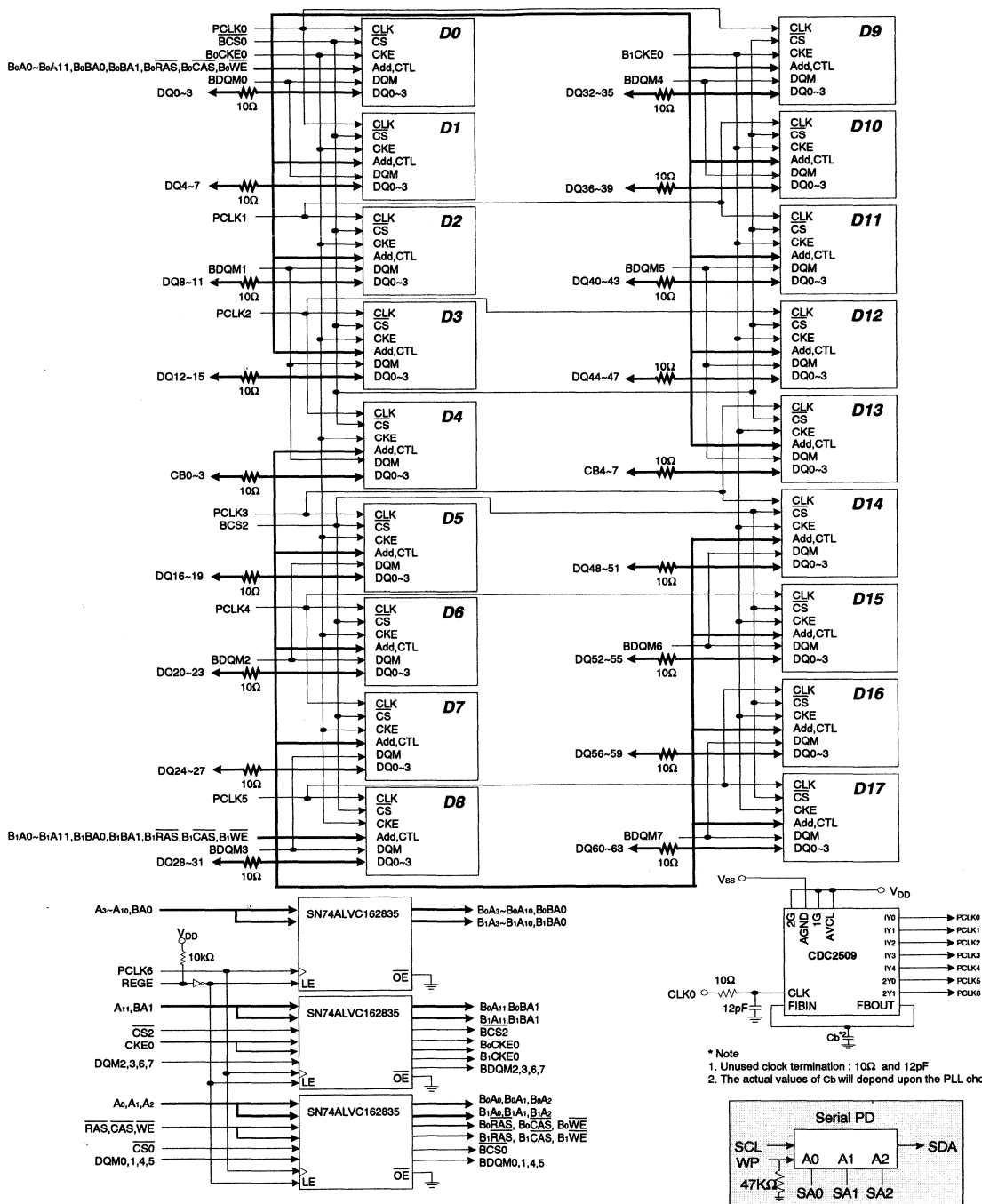
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

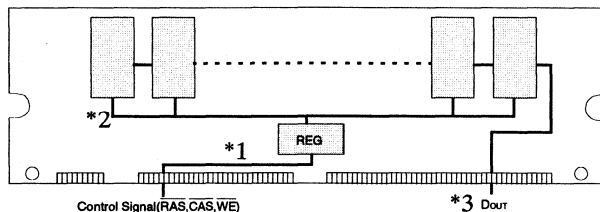
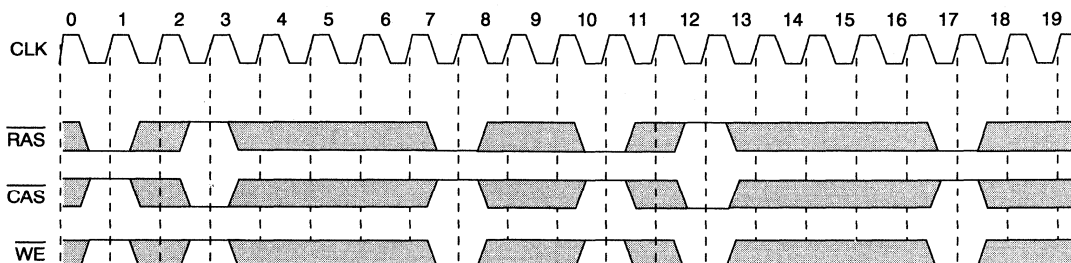
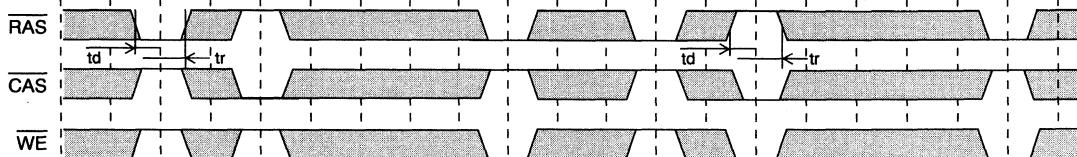
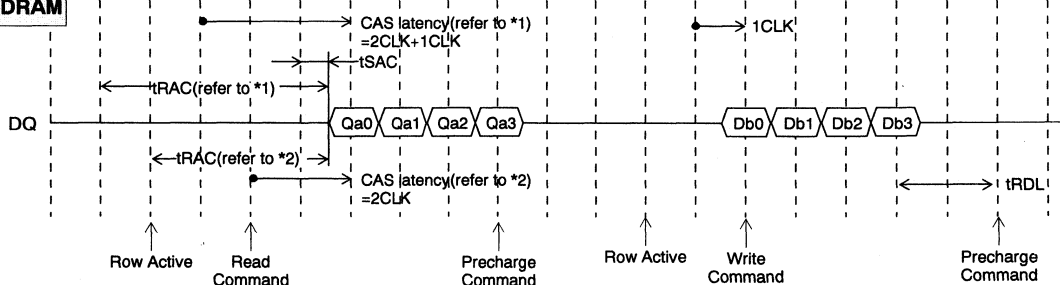
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RAO ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
WE	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V _{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write Protection</i>	WP pin is connected to V _{SS} through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V _{DD} /V _{SS}	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

td, tr = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C _{IN1}	-	19	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	19	pF
Input capacitance (CKE0)	C _{IN3}	-	19	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance (CS0, CS2)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	19	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	12	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	2,480		mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	368		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	20			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS} \geq V_{IH}(\min)$, tcc = 10ns Input signals are changed one time during 20ns	710		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	128			
Active Standby Current in Power-down Mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	440		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	92			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), $\overline{CS} \geq V_{IH}(\min)$, tcc = 10ns Input signals are changed one time during 20ns	890		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	362		mA	3
Operating current (Burst mode)	ICC4	Io = 0mA Page burst 4 Banks activated tccd=2CLK	2,570		mA	1
Refresh current	ICC5	trc ≥ trc(min)	4,280		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	377		mA	3

Notes : 1. Measured with outputs open.

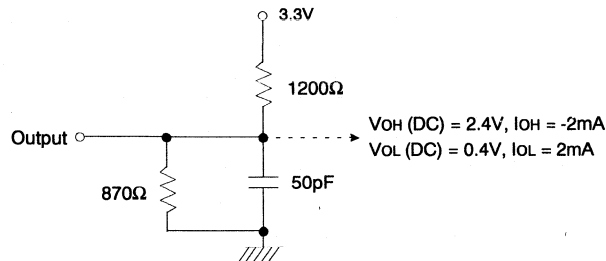
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

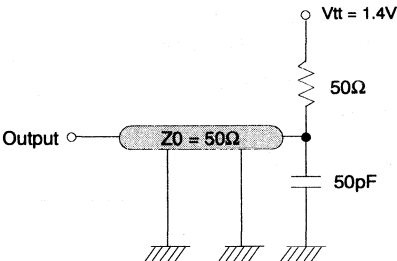
4. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :**
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.
 - 5. For -1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L	L	L	L	H	X	X			3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9, A11)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9, A11)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X	X			
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

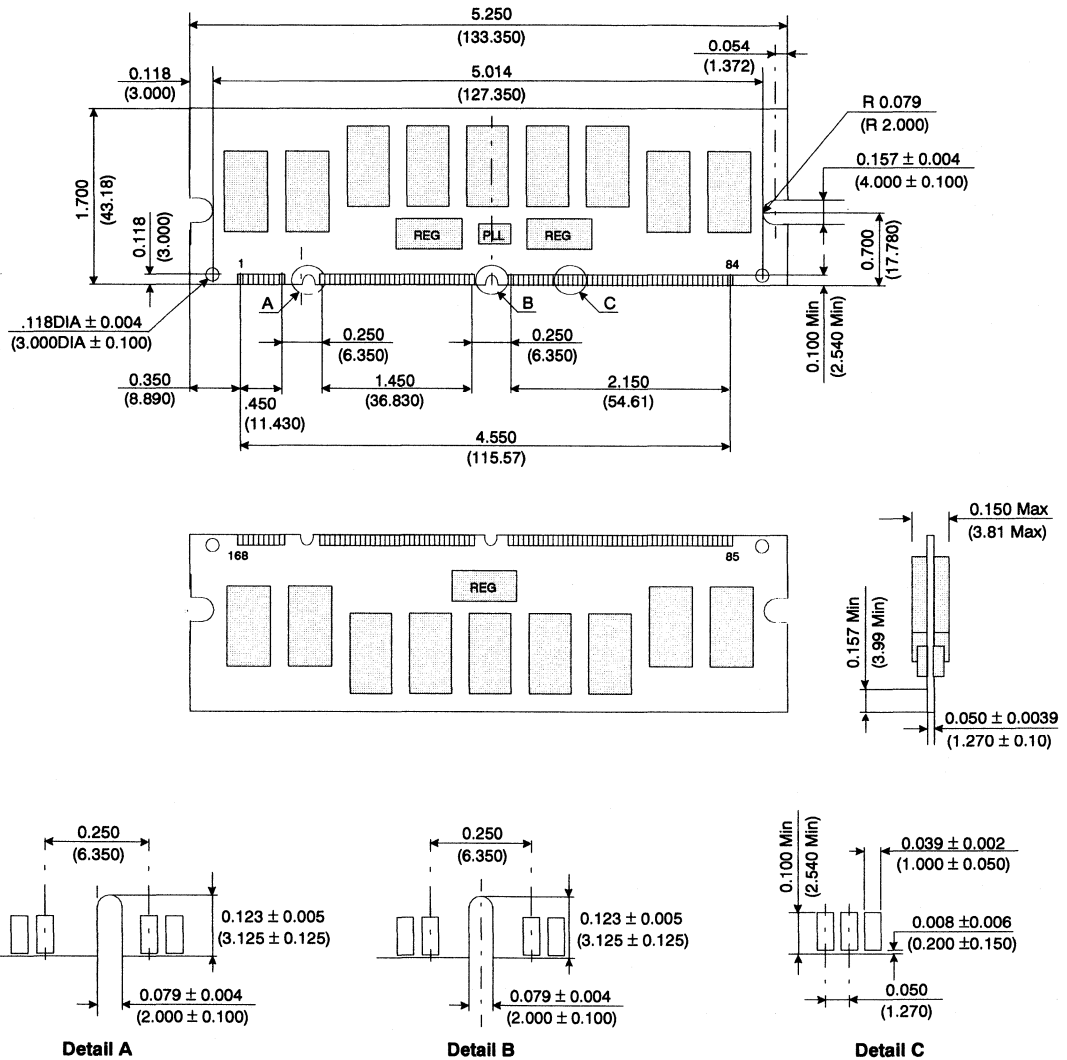
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 32Mx4 SDRAM, TSOP
 SDRAM Part No. : K4S280432A

M377S3320AT3-C1H/C1L (1.2ver)

- Organization : 32MX72
- Composition : 32MX4 *18
- Used component part # : K4S280432A-TC1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	11		0Bh		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 & 8 page		0Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 256MB		40h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		E0h	10h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	3		33h		
80	 Manufacturer part # (Module depth)	3		33h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	0		30h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	A-dle (2ndGen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S3323AT0 SDRAM DIMM (Intel 1.2 ver Base)

32Mx72 SDRAM DIMM with PLL & Register based on 16Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S3323AT0 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S3323AT0 consists of eighteen CMOS 16Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S3323AT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock-cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S3323AT0-C1H	100MHz (10ns) @CL=2
M377S3323AT0-C1L	100MHz (10ns) @CL=3

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

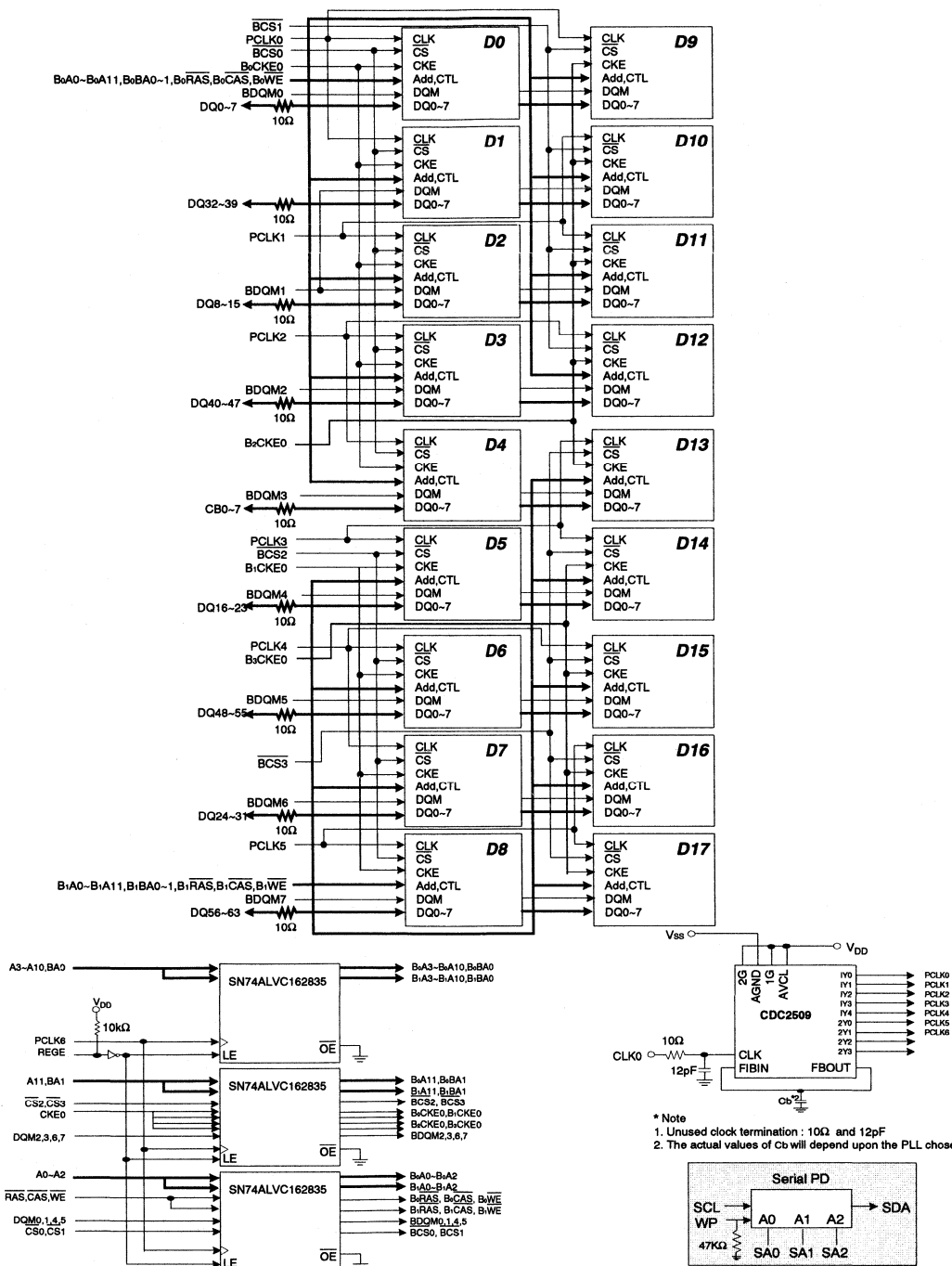
** These pins should be NC in the system which does not support SPD.

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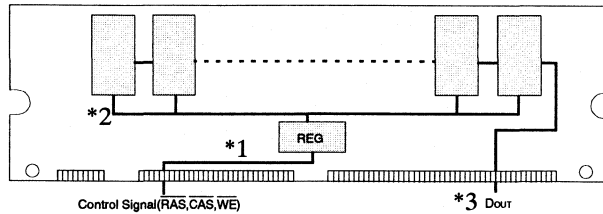
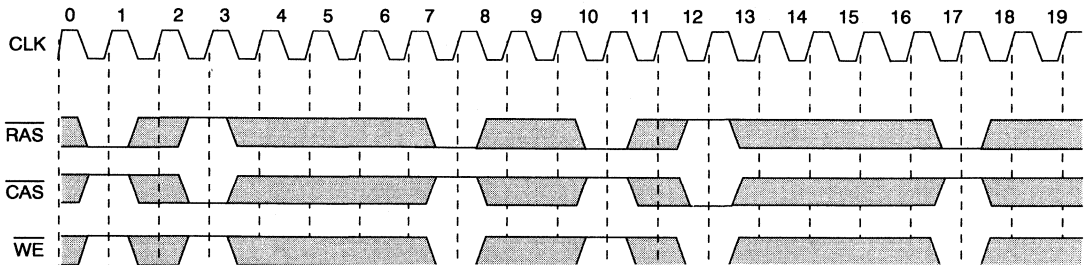
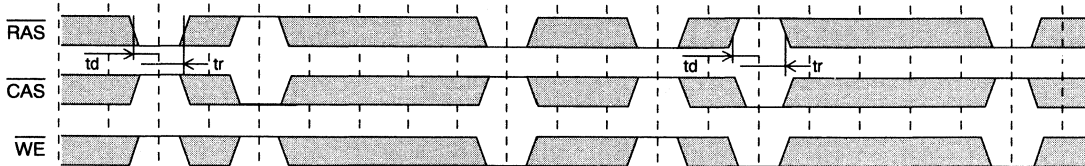
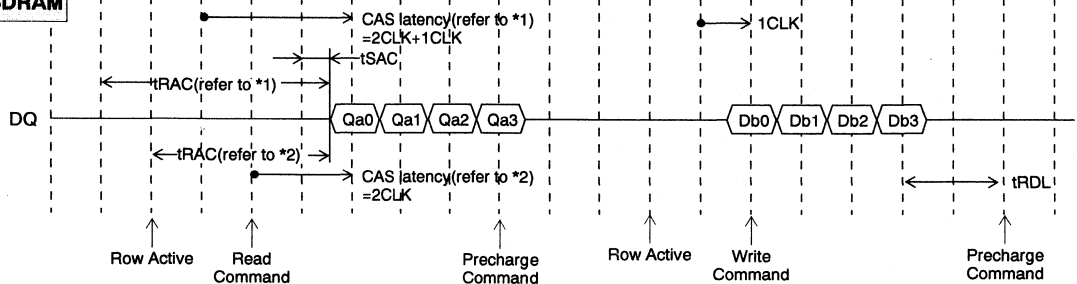
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System Clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip Select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock Enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank Select Address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row Address Strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column Address Strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write Enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data Input/Output Mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data Input/Output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write Protection</i>	WP pin is connected to Vcc. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power Supply/Ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

td, tr = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	μA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁)	C _{IN1}	-	19	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	19	pF
Input capacitance (CKE0)	C _{IN3}	-	33	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance ($\overline{\text{CS0}}$ ~ $\overline{\text{CS3}}$)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	19	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	19	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,760		mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	368		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	20			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, tcc = 10ns Input signals are changed one time during 20ns	710		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	128			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	440		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	92			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, tcc = 10ns Input signals are changed one time during 20ns	890		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	362		mA	3
Operating current (Burst mode)	ICC4	Io = 0mA Page Burst 4 Banks activated tccd=2CLK	1,895		mA	1
Refresh current	ICC5	trc ≥ trc(min)	2,660		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	377		mA	3

Notes : 1. Measured with outputs open.

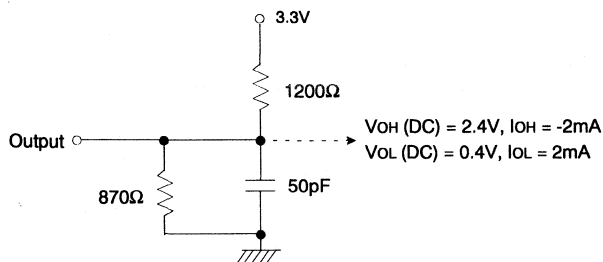
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

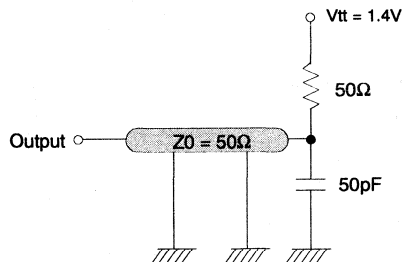
4. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version		Unit	Note
		-1H	-1L		
Row active to row active delay	$t_{RRD}(\text{min})$	20	20	ns	1
RAS to CAS delay	$t_{RCD}(\text{min})$	20	20	ns	1
Row precharge time	$t_{RP}(\text{min})$	20	20	ns	1
Row active time	$t_{RAS}(\text{min})$	50	50	ns	1
	$t_{RAS}(\text{max})$	100		us	
Row cycle time	$t_{RC}(\text{min})$	70	70	ns	1
Last data in to row precharge	$t_{RDL}(\text{min})$	2		CLK	2,5
Last data in to Active delay	$t_{DAL}(\text{min})$	2 CLK + 20 ns		-	5
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1		CLK	2
Last data in to burst stop	$t_{BDL}(\text{min})$	1		CLK	2
Col. address to col. address delay	$t_{CCD}(\text{min})$	1		CLK	3
Number of valid output data	CAS latency=3	2		ea	4
	CAS latency=2	1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -1H/1L, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .
SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1$ ns.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

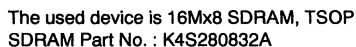
Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Units : Inches (Millimeters)



M377S3323AT0-C1H/C1L

- Organization : 32MX72
- Composition : 16MX8 *18
- Used component part # : K4S280832A-TC1H/C1L
- # of banks in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On- card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		48h	78h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	3		33h		
80	 Manufacturer part # (Module depth)	3		33h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	0		30h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	0		30h		
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S6428AT3 SDRAM DIMM (Intel 1.2 ver Base)

64Mx72 SDRAM DIMM with PLL & Register based on Stacked 64Mx4, 4Banks, 4K Ref., 3.3V SDRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S6428AT3 is a 64M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S6428AT3 consists of eighteen CMOS Stacked 64Mx4 bit Synchronous DRAMs in two TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S6428AT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S6428AT3-C1H	100MHz (10ns @ CL=2)
M377S6428AT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4 & 8 page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,700mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

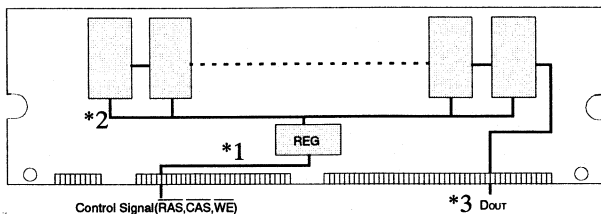
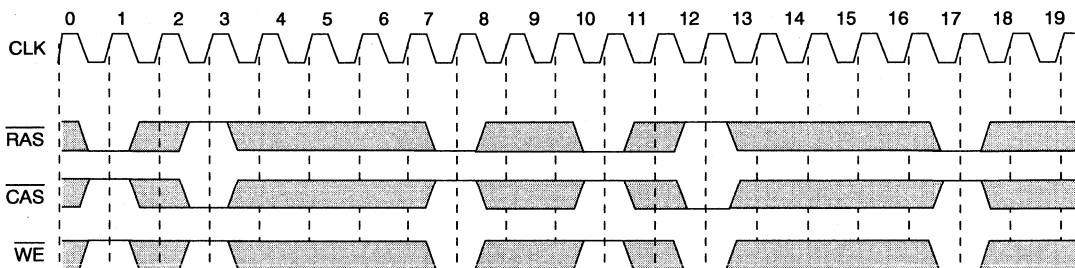
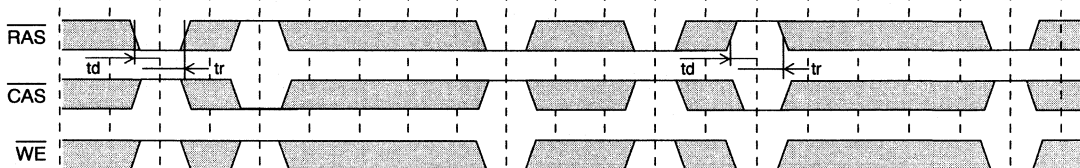
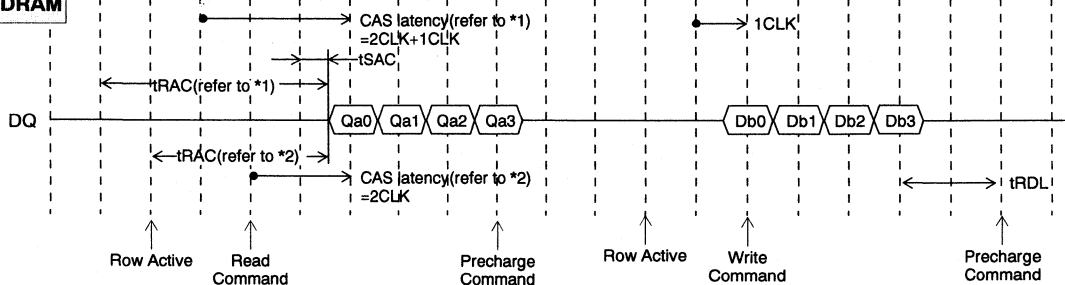
* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

[illegible]

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

td, tr = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	36	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁)	C _{IN1}	-	19	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	19	pF
Input capacitance (CKE0)	C _{IN3}	-	33	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance (CS0 ~ CS3)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	19	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	19	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	19	pF

DC CHARACTERISTICS(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IO = 0 mA	3,020		mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	386		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	38			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, tcc = 10ns Input signals are changed one time during 20ns	1,070		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	254			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	530		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	182			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, tcc = 10ns Input signals are changed one time during 20ns	1,430		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	722		mA	3
Operating current (Burst mode)	ICC4	IO = 0mA Page burst 4Banks activated tccd=2CLK	3,110		mA	1
Refresh current	ICC5	trc ≥ trc(min)	4,820		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	404		mA	3

Notes : 1. Measured with outputs open.

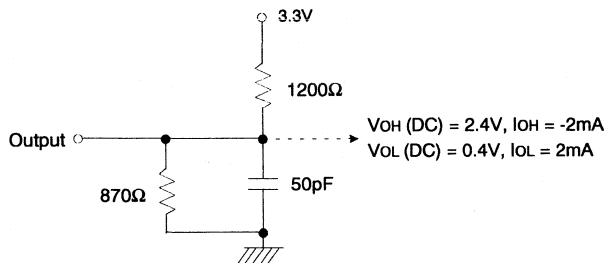
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

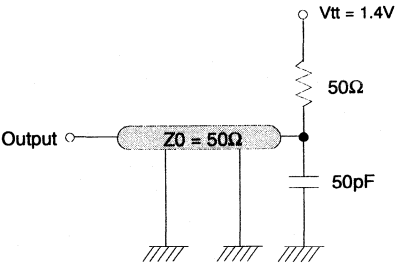
4. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :**
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.
 - 5. For -1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable										H		4,5
Write & Column Address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

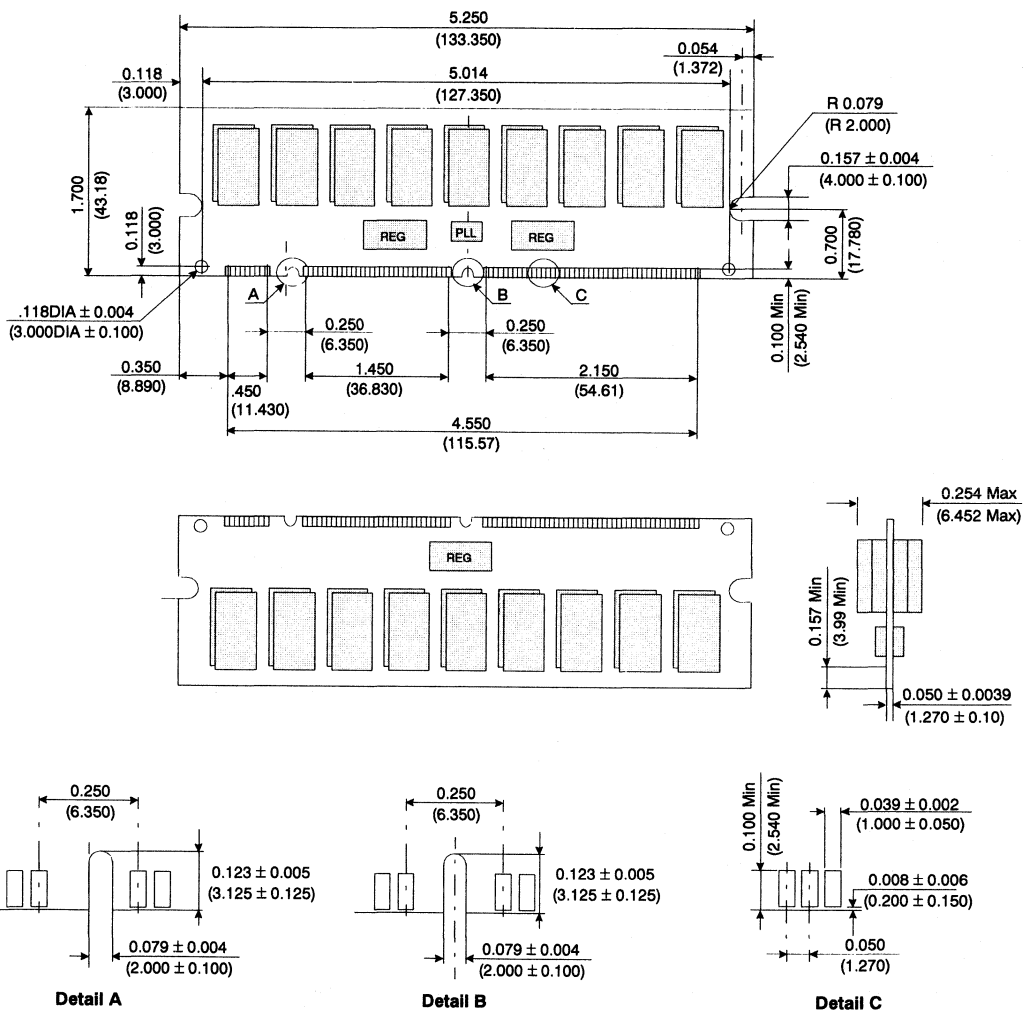
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)

Tolerances : ± 0.005 (.13) unless otherwise specified

The used device is 64Mx4 SDRAM, TSOP
 SDRAM Part No. : K4S560632A

M377S6428AT3-C1H/C1L (1.2ver)

- Organization : 64MX72
- Composition : 64MX4 *18
- Used component part # : K4S560632A-TC1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	11		0Bh		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 & 8 page		0Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 256MB		40h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		E1h	11h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	6		36h		
80	 Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	8		38h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M377S1723BT3 SDRAM DIMM (Intel 1.2 ver Base)

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S1723BT3 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S1723BT3 consists of nine CMOS 16Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S1723BT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S1723BT3-C1H	100MHz (10ns @ CL=2)
M377S1723BT3 -C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,500mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	*CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

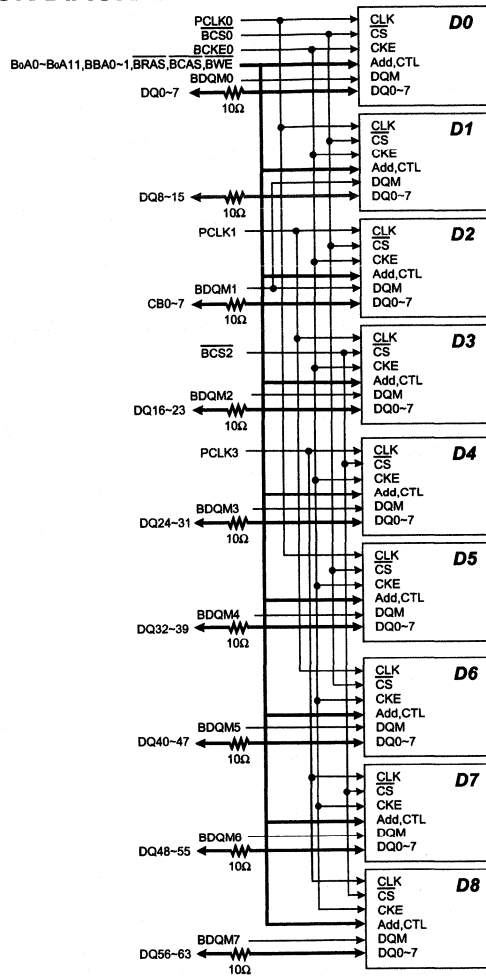
** These pins should be NC in the system which does not support SPD.

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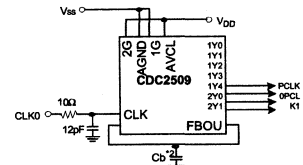
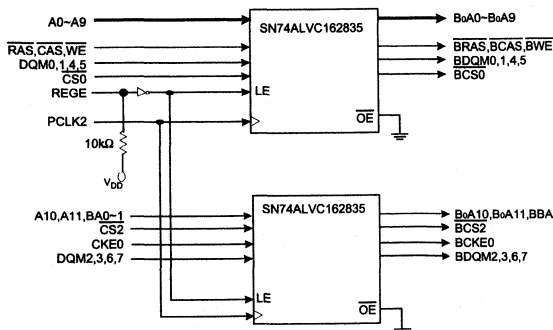
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	Register enable	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V _{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Check bit	Check bits for ECC.
WP	Write protection	WP pin is connected to V _{SS} through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V _{DD} /V _{SS}	Power supply/ground	Power and ground for the input buffers and the core logic.

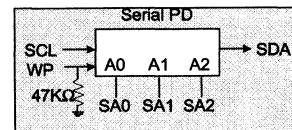
FUNCTIONAL BLOCK DIAGRAM



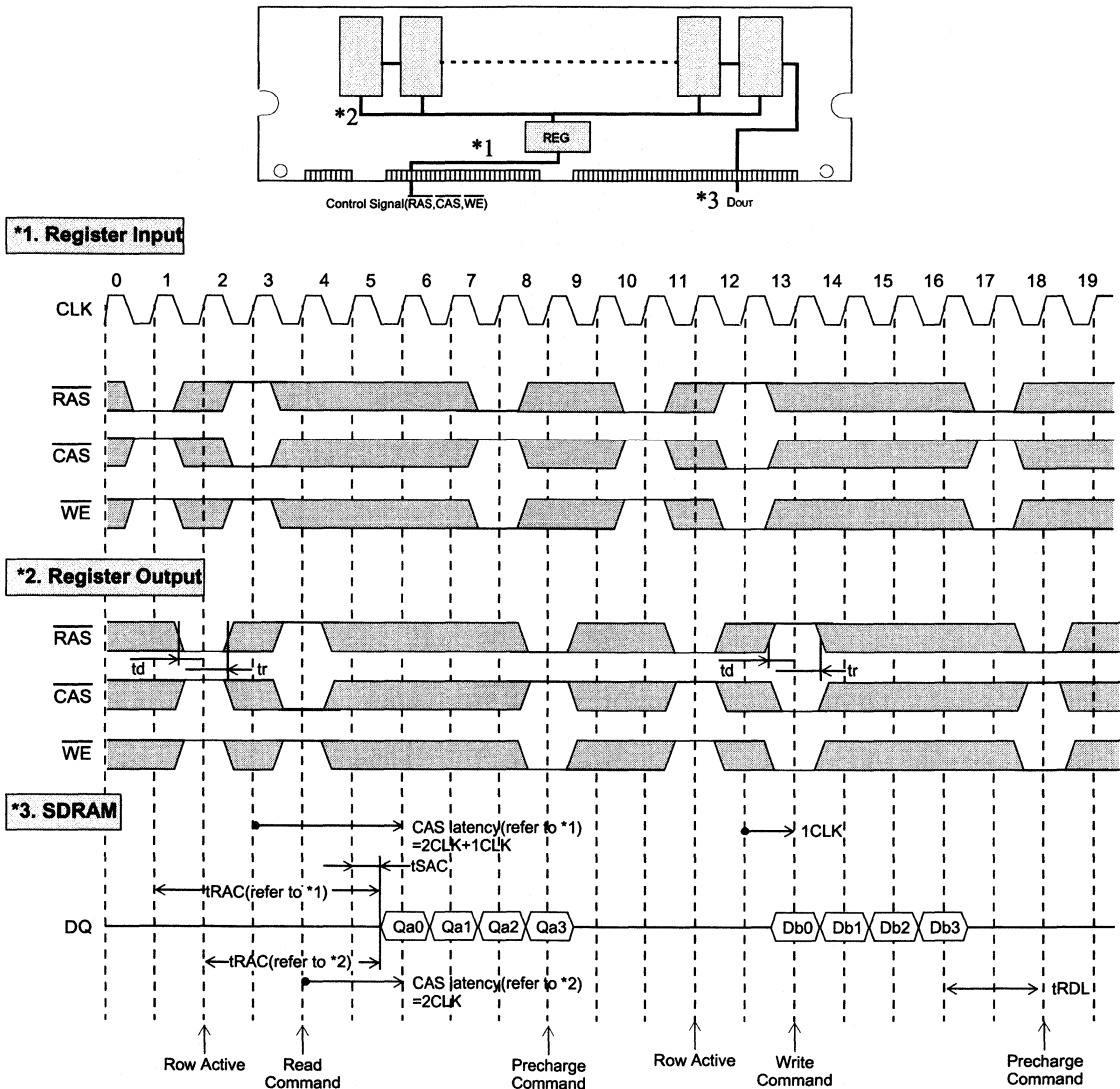
Notes : Address/Control Signals are connected to D2 through 100 ohms resistor.



- * Note
1. Unused clock termination : 100Ω and 12pF
2. The actual values of Cb will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)



td, tr = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C _{IN1}	-	12	pF
Input capacitance (<u>RAS</u> , <u>CAS</u> , <u>WE</u>)	C _{IN2}	-	12	pF
Input capacitance (CKE0)	C _{IN3}	-	12	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance (CS0, CS2)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	12	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,490		mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	359		mA	3
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	11			
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	530		mA	3
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	65			
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	395		mA	3
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	47			
Active standby current in non power-down mode	Icc3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	620		mA	3
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	182		mA	3
Operating current (Burst mode)	Icc4	Io = 0mA Page burst 4Banks activated tccd=2CLK	1,625		mA	1
Refresh current	Icc5	trc ≥ trc(min)	2,390		mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	364		mA	3

Notes : 1. Measured with outputs open.

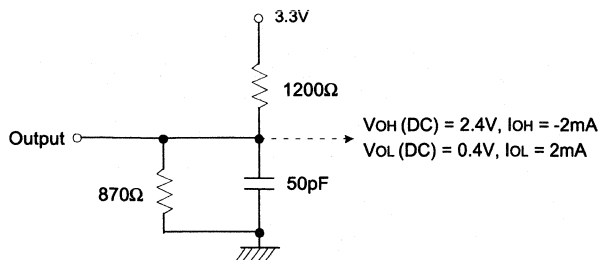
2. Refresh period is 64ms.

3. Measured with 1 PLL & 2 Drive ICs.

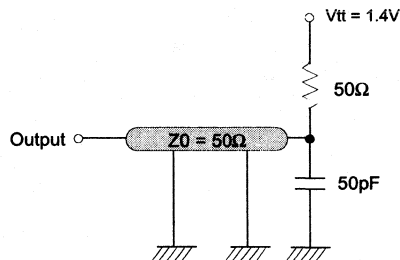
4. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -1H/1L, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .
SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	toH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L							3		
		Exit	L	H	L	H	H	H	X	X	3		
					H	X	X	X			3		
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

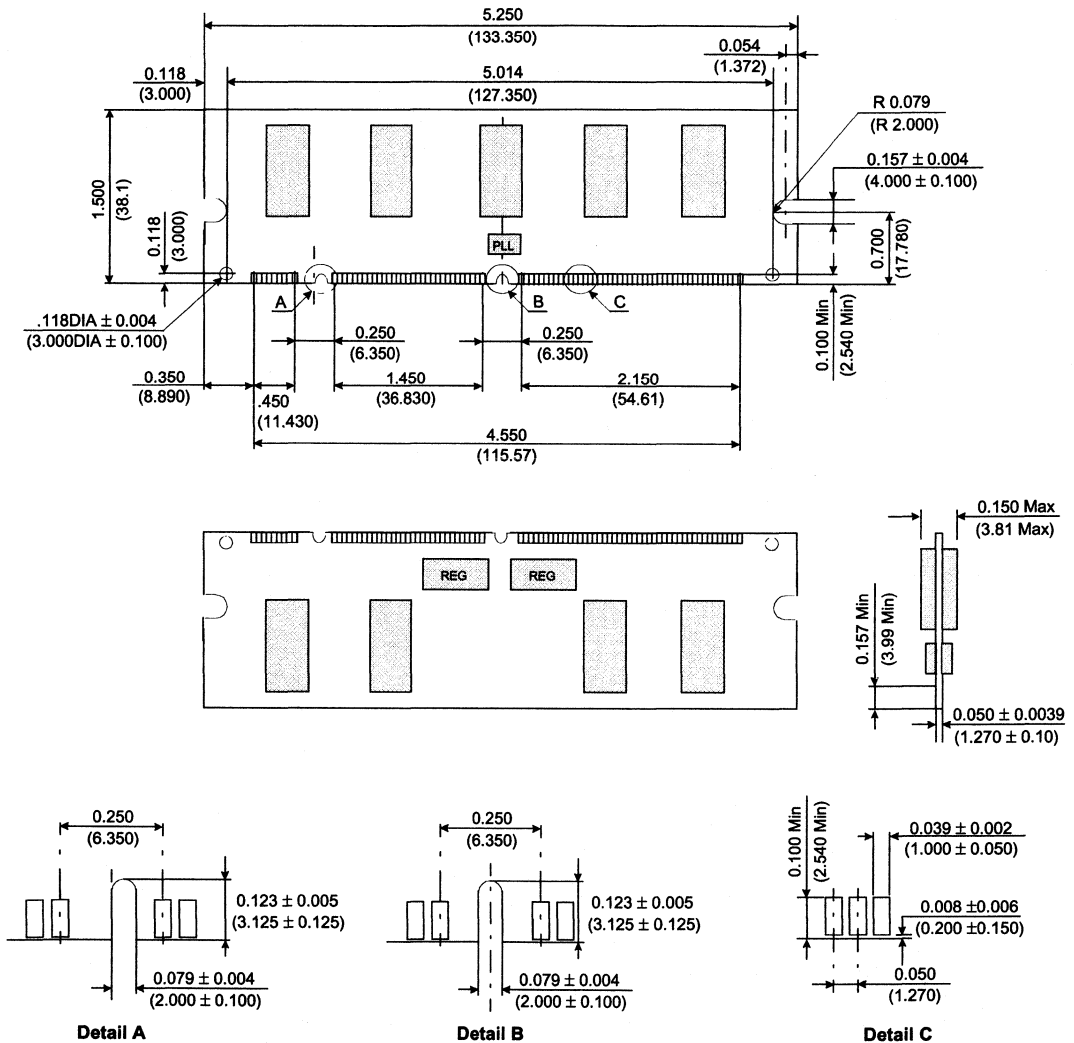
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832B

SERIAL PRESENCE DETECT

PC100 Registered DIMM

M377S1723BT3-C1H/C1L (1.2ver)

- Organization : 16MX72
- Composition : 16MX8 *9
- Used component part # : K4S280832B-TC1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 and full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		47h	77h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	 Manufacturer part # (Module depth)	7		37h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	B		42h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)		42h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S3320BT3 SDRAM DIMM (Intel 1.2 ver Base)

32Mx72 SDRAM DIMM with PLL & Register based on 32Mx4, 4Banks, 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S3320BT3 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S3320BT3 consists of eighteen CMOS 32Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S3320BT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S3320BT3-C1H	100MHz (10ns @ CL=2)
M377S3320BT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4 & 8 page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,700mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V _{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write Protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

Figure 1: Block diagram of the PLL and I/O connections for the SN74ALVC162835.

The diagram illustrates the internal connections and external I/O for three SN74ALVC162835 chips and a CDC2509 PLL chip. The top section shows the PLL configuration, the middle section shows the I/O connections for 18 data buffers (D0-D17), and the bottom section shows the CDC2509 PLL chip and its connections to the SN74ALVC162835 chips.

PLL Configuration:

- Inputs:** A0-A10, BA0, PCLK6, REGE, A11, BA1, CS2, CKE0, DQM2,3,6,7, A0, A1, A2, RAS, CAS, WE, CS0, DQM0,1,4,5.
- Outputs:** B0A0-B0A11, B0BA0, B0BA1, B0RAS, B0CAS, B0WE, BDQM0, B1A0-B1A11, B1BA0, B1BA1, B1RAS, B1CAS, B1WE, BDQM3, B2A0-B2A11, B2BA0, B2BA1, B2RAS, B2CAS, B2WE, BDQM6, B2A0-B2A11, B2BA0, B2BA1, B2RAS, B2CAS, B2WE, BDQM9.

CDC2509 PLL Chip:

- Inputs:** VDD, VSS, AGND, I/O, AVCL, CLK0, FBIN.
- Outputs:** I/O0-I/O6, FBOUT, Cb.

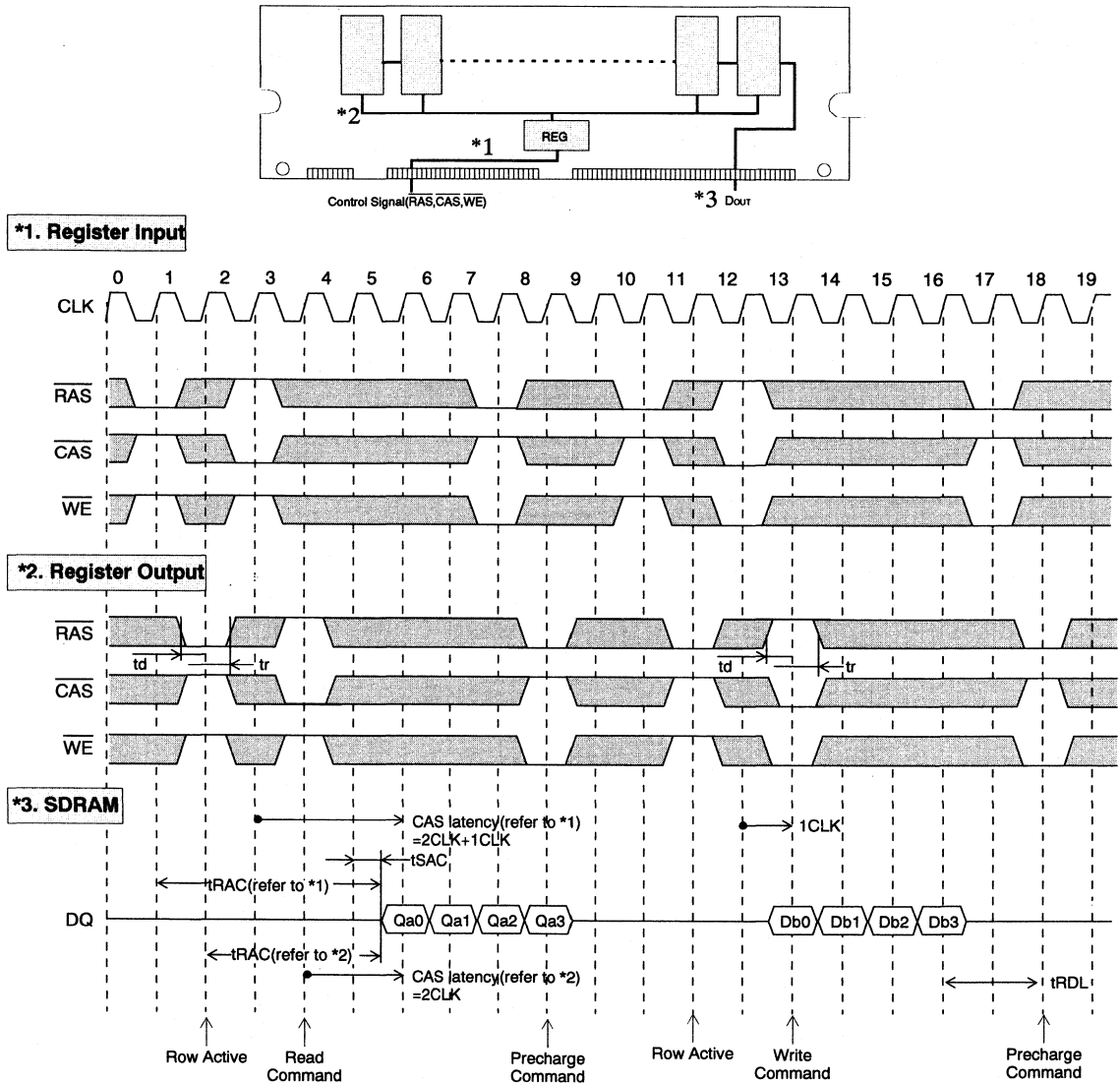
Note:

- Unused clock termination: 10Ω and 12pF
- The actual values of Cb will depend upon the PLL chip

Table 1: Actual values of Cb

PLL Chip	Cb (pF)
SN74ALVC162835	10
SN74ALVC162835	10
SN74ALVC162835	10

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)



t_d , t_r = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C _{IN1}	-	19	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	19	pF
Input capacitance (CKE0)	C _{IN3}	-	19	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance (CS0, CS2)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	19	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	12	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	2,480		mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	368		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	20			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, tcc = 10ns Input signals are changed one time during 20ns	710		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	128			
Active Standby Current in Power-down Mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	440		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	92			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, tcc = 10ns Input signals are changed one time during 20ns	890		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	362		mA	3
Operating current (Burst mode)	ICC4	Io = 0mA Page burst 4 Banks activated tccd=2CLK	2,570		mA	1
Refresh current	ICC5	trc ≥ trc(min)	4,280		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	377		mA	3

Notes : 1. Measured with outputs open.

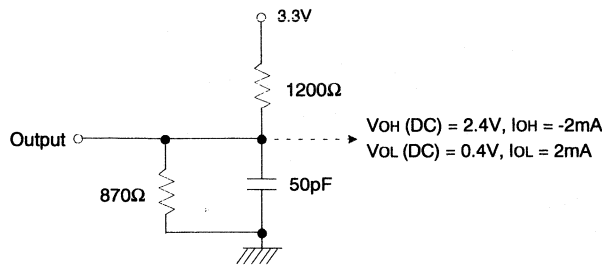
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

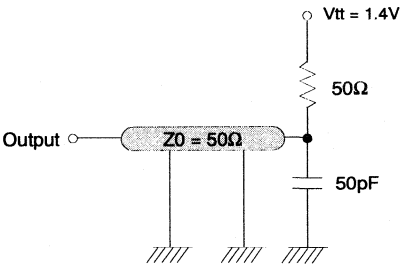
4. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :**
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.
 - 5. For -1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9, A11)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9, A11)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

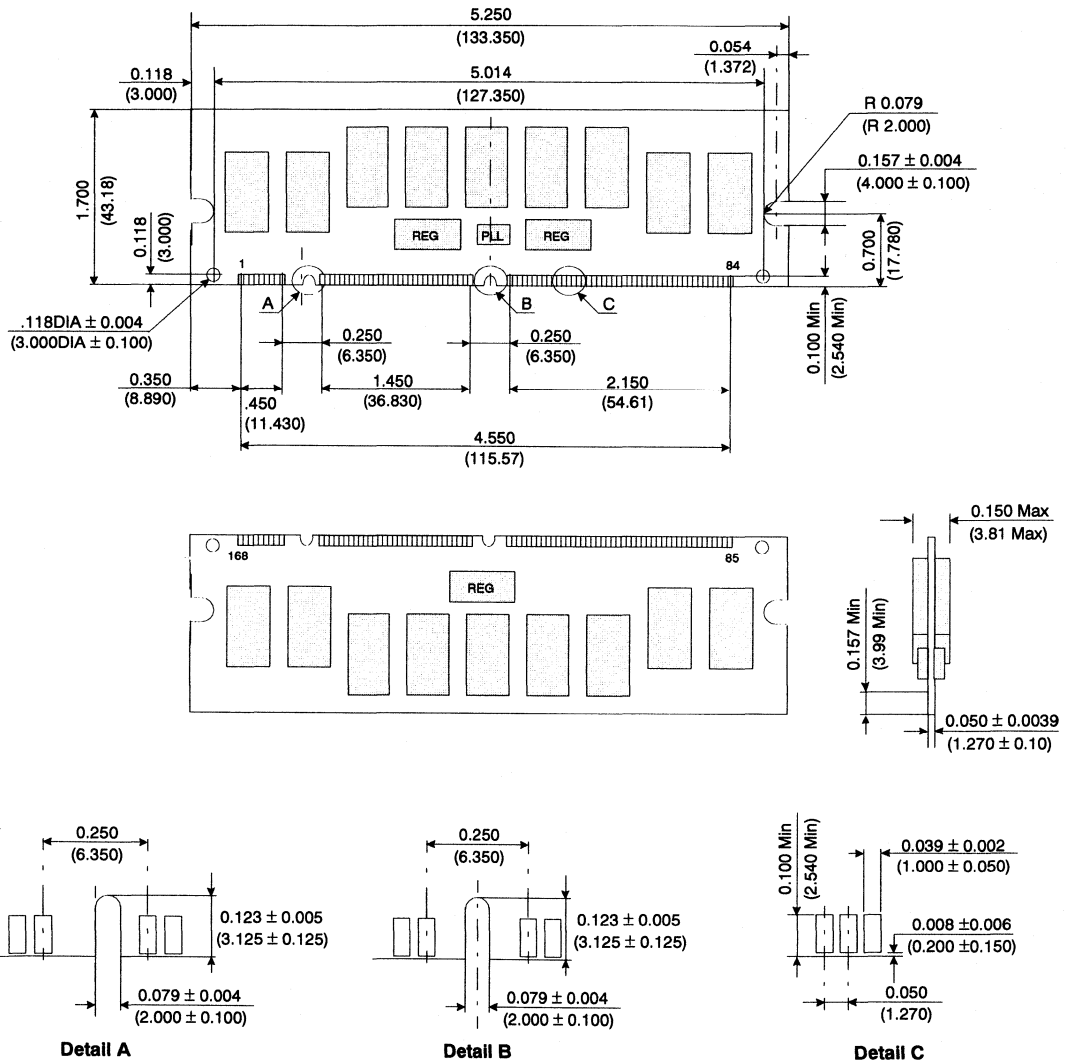
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 32Mx4 SDRAM, TSOP
 SDRAM Part No. : K4S280432B

SERIAL PRESENCE DETECT

PC100 Registered DIMM

M377S3320BT3-C1H/C1L (1.2ver)

- Organization : 32MX72
- Composition : 32MX4 *18
- Used component part # : K4S280432B-TC1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	11		08h		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 & 8 page		0Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 256MB		40h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		E0h	10h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	3		33h		
80	 Manufacturer part # (Module depth)	3		33h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	0		30h		
83	Manufacturer part # (Component revision)	B		42h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)		42h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S3323BT0 SDRAM DIMM (Intel 1.2 ver Base)

32Mx72 SDRAM DIMM with PLL & Register based on 16Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S3323BT0 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S3323BT0 consists of eighteen CMOS 16Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S3323BT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock-cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S3323BT0-C1H	100MHz (10ns) @CL=2
M377S3323BT0-C1L	100MHz (10ns) @CL=3

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,700mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

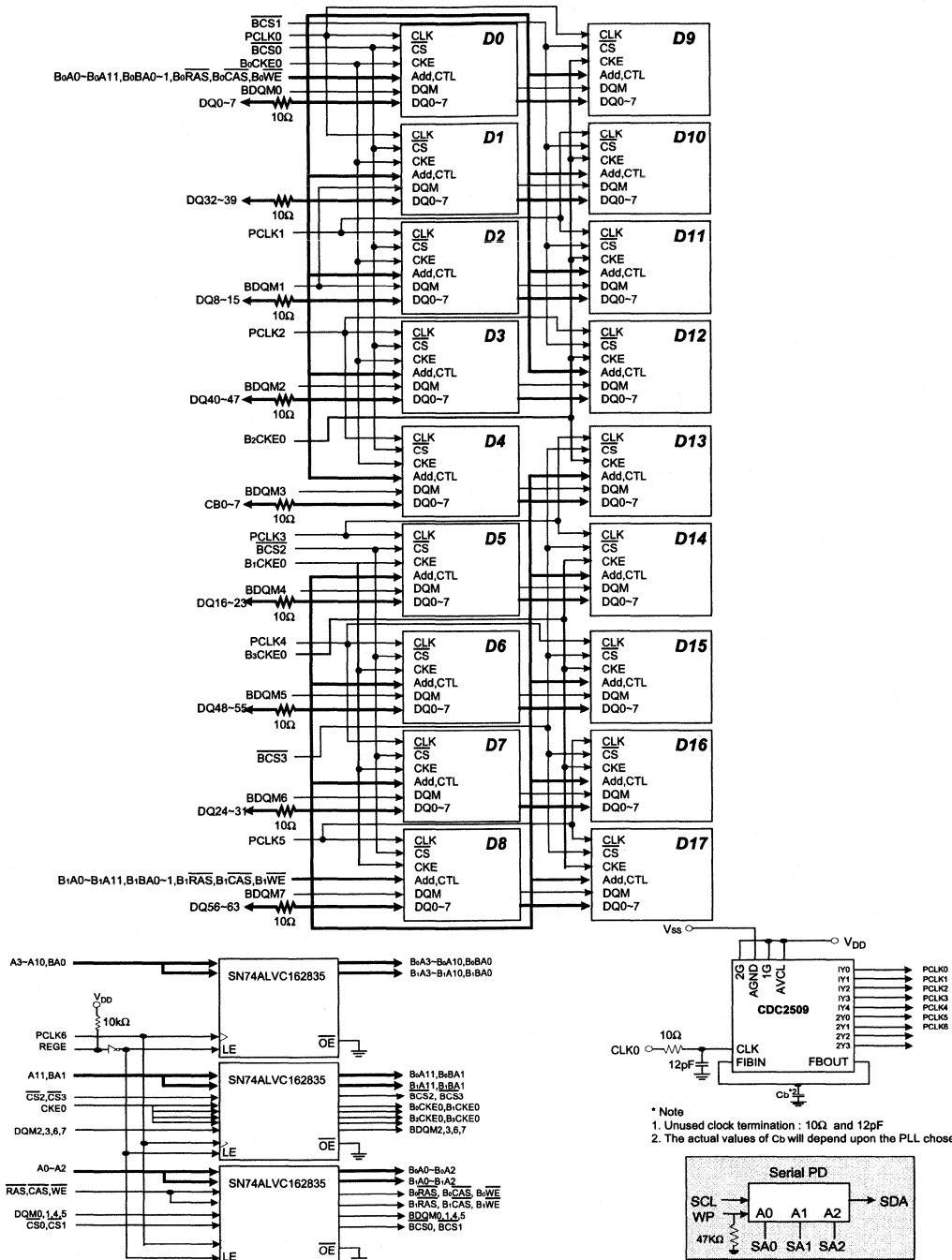
** These pins should be NC in the system which does not support SPD.

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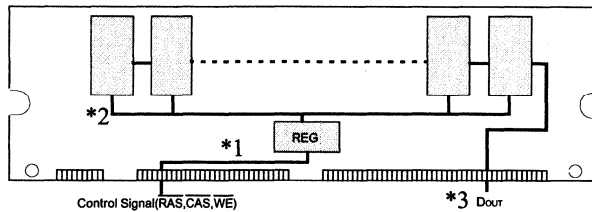
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System Clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip Select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock Enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank Select Address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row Address Strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column Address Strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write Enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM0 ~ 7	<i>Data Input/Output Mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data Input/Output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write Protection</i>	WP pin is connected to Vcc. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power Supply/Ground</i>	Power and ground for the input buffers and the core logic.

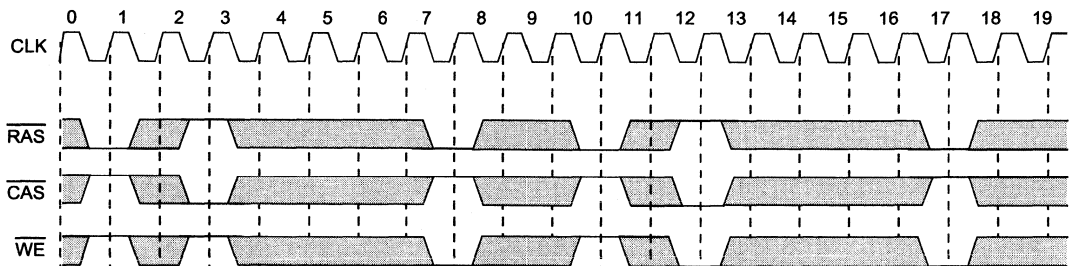
FUNCTIONAL BLOCK DIAGRAM



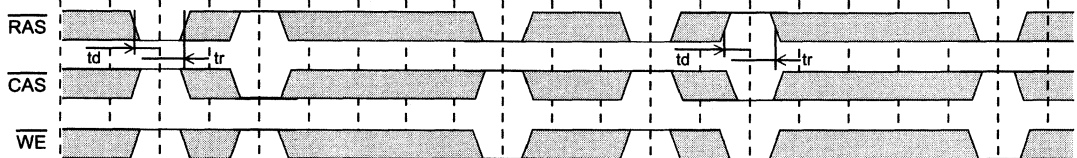
STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)



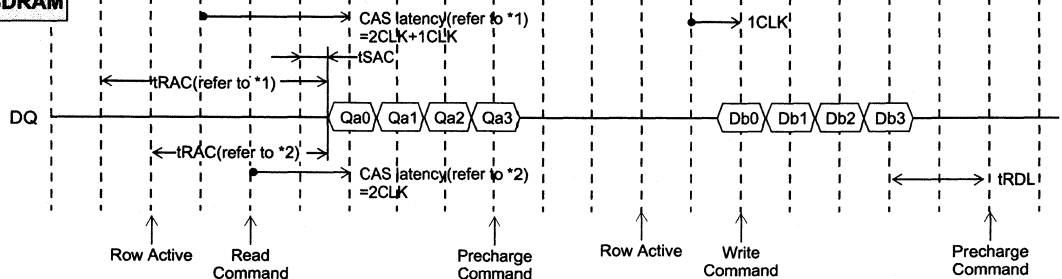
*1. Register Input



*2. Register Output



*3. SDRAM



td, tr = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

 : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _d	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁)	C _{IN1}	-	19	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	19	pF
Input capacitance (CKE0)	C _{IN3}	-	33	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance (CS ₀ ~ CS ₃)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	19	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	19	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	Icc1	Burst length =1 trc ≥ trc(min) Io = 0 mA	1,760		mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	368		mA	3
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	20			
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, tcc = 10ns Input signals are changed one time during 20ns	710		mA	3
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	128			
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	440		mA	3
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	92			
Active standby current in non power-down mode	Icc3N	CKE ≥ VIH(min), $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, tcc = 10ns Input signals are changed one time during 20ns	890		mA	3
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	362		mA	3
Operating current (Burst mode)	Icc4	Io = 0mA Page Burst 4 Banks activated tccd=2CLK	1,895		mA	1
Refresh current	Icc5	trc ≥ trc(min)	2,660		mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	377		mA	3

Notes : 1. Measured with outputs open.

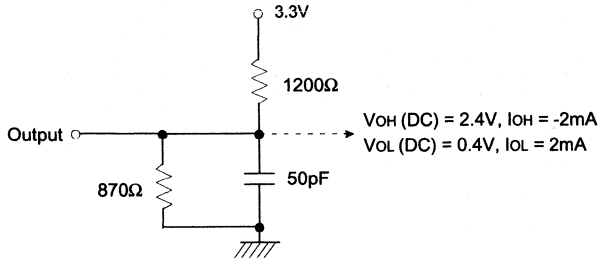
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

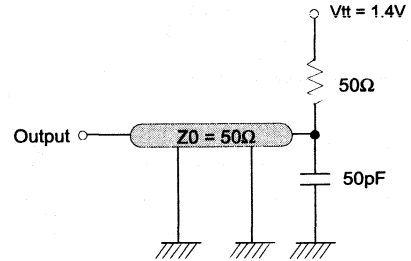
4. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version		Unit	Note
		-1H	-1L		
Row active to row active delay	$t_{RRD}(\min)$	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	$t_{RCD}(\min)$	20	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	20	ns	1
Row active time	$t_{RAS}(\min)$	50	50	ns	1
	$t_{RAS}(\max)$	100		us	
Row cycle time	$t_{RC}(\min)$	70	70	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2		CLK	2,5
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20 ns		-	5
Last data in to new col. address delay	$t_{CDL}(\min)$	1		CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1		CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1		CLK	3
Number of valid output data	CAS latency=3	2		ea	4
	CAS latency=2	1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -1H/1L, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .
SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

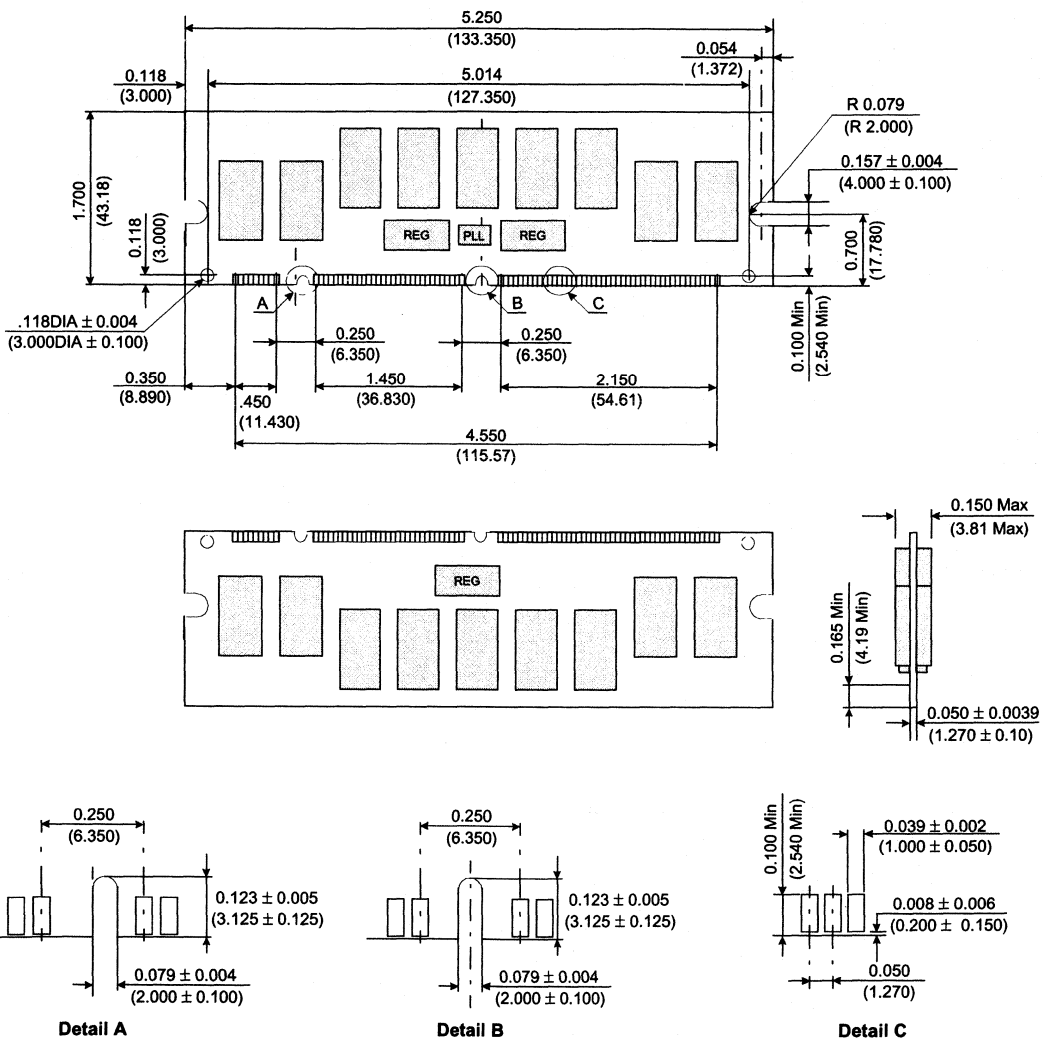
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC100 Registered DIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances :± 0.005(.13) unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832B

M377S3323BT0-C1H/C1L

- Organization : 32MX72
- Composition : 16MX8 *18
- Used component part # : K4S280832B-TC1H/C1L
- # of banks in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On- card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 128MB		20h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		48h	78h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	3		33h		
80	 Manufacturer part # (Module depth)	3		33h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	B		42h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	0		30h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	0		30h		
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)		42h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S6428BT3 SDRAM DIMM (Intel 1.2 ver Base)

64Mx72 SDRAM DIMM with PLL & Register based on Stacked 64Mx4, 4Banks, 4K Ref., 3.3V SDRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S6428BT3 is a 64M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S6428BT3 consists of eighteen CMOS Stacked 64Mx4 bit Synchronous DRAMs in two TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S6428BT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S6428BT3-C1H	100MHz (10ns @ CL=2)
M377S6428BT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4 & 8 page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,700mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

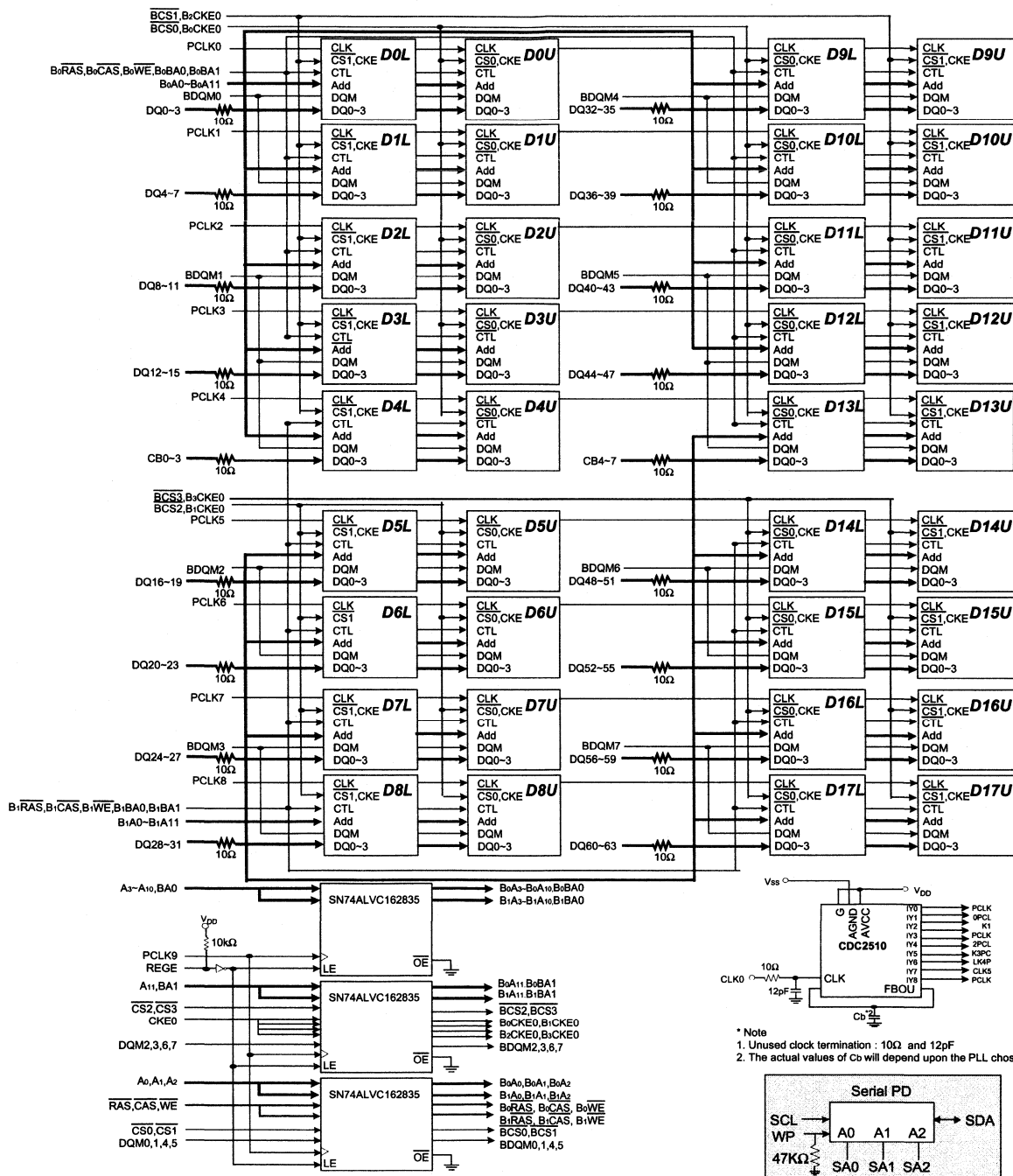
** These pins should be NC in the system which does not support SPD.

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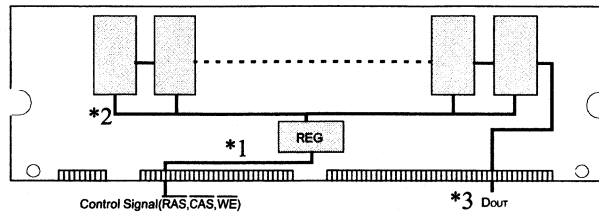
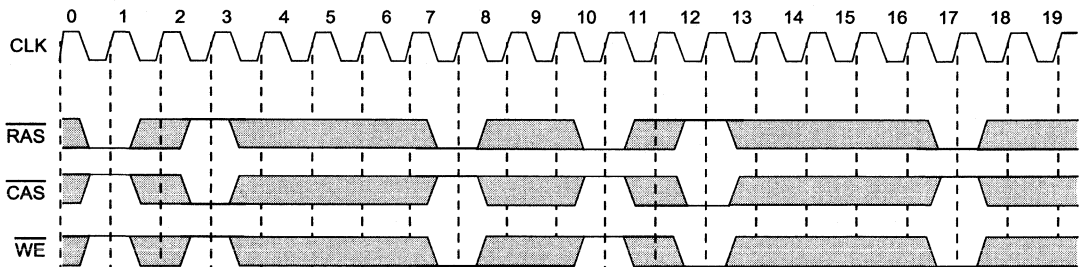
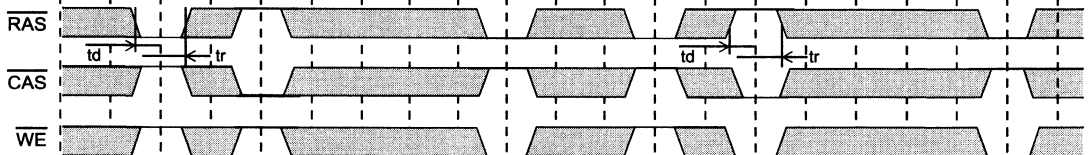
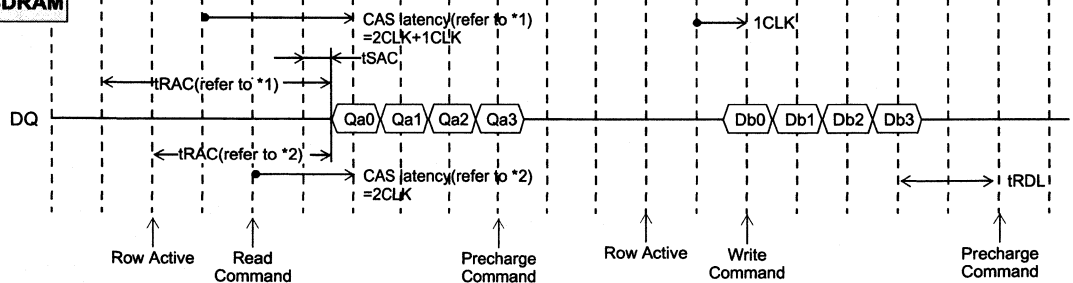
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

td, tr = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. Din is to be issued 1clock after write command in external timing because Din is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	36	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	μA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ VDDQ

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C _{IN1}	-	19	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	19	pF
Input capacitance (CKE0)	C _{IN3}	-	33	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance (CS0 ~ CS3)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	19	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	19	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	19	pF

DC CHARACTERISTICS(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	3,020		mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	386		mA	3
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	38			
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, tcc = 10ns Input signals are changed one time during 20ns	1,070		mA	3
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	254			
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	530		mA	3
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	182			
Active standby current in non power-down mode	Icc3N	CKE ≥ VIH(min), $\overline{\text{CS}} \geq \text{VIH}(\text{min})$, tcc = 10ns Input signals are changed one time during 20ns	1,430		mA	3
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	722		mA	3
Operating current (Burst mode)	Icc4	Io = 0mA Page burst 4Banks activated tccd=2CLK	3,110		mA	1
Refresh current	Icc5	trc ≥ trc(min)	4,820		mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	404		mA	3

Notes : 1. Measured with outputs open.

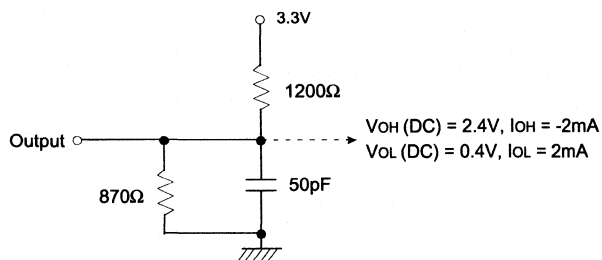
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

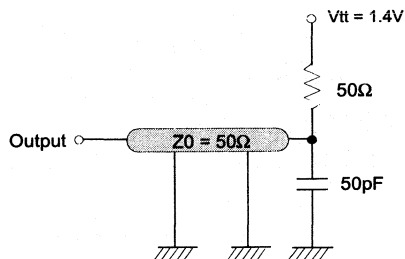
4. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -1H/1L, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .

SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.
 - Assumed input rise and fall time $(t_r \& t_f) = 1$ ns.
If t_r & t_f is longer than 1ns, transient time compensation should be considered,
i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L							3		
		Exit	L	H	L	H	H	H	X	X	3		
					H	X	X	X			3		
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H		4,5	
Write & Column Address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H		4,5	
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

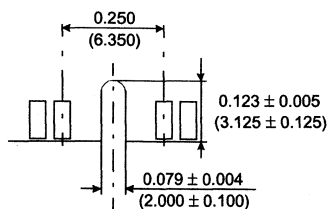
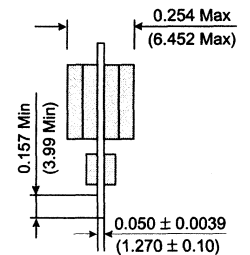
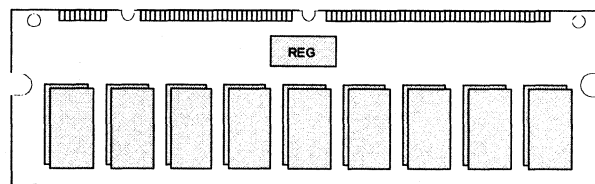
New row active of the associated bank can be issued at trp after the end of burst.

6. Burst stop command is valid at every burst length.

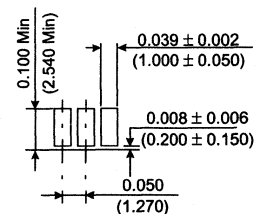
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC100 Registered DIMM

Units : Inches (Millimeters)



Detail B



Detail C

The used device is 64Mx4 SDRAM, TSOP
SDRAM Part No. : K4S560632B

M377S6428BT3-C1H/C1L (1.2ver)

- Organization : 64MX72
- Composition : 64MX4 *18
- Used component part # : K4S560632B-TC1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	12		0Ch		1
4	# of column address on this assembly	11		0Bh		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	15.625us, support self refresh		80h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 & 8 page		0Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 256MB		40h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		E1h	11h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	6		36h		
80	 Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	8		38h		
83	Manufacturer part # (Component revision)	B		42h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)		42h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S3253AT3 SDRAM DIMM (Intel 1.2 ver Base)

32Mx72 SDRAM DIMM with PLL & Register based on 32Mx8, 4Banks 8K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S3253AT3 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S3253AT3 consists of nine CMOS 32Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S3253AT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S3253AT3-C1H	100MHz (10ns @ CL=2)
M377S3253AT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,500mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

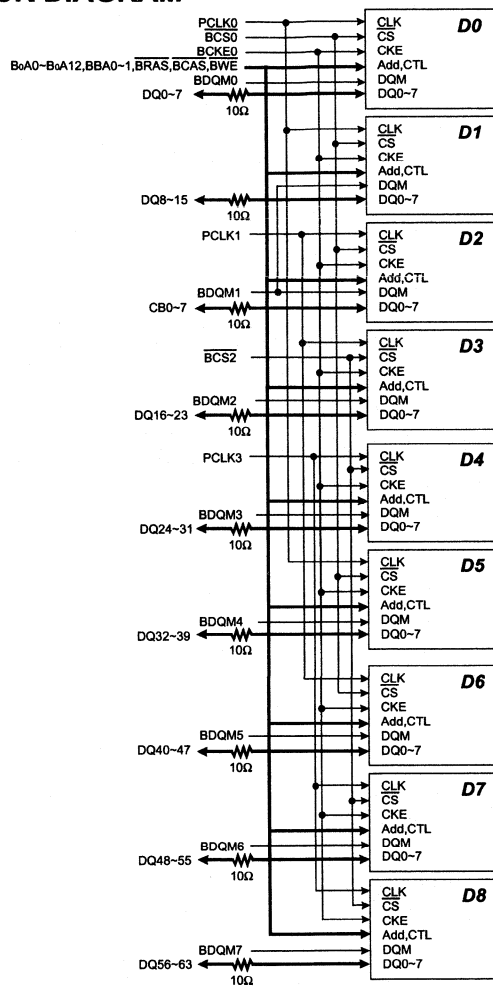
** These pins should be NC in the system which does not support SPD.

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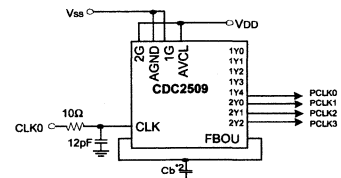
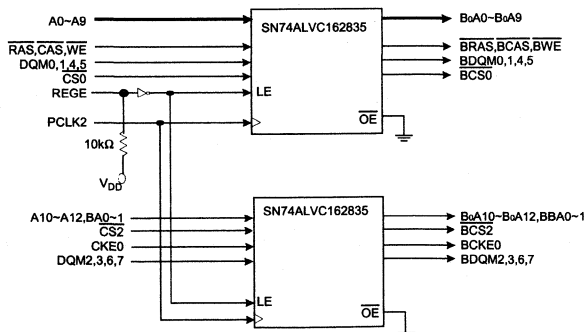
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	Register enable	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Check bit	Check bits for ECC.
WP	Write protection	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM

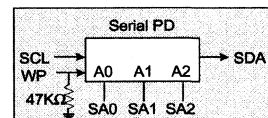


Notes : Address/Control Signals are connected to D2 through 100 ohms resistor.

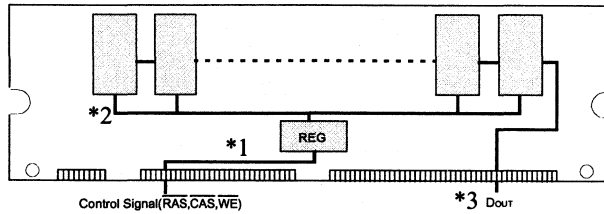
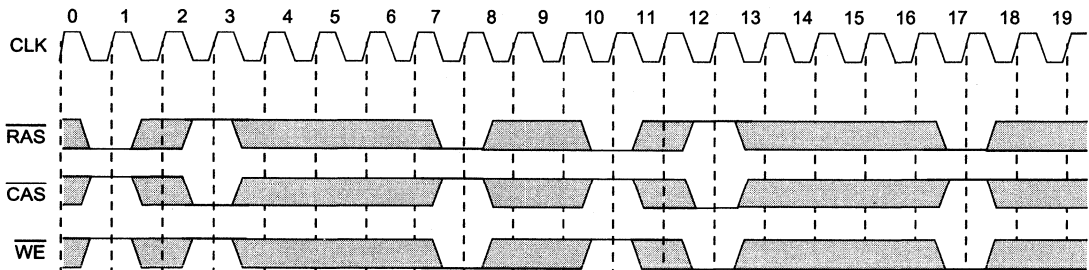
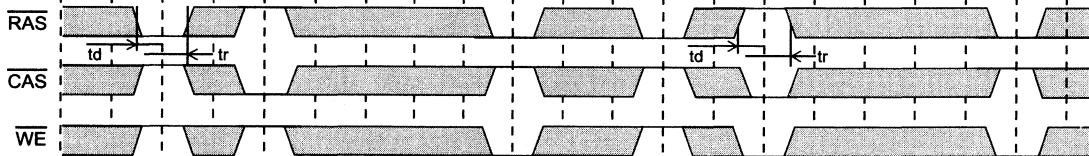
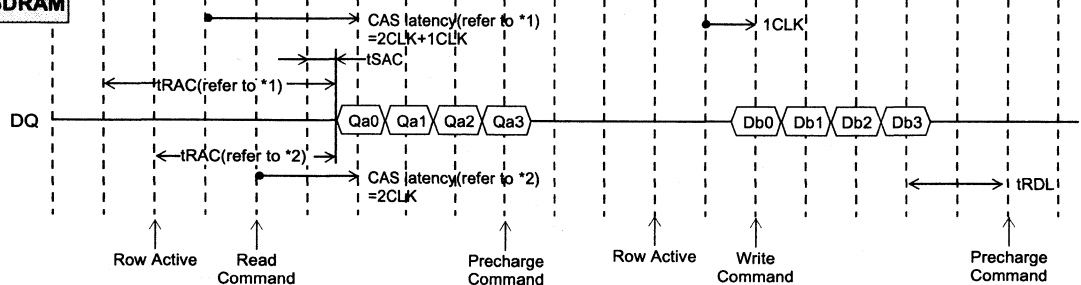


* Note

1. Unused clock termination : 10Ω and 12pF
2. The actual values of Cb will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

t_d , t_r = Delay of register (74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	PD	9	W
Short circuit current	Ios	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	VIH	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	VIL	-0.3	0	0.8	V	2
Output high voltage	VOH	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	VOL	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	ILI	-10	-	10	uA	3

Notes : 1. VIH (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. VIL (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ VIN ≤ VDDQ

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12)	CIN1	-	12	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	CIN2	-	12	pF
Input capacitance (CKE0)	CIN3	-	12	pF
Input capacitance (CLK0)	CIN4	-	12	pF
Input capacitance ($\overline{\text{CS0}}$, $\overline{\text{CS2}}$)	CIN5	-	12	pF
Input capacitance (DQM0 ~ DQM7)	CIN6	-	12	pF
Input capacitance (BA0 ~ BA1)	CIN7	-	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	COU _T	-	12	pF
Data input/output capacitance (CB0 ~ CB7)	COU _{T1}	-	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,490		mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	368		mA	3
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	20			
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 10ns Input signals are changed one time during 20ns	494		mA	3
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	146			
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	404		mA	3
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	56			
Active standby current in non power-down mode	Icc3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 10ns Input signals are changed one time during 20ns	620		mA	3
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	227		mA	3
Operating current (Burst mode)	Icc4	Io = 0mA Page burst 4Banks activated tccd=2CLK	1,535		mA	1
Refresh current	Icc5	trc ≥ trc(min)	2,300		mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	395		mA	3

Notes : 1. Measured with outputs open.

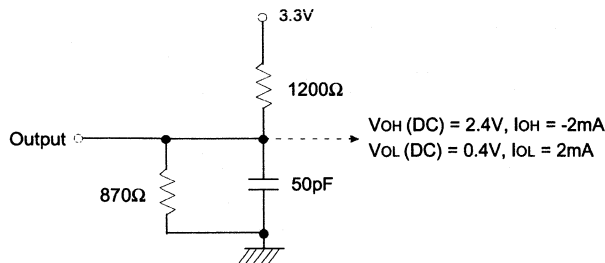
2. Refresh period is 64ms.

3. Measured with 1 PLL & 2 Drive ICs.

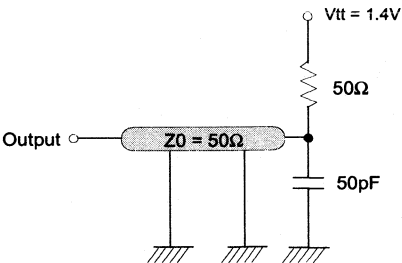
4. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2.5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3	2		ea	4	
	CAS latency=2	1				

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	toH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A12 A9 ~ A10	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

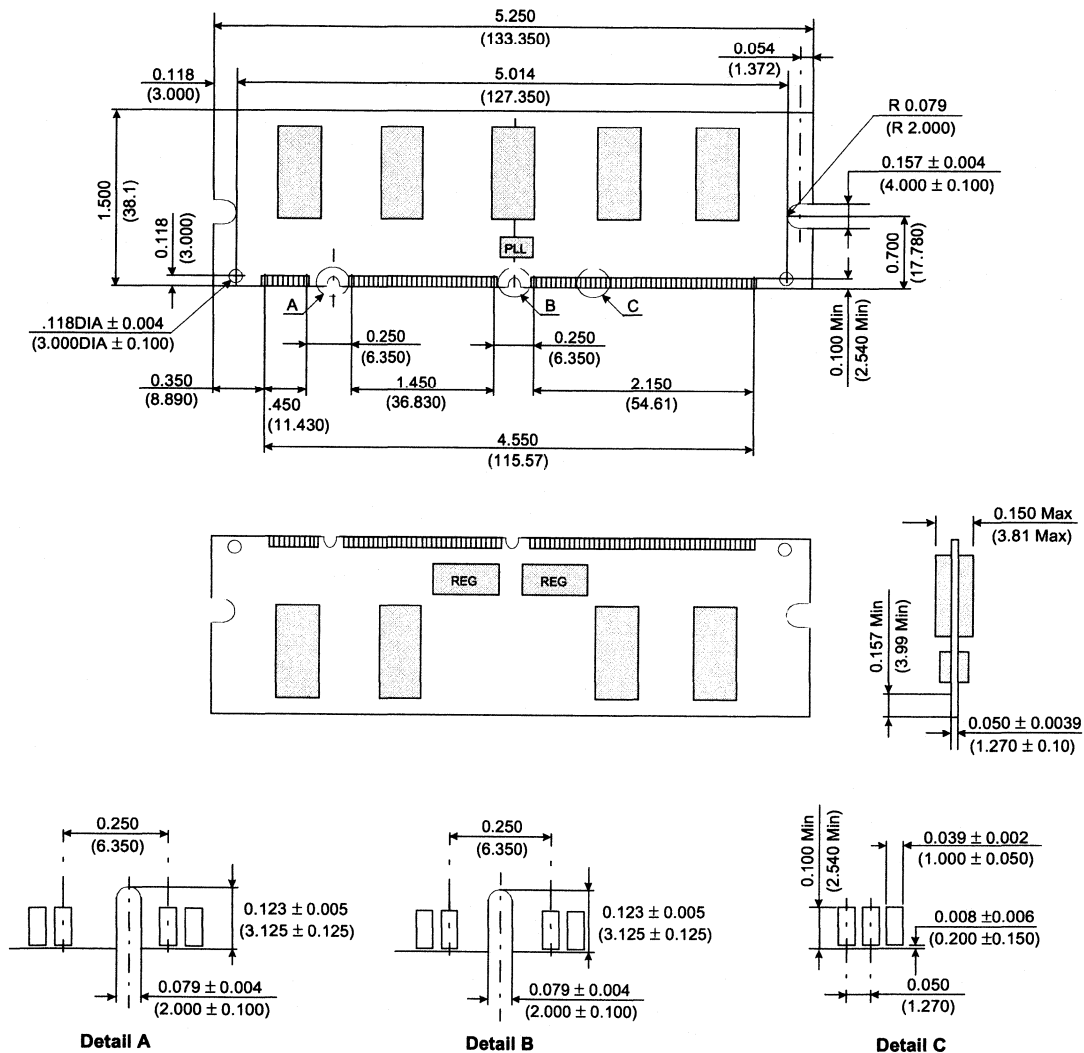
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)

Tolerances : ± 0.005 (.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
 SDRAM Part No. : K4S560832A

M377S3253AT3-C1H/C1L (1.2 ver.)

- Organization : 32MX72
- Composition : 32MX8 * 9ea
- Used component part # : K4S560832A-TC1H/1L
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 8K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	13		0Dh		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	7.8us, support self refresh		82h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 256MB		40h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		86h	34h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Samsung memory)	M		4Dh		
74	Manufacturer part # (Samsung memory)	3		33h		
75	Manufacturer part # (Memory module)	Blank		20h		
76	Manufacturer part # (Memory type & edge connector)	7		37h		
77	Manufacturer part # (Data bits)	7		37h		
78	 Manufacturer part # (Data bits)	S		53h		
79	 Manufacturer part # (Data bits)	3		33h		
80	Manufacturer part # (Mode & operating voltage)	2		32h		
81	Manufacturer part # (Module density)	5		35h		
82	 Manufacturer part # (Module density)	3		33h		
83	Manufacturer part # (Refresh, # of banks in Comp. & Inter-	A		41h		
84	Manufacturer part # (Compositon component)	T		54h		
85	Manufacturer part # (Component revision)	3		33h		
86	Manufacturer part # (Package type)	" - "		2Dh		
87	Manufacturer part # (PCB revision)	C		43h		
88	Manufacturer part # (Hyphen)	1	1	31h	31h	
89	Manufacturer part # (Power)	H	L	48h	4Ch	
90	Manufacturer part # (Minimum cycle time)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	Module Supports this CLK Frequency	100MHz		64h		
127	Attributes for CLK frequency defined	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M377S6450AT3 SDRAM DIMM (Intel 1.2 ver Base)

64Mx72 SDRAM DIMM with PLL & Register based on 64Mx4, 4Banks, 8K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S6450AT3 is a 64M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S6450AT3 consists of eighteen CMOS 64Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S6450AT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S6450AT3-C1H	100MHz (10ns @ CL=2)
M377S6450AT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

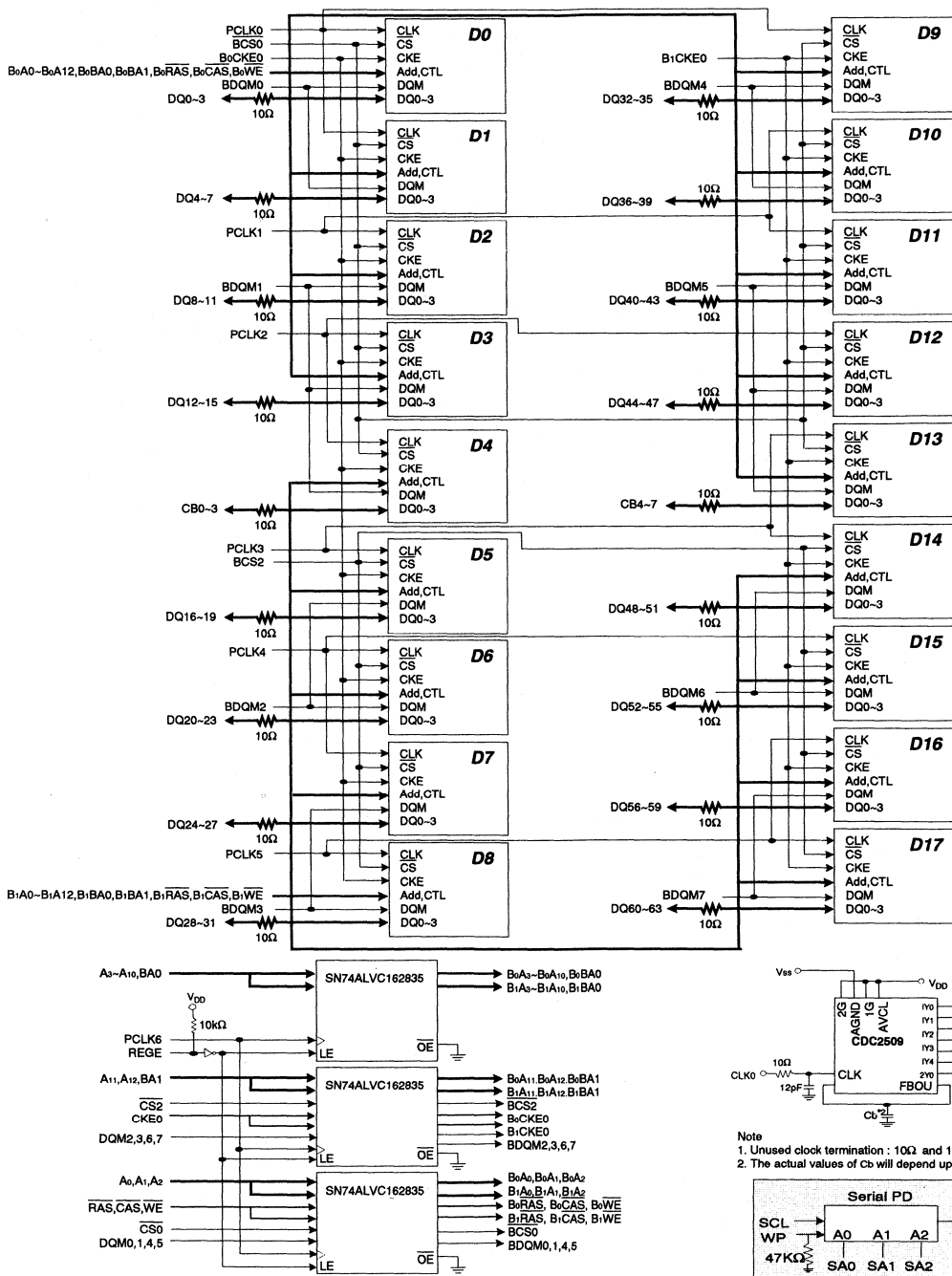
** These pins should be NC in the system which does not support SPD.

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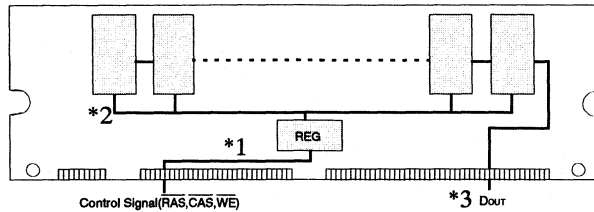
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

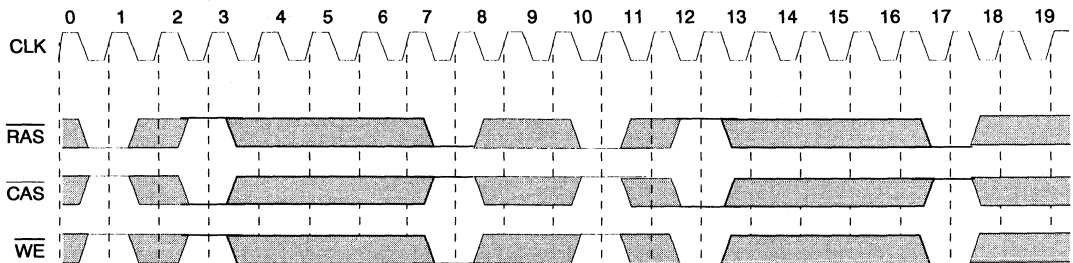
FUNCTIONAL BLOCK DIAGRAM



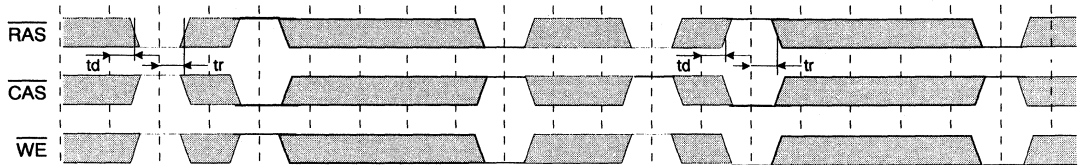
STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)



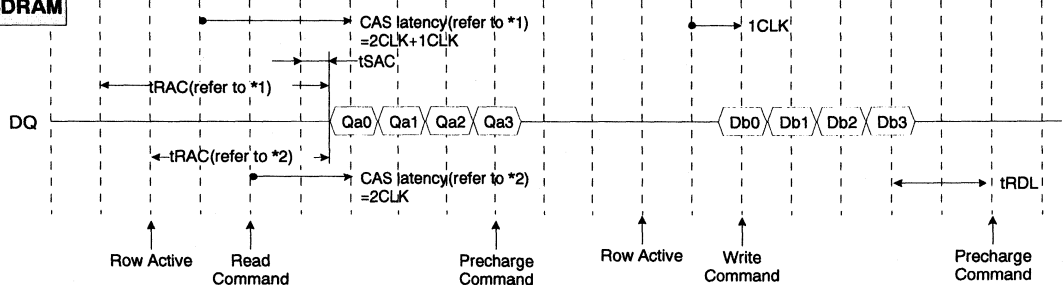
*1. Register Input



*2. Register Output



*3. SDRAM



td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

☐ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ VDDQ.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12)	C _{IN1}	-	19	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	19	pF
Input capacitance (CKE0)	C _{IN3}	-	19	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance (CS0, CS2)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	19	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	12	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	12	pF

DC CHARACTERISTICS

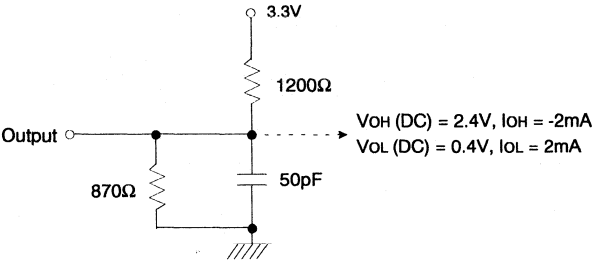
(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	2,480		mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	386		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	38		mA	
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS} \geq V_{IH(min)}$, tcc = 10ns Input signals are changed one time during 20ns	638		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	254			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	458		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	110			
Active Standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), $\overline{CS} \geq V_{IH(min)}$, tcc = 10ns Input signals are changed one time during 20ns	890		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	452		mA	3
Operating current (Burst mode)	ICC4	Io = 0mA Page burst 4Banks activated tccD=2CLK	2,570		mA	1
Refresh current	ICC5	trc ≥ trc(min)	4,100		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	440		mA	3

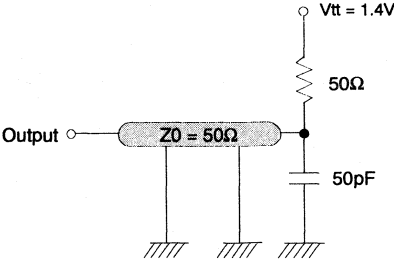
- Notes :**
1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Measured with 1 PLL & 3 Drive ICs.
 4. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.
 - 5. For -1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A12, A9 ~ A0	Note
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X	X	3	
					H	X	X	X			3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9,A11)	4
	Auto precharge enable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9,A11)	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks								X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X		
					L	V	V	V				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X		
					L	H	H	H				
		Exit	L	H	H	X	X	X	X			
					L	V	V	V				
DQM		H	X					V	X		7	
No operation command		H	X	H	X	X	X	X	X			
				L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

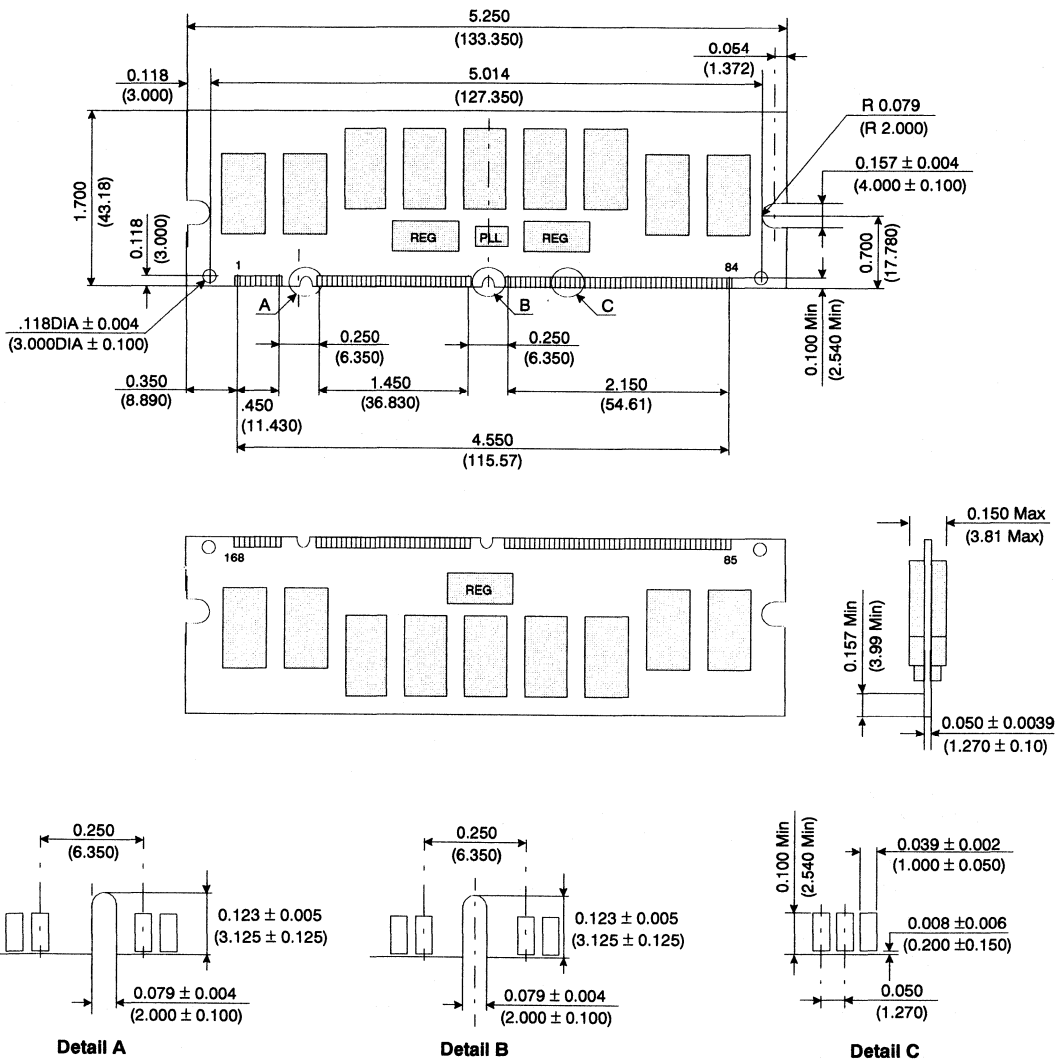
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 64Mx4 SDRAM, TSOP
 SDRAM Part No. : K4S560432A

M377S6450AT3-C1H/C1L (1.2ver)

- Organization : 64MX72
- Composition : 64MX4 *18
- Used component part # : K4S560432A-TC1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 8K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	13		0Dh		1
4	# of column address on this assembly	11		0Bh		1
5	# of module Rows on this assembly	1 Row		01h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	7.8us, support self refresh		82h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCB)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row of 512MB		80h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		A3h	D3h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	6		36h		
80	 Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	5		35h		
82	Manufacturer part # (Composition component)	0		30h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	A-die(2nd Gen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S6453AT0 SDRAM DIMM (Intel 1.2 ver Base)

64Mx72 SDRAM DIMM with PLL & Register based on 32Mx8, 4Banks 8K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S6453AT0 is a 64M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S6453AT0 consists of eighteen CMOS 32Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S6453AT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock-cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S6453AT0-C1H	100MHz (10ns @ CL=2)
M377S6453AT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

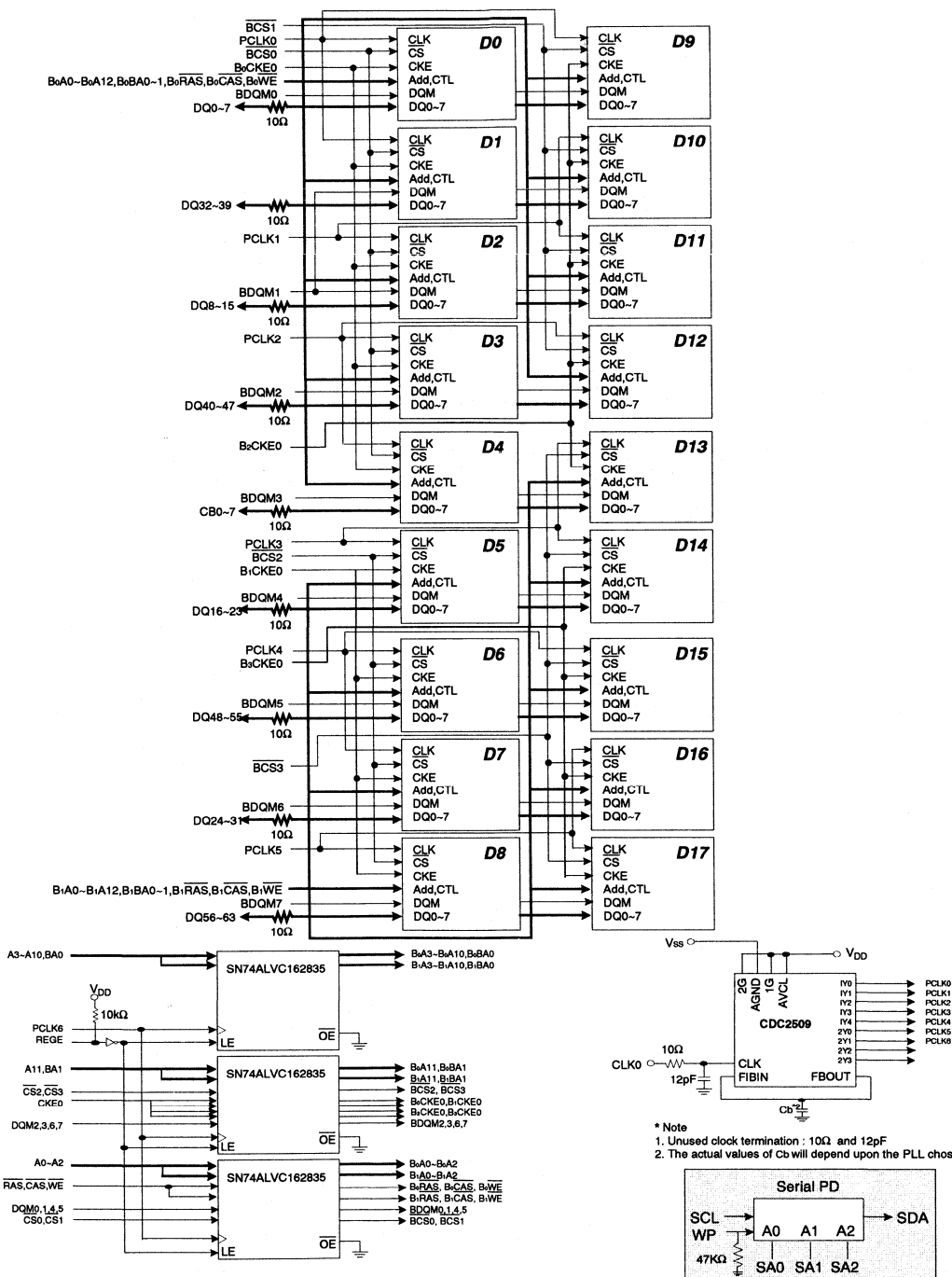
** These pins should be NC in the system which does not support SPD.

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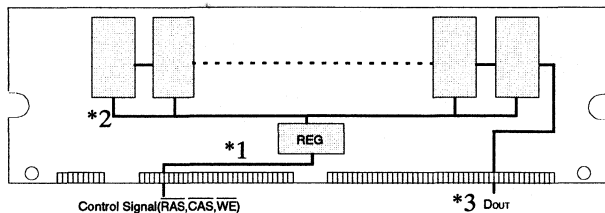
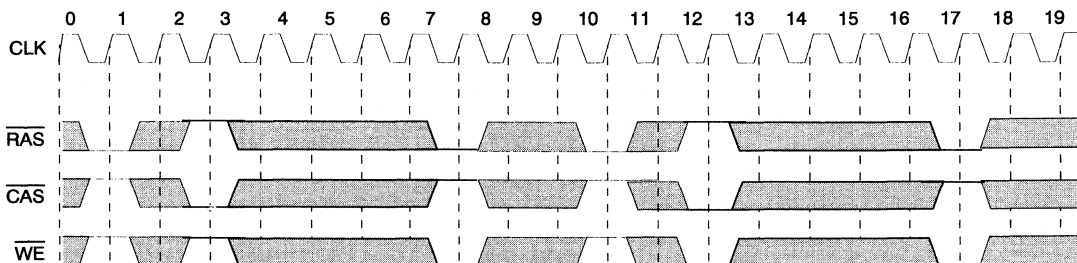
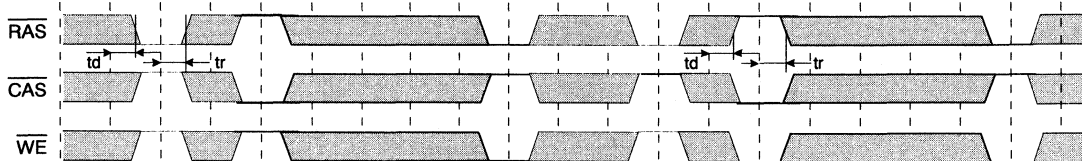
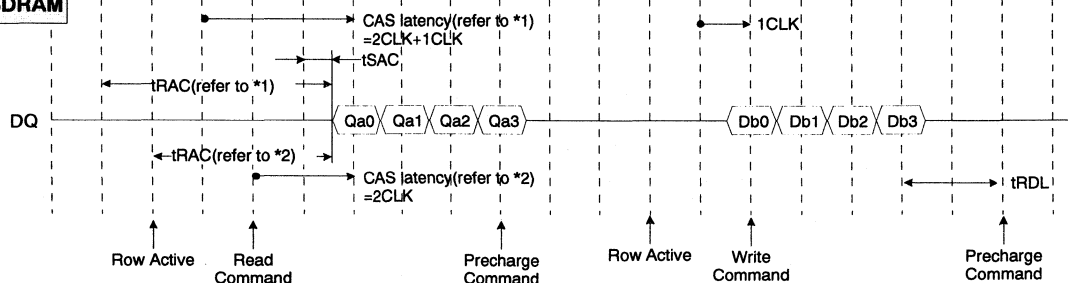
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	Register enable	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V _{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Check bit	Check bits for ECC.
WP	Write protection	WP pin is connected to V _{SS} through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V _{DD} /V _{SS}	Power supply/ground	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

td, tr = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12)	C _{IN1}	-	19	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	19	pF
Input capacitance (CKE0)	C _{IN3}	-	33	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance (CS0 ~ CS3)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	19	pF
Data input/output capacitance (CB0~CB7)	C _{OUT1}	-	19	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,760		mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	386		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	38			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	638		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	254			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	458		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	110			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	890		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	452		mA	3
Operating current (Burst mode)	ICC4	Io = 0mA Page Burst 4 Banks activated tccd=2CLK	1,805		mA	1
Refresh current	ICC5	trc ≥ trc(min)	2,570		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	440		mA	3

Notes : 1. Measured with outputs open.

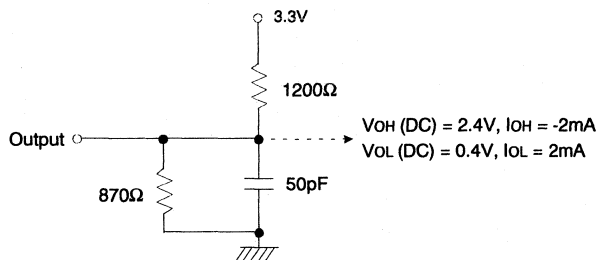
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

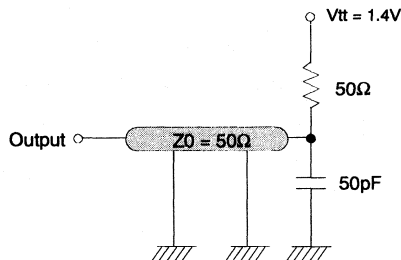
4. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -1H/1L, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .
SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A12 A9 ~ A0	Note				
Register	Mode register set		H	X	L	L	L	L	X	OP code		1,2				
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3				
	Self refresh	Entry		L							3					
		Exit	L	H	L	H	H	H	X	X	3					
					H	X	X	X			3					
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address					
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4			
	Auto precharge enable										H		4,5			
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4			
	Auto precharge enable										H		4,5			
Burst stop			H	X	L	H	H	L	X	X		6				
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X				
	All banks									X	H					
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X						
					L	V	V	V								
Precharge power down mode		Exit	L	H	X	X	X	X	X	X						
		Entry	H	L	H	X	X	X	X							
					L	H	H	H								
Exit		L	H	H	X	X	X	X								
				L	V	V	V									
DQM			H	X					V	X		7				
No operation command			H	X	H	X	X	X	X	X						
					L	H	H	H								

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

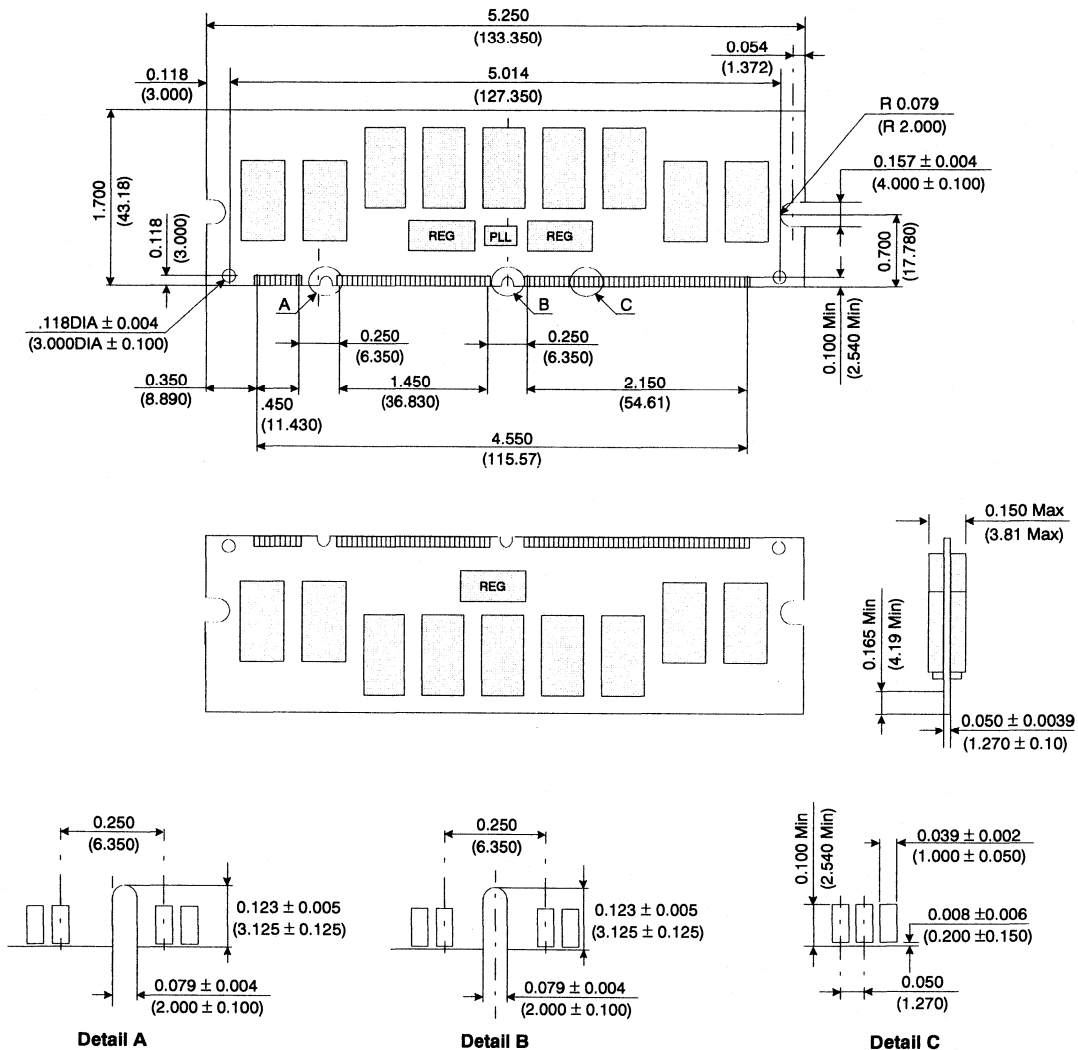
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)

Tolerances ± 0.005 (.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
 SDRAM Part No. : K4S560832A

M377S6453AT0-C1H/C1L (1.2ver)

- Organization : 64MX72
- Composition : 32MX8 *18
- Used component part # : K4S560832A-TC1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 8K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	13		0Dh		1
4	# of column address on this assembly	10		0Ah		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	7.8us, support self refresh		82h		
13	Primary SDRAM width	x8		08h		
14	Error checking SDRAM width	x8		08h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 256MB		40h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		6Bh	9Bh	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	6		36h		
80	 Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	5		35h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	0		30h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	0		30h		
92	 Manufacturer revision code (For component)	A-die(2nd Gen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M377S2858AT3 SDRAM DIMM (Intel 1.2 ver Base)

128Mx72 SDRAM DIMM with PLL & Register based on Stacked 128Mx4, 4Banks 8K Ref., 3.3V SDRAMs with SPD

GENERAL DESCRIPTION

The Samsung M377S2858AT3 is a 128M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M377S2858AT3 consists of eighteen CMOS Stacked 128Mx4 bit Synchronous DRAMs in two TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M377S2858AT3 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M377S2858AT3-C1H	100MHz (10ns @ CL=2)
M377S2858AT3-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,700mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

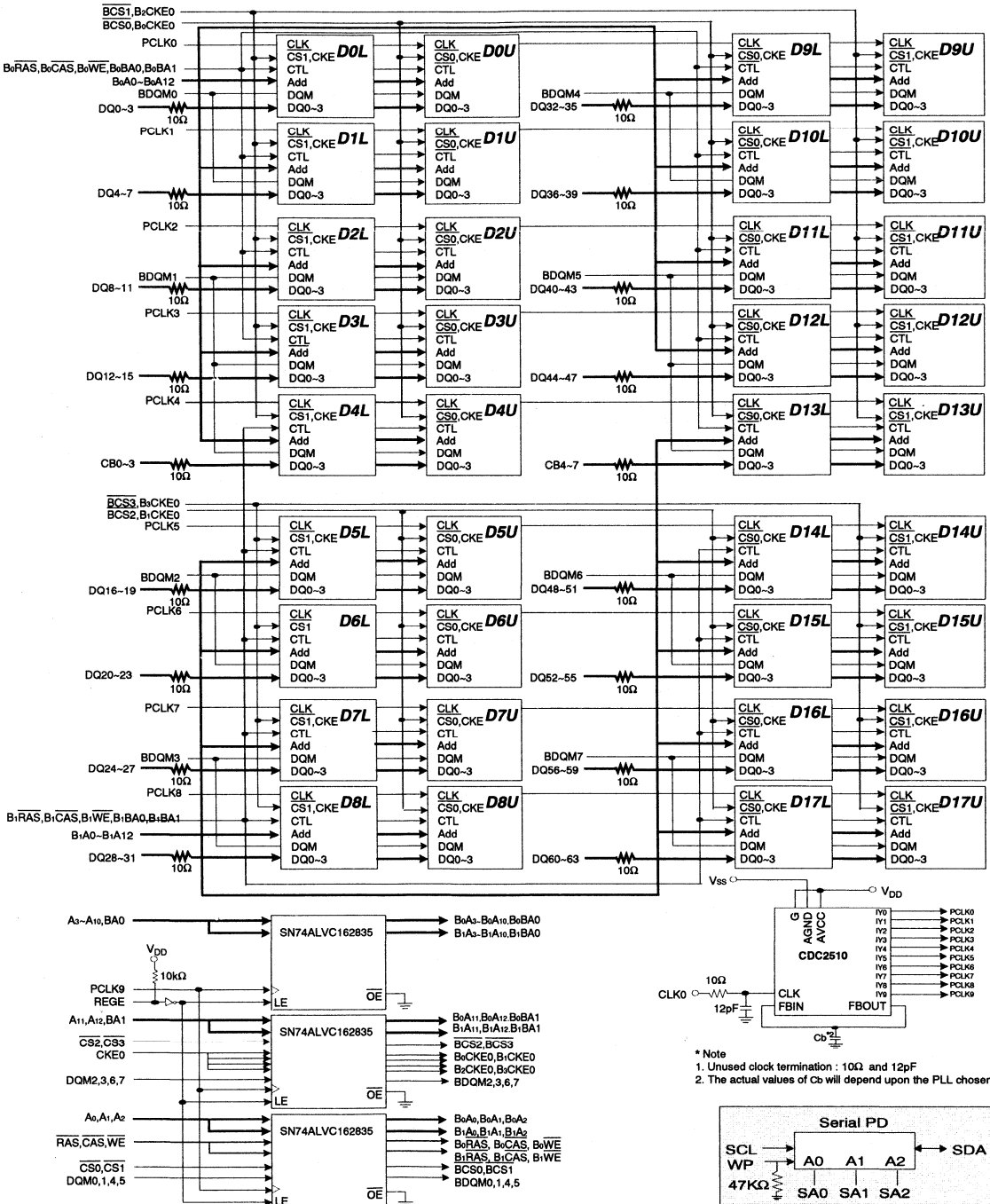
** These pins should be NC in the system which does not support SPD.

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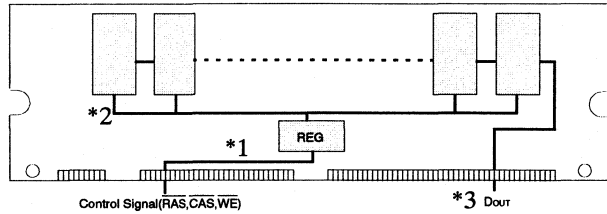
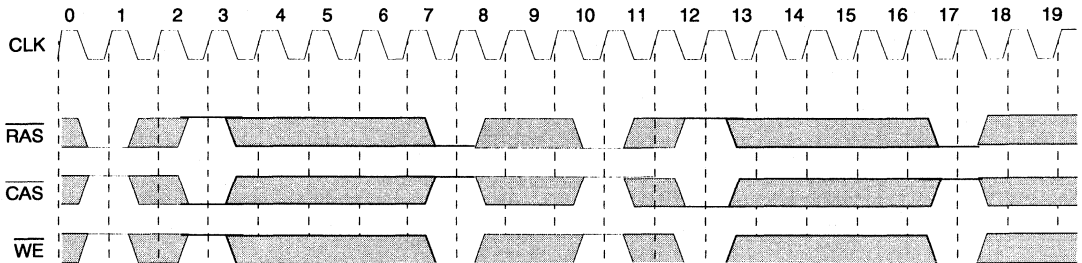
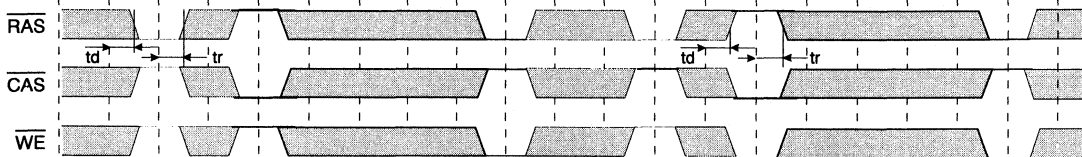
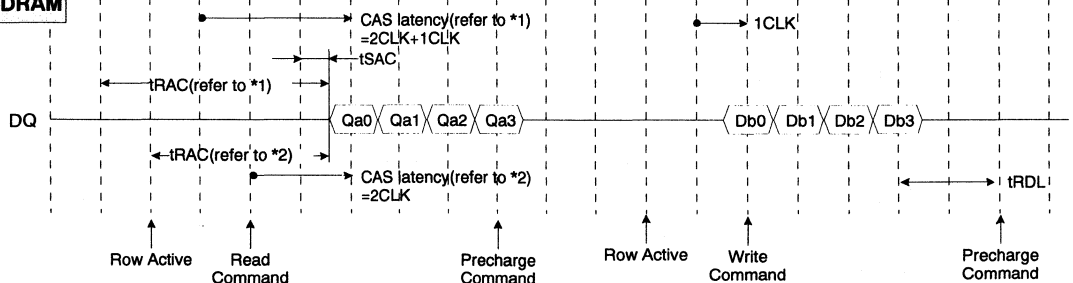
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

t_d, t_r = Delay of register (SN74ALVC162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (SN74ALVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	36	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	µA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ VDDQ

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12)	C _{IN1}	-	19	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	-	19	pF
Input capacitance (CKE0)	C _{IN3}	-	33	pF
Input capacitance (CLK0)	C _{IN4}	-	12	pF
Input capacitance (CS0 ~ CS3)	C _{IN5}	-	12	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	12	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	19	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	19	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IO = 0 mA	3,020		mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	422		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	74			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	926		mA	3
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	506			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	566		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	218			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	1,430		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	902		mA	3
Operating current (Burst mode)	ICC4	IO = 0mA Page burst 4Banks activated tccd=2CLK	3,110		mA	1
Refresh current	ICC5	trc ≥ trc(min)	4,640		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	530		mA	3

Notes : 1. Measured with outputs open.

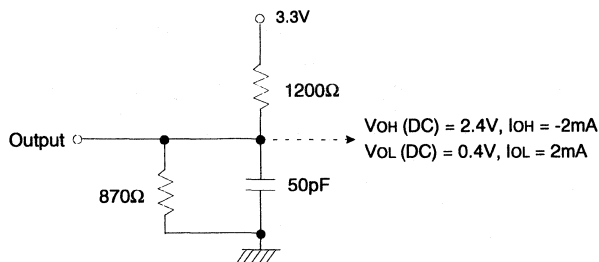
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

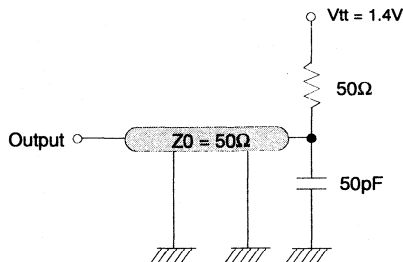
4. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	Note
			-1H	-1L		
Row active to row active delay		tRRD(min)	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	ns	1
Row precharge time		tRP(min)	20	20	ns	1
Row active time		tRAS(min)	50	50	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	70	70	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -1H/1L, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .
SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-1H		-1L		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	10	1000	ns	1
	CAS latency=2		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6	ns	1,2
	CAS latency=2			6		7		
Output data hold time	CAS latency=3	tOH	3		3		ns	1,2
	CAS latency=2		3		3			
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6	ns	1
	CAS latency=2			6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A12 A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	L		3									
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable										H		4,5
Write & Column Address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

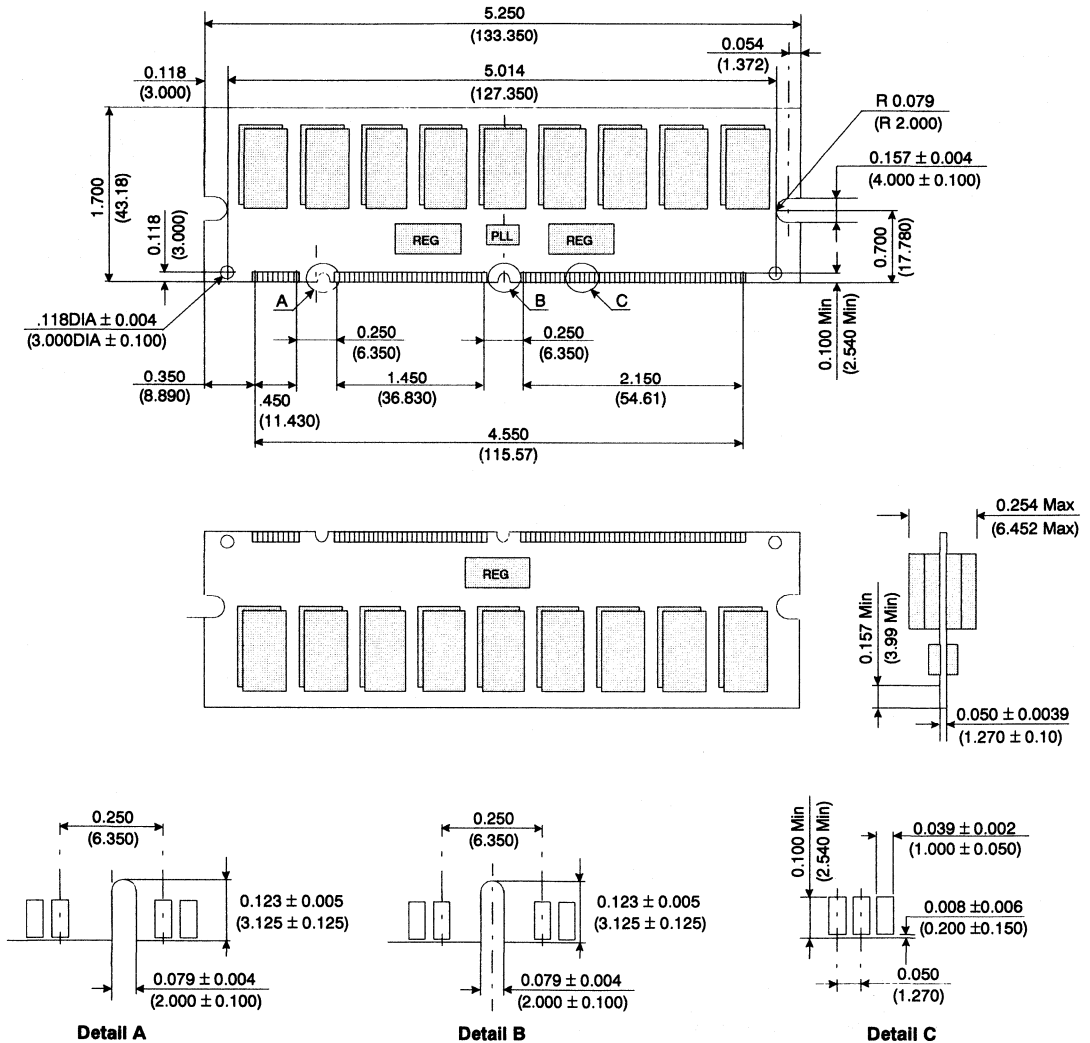
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC100 Registered DIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 128Mx4 SDRAM, TSOP
SDRAM Part No. : K4S510632A

M377S2858AT3-C1H/C1L (1.2ver)

- Organization : 128MX72
- Composition : 128MX4 *18
- Used component part # : K4S510632A-TC1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 8K/64ms
- Contents :

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes		80h		
1	Total # of bytes of SPD memory device	256bytes (2K-bit)		08h		
2	Fundamental memory type	SDRAM		04h		
3	# of row address on this assembly	13		0Dh		1
4	# of column address on this assembly	11		0Bh		1
5	# of module Rows on this assembly	2 Rows		02h		
6	Data width of this assembly	72 bits		48h		
7	 Data width of this assembly	-		00h		
8	Voltage interface standard of this assembly	LVTTTL		01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	ECC		02h		
12	Refresh rate & type	7.8us, support self refresh		82h		
13	Primary SDRAM width	x4		04h		
14	Error checking SDRAM width	x4		04h		
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK		01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page		8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 banks		04h		
18	SDRAM device attributes : CAS latency	2 & 3		06h		
19	SDRAM device attributes : CS latency	0 CLK		01h		
20	SDRAM device attributes : Write latency	0 CLK		01h		
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL		1Fh		
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge		0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows of 512MB		80h		
32	Command and Address signal input setup time	2ns		20h		
33	Command and Address signal input hold time	1ns		10h		
34	Data signal input setup time	2ns		20h		

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-1H	-1L	-1H	-1L	
35	Data signal input hold time	1ns		10h		
36~61	Superset Information (maybe used in future)	-		00h		
62	SPD data revision code	Current release Intel spd 1.2A		12h		
63	Checksum for bytes 0 ~ 62	-		A4h	D4h	
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM configuration)	3		33h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	7		37h		
77	 Manufacturer part # (Data bits)	7		37h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	2		32h		
80	 Manufacturer part # (Module depth)	8		38h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	5		35h		
82	Manufacturer part # (Composition component)	8		38h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	3		33h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	C		43h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	H	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	3		33h		
92	 Manufacturer revision code (For component)	A-die(2nd Gen.)		41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	System frequency for 100MHz	100MHz		64h		
127	Intel Specification details	Detailed 100MHz Information		8Fh	8Dh	
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M366S0924MTS SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0924MTS is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0924MTS consists of four CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0924MTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0924MTS-C80	125MHz (8ns @ CL=3)
M366S0924MTS-C1H	100MHz (10ns @ CL=2)
M366S0924MTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,000mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

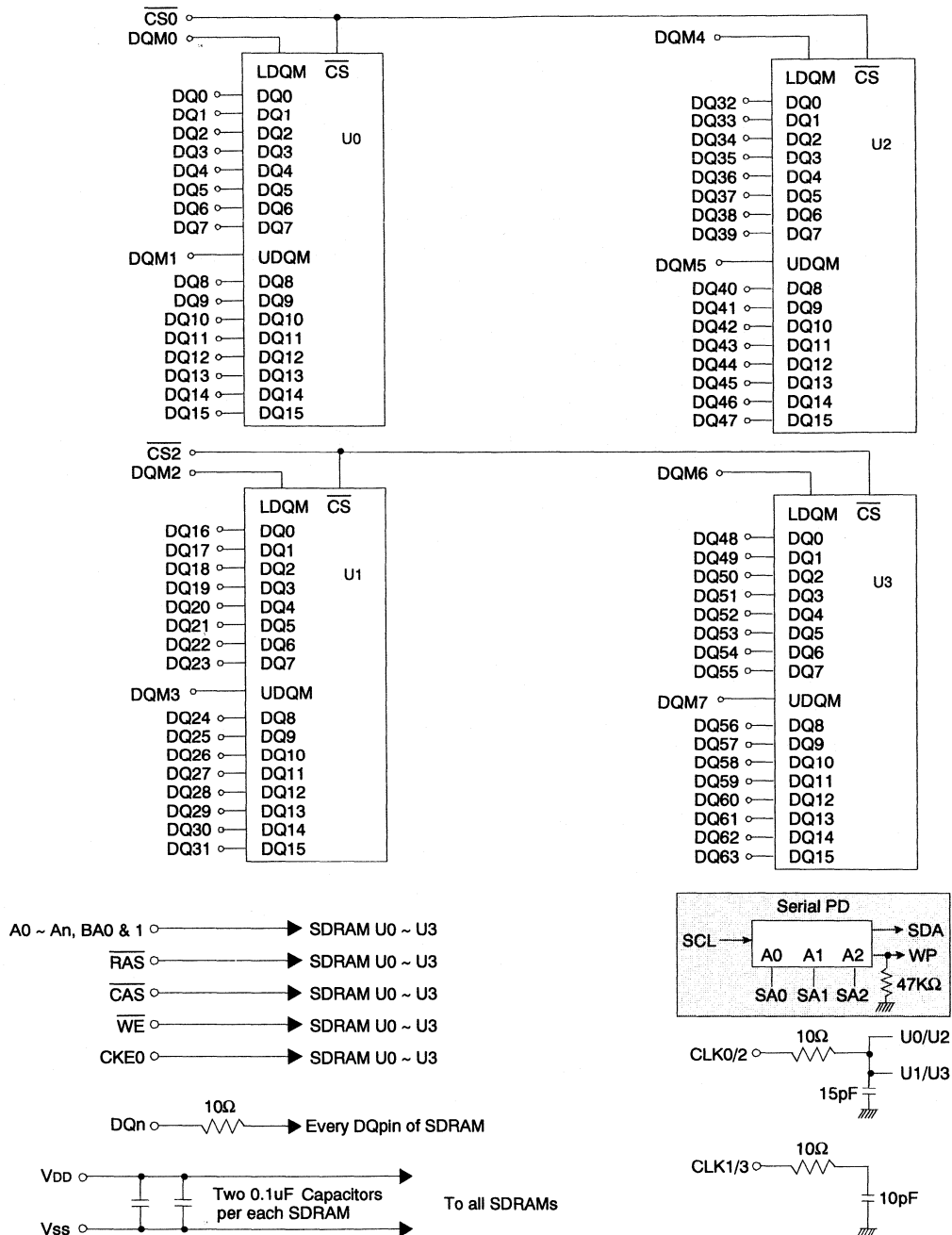
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	4	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-4	-	4	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	30	40	pF
RAS, CAS, WE	C _{IN}	30	40	pF
CKE (CKE0)	C _{CKE}	25	35	pF
Clock (CLK0, CLK2)	C _{CLK}	15	25	pF
CS (CS0, CS2)	C _{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	5	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

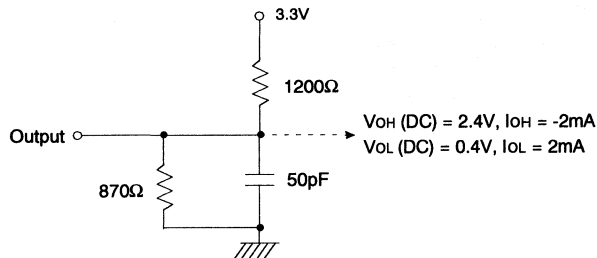
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		520	480	480	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		4			mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		4				
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		60			mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		28				
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		20			mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		20				
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		120			mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		80			mA	
Operating current (Burst mode)	ICC4	IOL = 0 mA Page burst 2Banks activated tccd = 2CLKs	3	680	580	580	mA	1
			2	540	580	540		
Refresh current	ICC5	trc ≥ trc(min)		800			mA	2
Self refresh current	ICC6	CKE ≤ 0.2V		6			mA	

Notes : 1. Measured with outputs open.

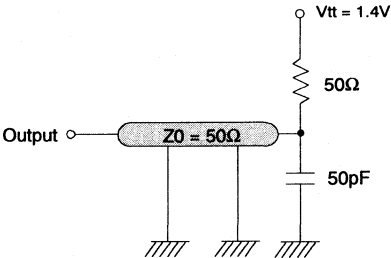
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

- Notes :** 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	toH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tss	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

- Notes :
- 1. Parameters depend on programmed CAS latency.
 - 2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
 - 3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

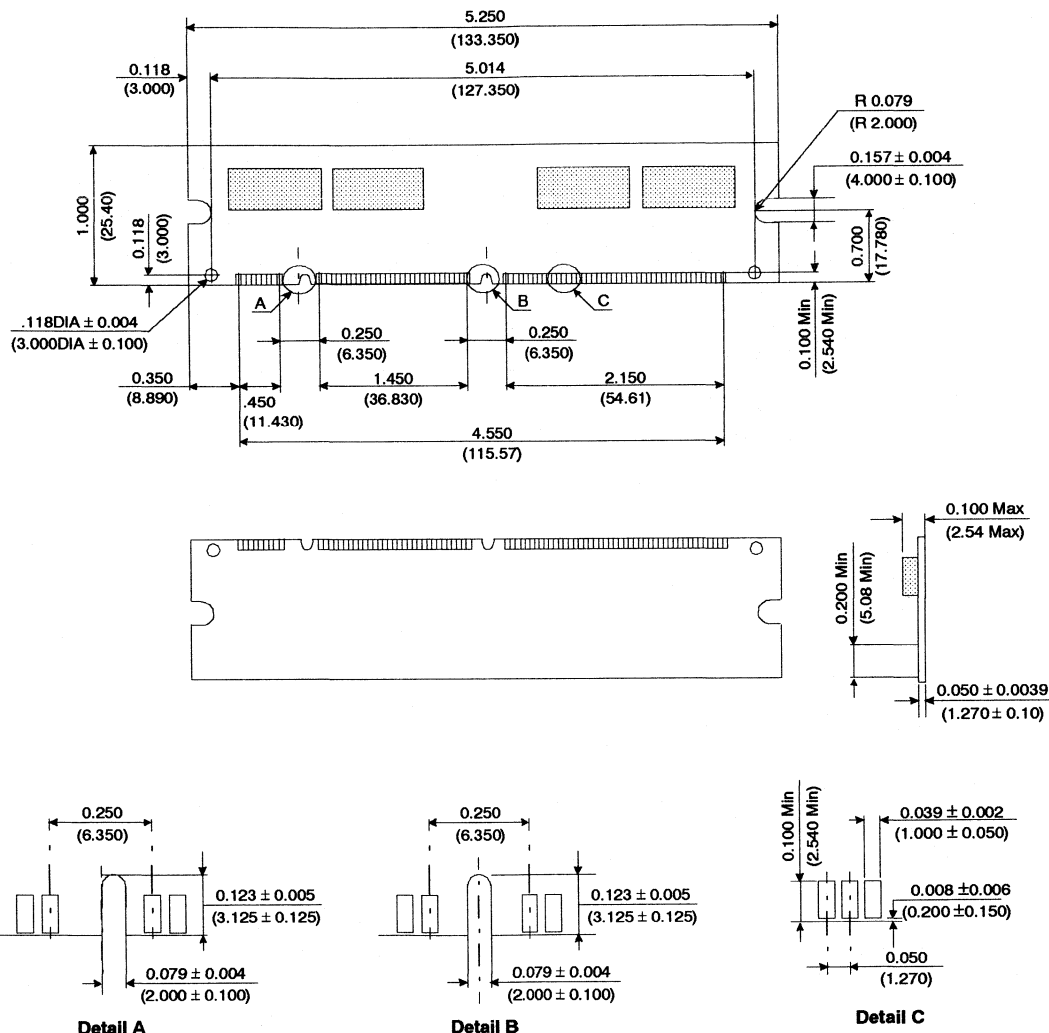
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± .005(.13) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
 SDRAM Part No. : K4S281632M

M366S0924MTS-C80/C1H/C1L

- Organization : 8Mx64
- Composition : 8Mx16 *4
- Used component part # : K4S281632M-TC80/C1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec.Ver.1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			07h	0Dh	3Dh	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	 Manufacturer part # (Module depth)	9			39h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	4			34h			
83	Manufacturer part # (Component revision)	M			4Dh			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	 Manufacturer revision code (For component)	M-die (1st Gen.)			4Dh			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M366S1724MT0 SDRAM DIMM

16Mx64 SDRAM DIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1724MT0 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1724MT0 consists of eight CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S1724MT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S1724MT0-C80	125MHz (8ns @ CL=3)
M366S1724MT0-C1H	100MHz (10ns @ CL=2)
M366S1724MT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	Vdd	77	DQ31	105	*CB4	133	Vdd	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

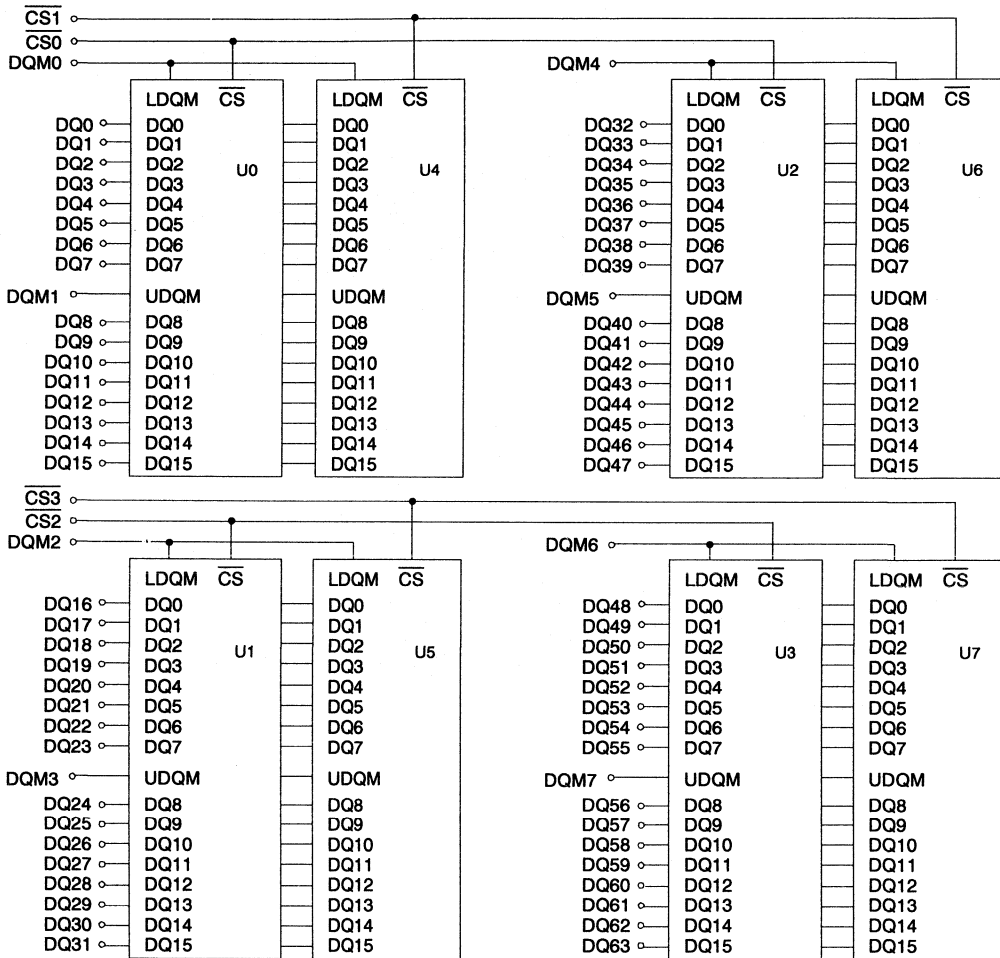
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

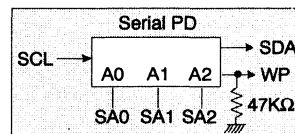
FUNCTIONAL BLOCK DIAGRAM



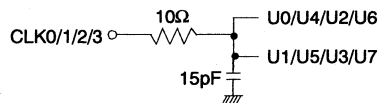
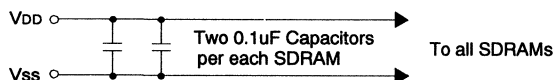
A0 ~ An, BA0 & 1 → SDRAM U0 ~ U7

 $\overline{\text{RAS}}$ → SDRAM U0 ~ U7 $\overline{\text{CAS}}$ → SDRAM U0 ~ U7 $\overline{\text{WE}}$ → SDRAM U0 ~ U7

CKE0 → SDRAM U0 ~ U3 CKE1 → SDRAM U4 ~ U7



DQn → 10Ω → Every DQpin of SDRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-8	-	8	μA	3
Input leakage current (I/O pins)	I _{IL}	-3	-	3	μA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	40	60	pF
RAS, CAS, WE	C _{IN}	40	60	pF
CKE (CKE0)	C _{CKE}	25	35	pF
Clock (CLK0, CLK2)	C _{CLK}	15	25	pF
$\overline{\text{CS}}$ ($\overline{\text{CS0}}$, $\overline{\text{CS2}}$)	C _{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	5	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

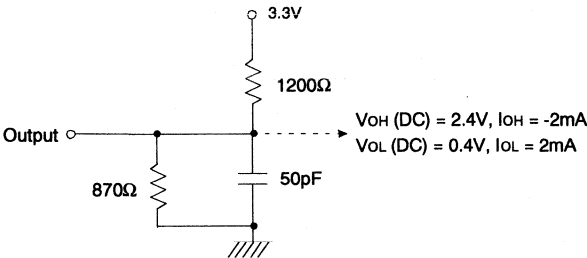
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		640	600	600	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		8			mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		8				
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		120			mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		56				
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		40			mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		40				
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		160			mA	
Operating current (Burst mode)	ICC4	IOL = 0 mA Page burst 2Banks activated tCCD = 2CLKs	3	800	700	700	mA	1
			2	660	700	660		
Refresh current	ICC5	trc ≥ trc(min)		1,600			mA	2
Self refresh current	ICC6	CKE ≤ 0.2V		12			mA	

Notes : 1. Measured with outputs open.

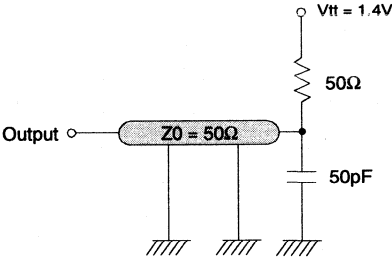
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (V _{ih} /V _{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

- Notes :** 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1, 2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA _{0,1}	A _{10/AP}	A ₁₁ , A ₉ ~ A ₀	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A ₀ ~ A ₉)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A ₀ ~ A ₉)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A_{10/AP} is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

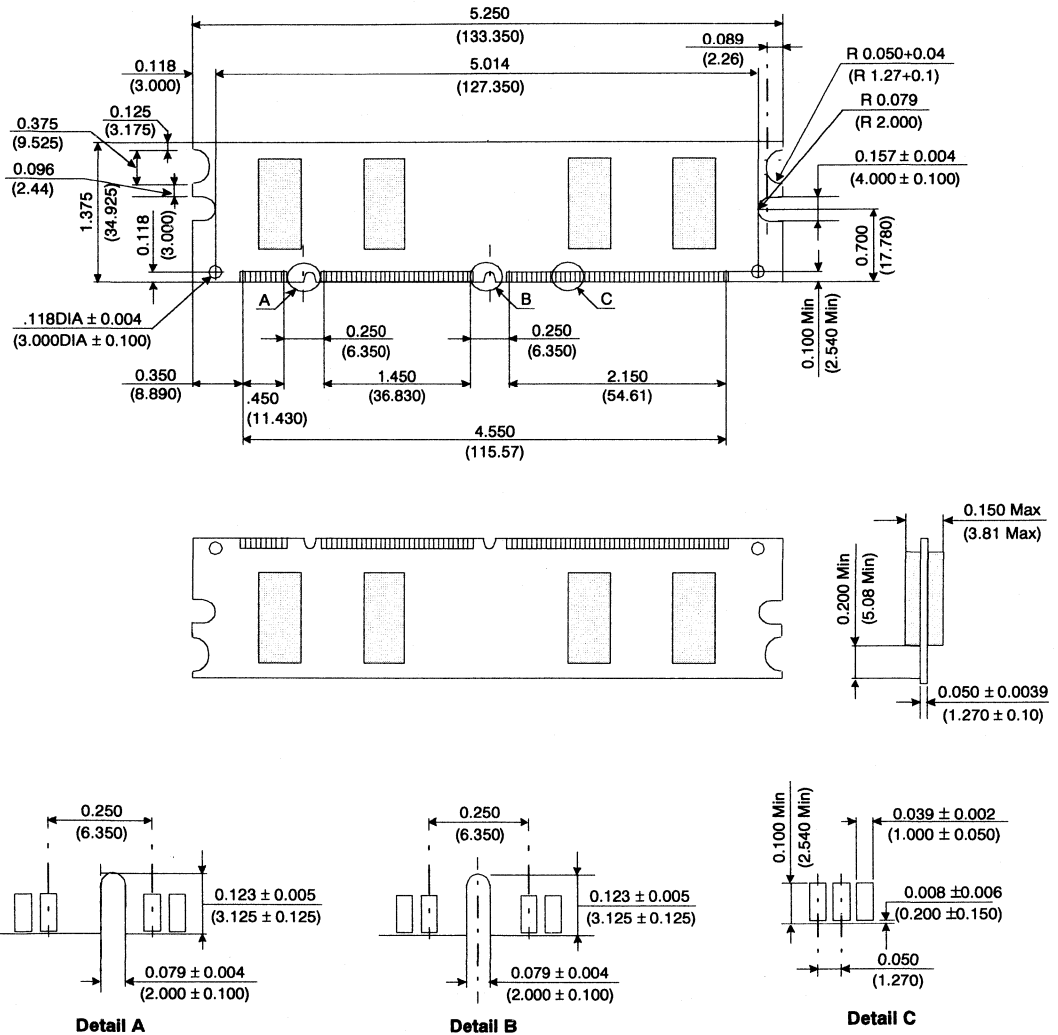
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)

Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
 SDRAM Part No. : K4S281632M

M366S1724MT0-C80/C1H/C1L

- Organization : 16Mx64
- Composition : 8Mx16 *8
- Used component part # : K4S281632M-TC80/C1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

SERIAL PRESENCE DETECT

PC100 Unbuffered DIMM

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			08h	0Eh	3Eh	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	 Manufacturer part # (Module depth)	7			37h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	4			34h			
83	Manufacturer part # (Component revision)	M			4Dh			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	 Manufacturer revision code (For component)	M-die (1st Gen.)			4Dh			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :** 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S1723MTS SDRAM DIMM

16Mx64 SDRAM DIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1723MTS is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1723MTS consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.22 uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S1723MTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S1723MTS-C80	125MHz (8ns @ CL=3)
M366S1723MTS-C1H	100MHz (10ns @ CL=2)
M366S1723MTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

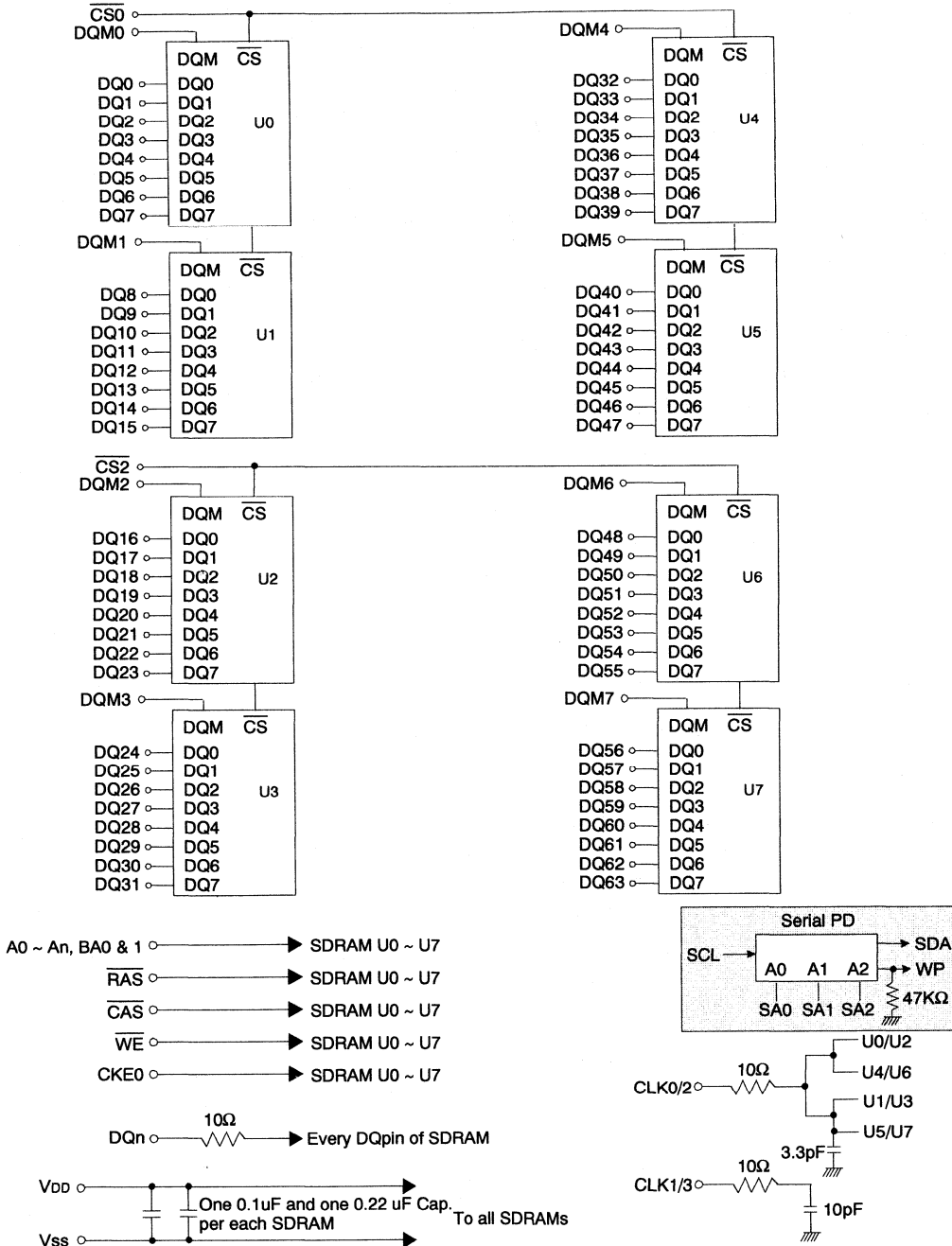
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, 0V ≤ V_{OUT} ≤ VDDQ.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	40	60	pF
RAS, CAS, WE	C _{IN}	40	60	pF
CKE (CKE0)	C _{CKE}	35	55	pF
Clock (CLK0, CLK2)	C _{CLK}	25	35	pF
CS (CS0, CS2)	C _{CS}	25	35	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	5	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

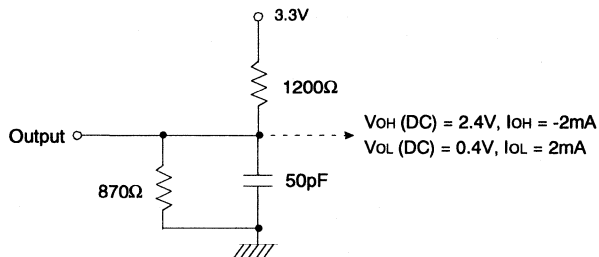
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) IoL = 0 mA		960	880	880	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 15ns		8			mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞		8				
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		120			mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		56				
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 15ns		40			mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞		40				
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		160			mA	
Operating current (Burst mode)	Icc4	IoL = 0 mA Page burst 2Banks activated tccD = 2CLKs	3	1,200	1,000	1,000	mA	1
			2	920	1,000	920		
Refresh current	Icc5	trc ≥ trc(min)		1,600			mA	2
Self refresh current	Icc6	CKE ≤ 0.2V		12			mA	

Notes : 1. Measured with outputs open.

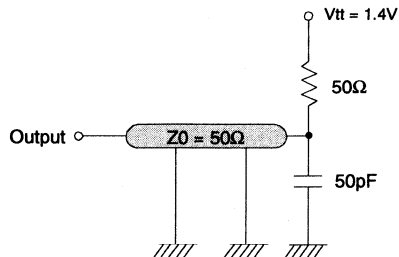
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4	
	CAS latency=2	1					

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12			
CLK to valid output delay	CAS latency=3	tsac		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	toH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tss	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	H	X	X			3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	X	X			3	
												H	X
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

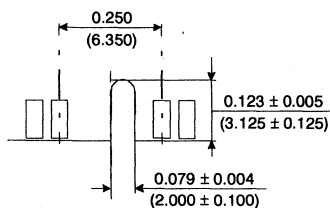
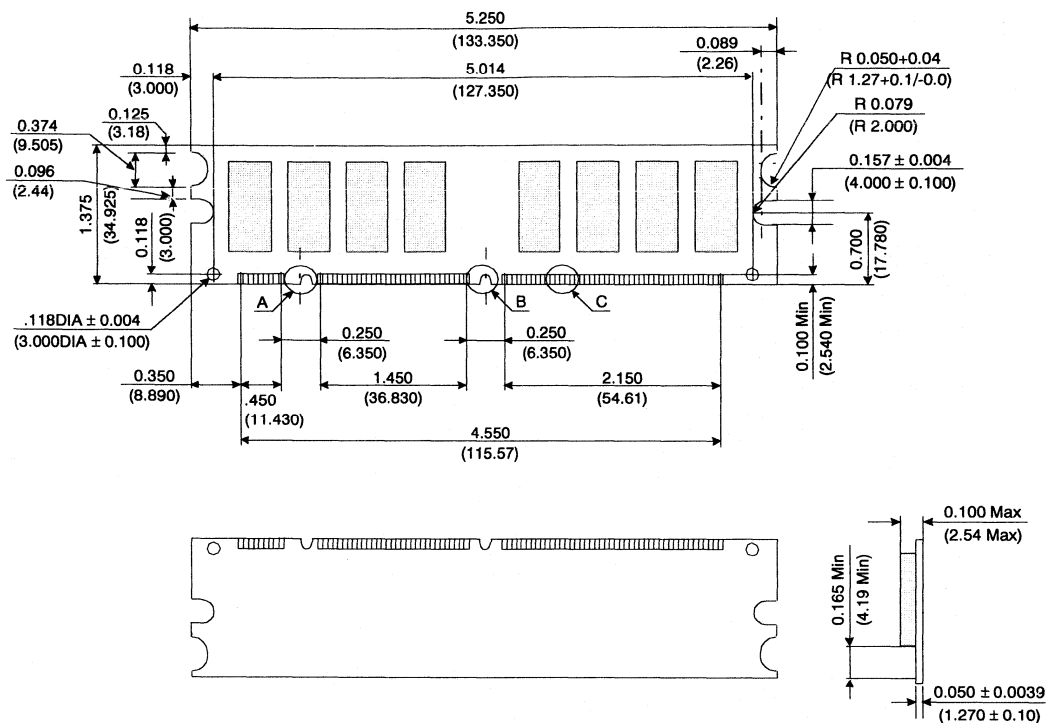
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

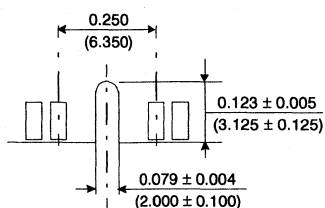
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

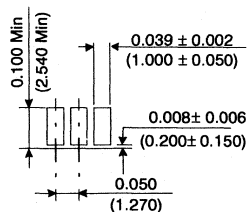
Units : Inches (Millimeters)



Detail A



Detail B



Detail C

Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832M

M366S1723MTS-C80/C1H/C1L

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832M-TC80/C1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			10h	16h	46h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	 Manufacturer part # (Module depth)	7			37h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	M			4Dh			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	 Manufacturer revision code (For component)	M-die (1st Gen.)			4Dh			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S1723MTS SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S1723MTS is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S1723MTS consists of nine CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.22 uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S1723MTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S1723MTS-C80	125MHz (8ns @ CL=3)
M374S1723MTS-C1H	100MHz (10ns @ CL=2)
M374S1723MTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	*SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	*SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

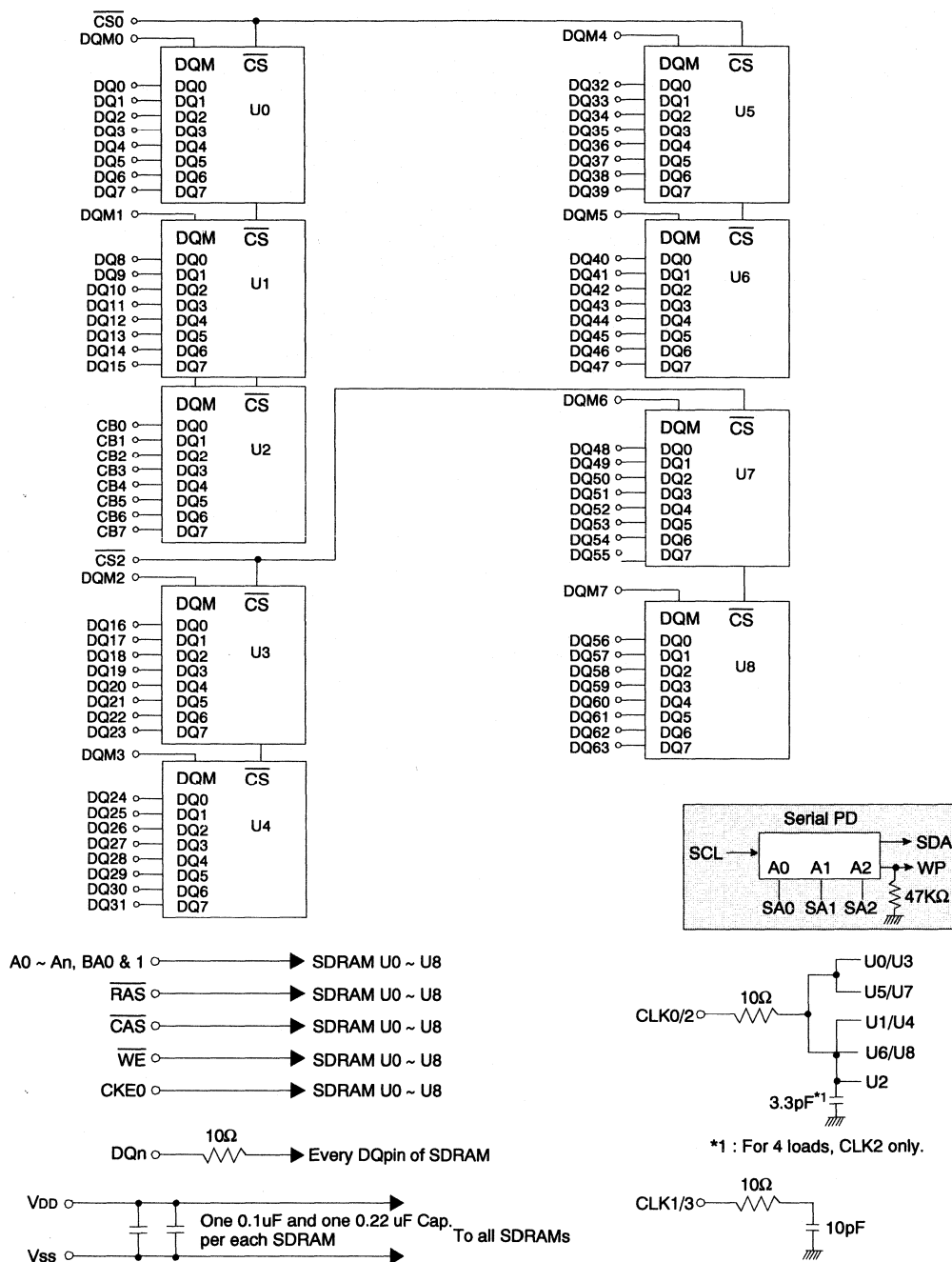
* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Check bit	Check bits for ECC.
WP	Write protection	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-9	-	9	uA	3
Input leakage current (I/O pins)	I _{IL}	-1.5	-	1.5	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	45	65	pF
RAS, CAS, WE	C _{IN}	45	65	pF
CKE (CKE0)	C _{CKE}	40	60	pF
Clock (CLK0, CLK2)	C _{CLK}	30	40	pF
CS (CS0, CS2)	C _{CS}	30	40	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	5	15	pF
DQ (DQ0 ~ DQ63)	C _{OUT1}	5	15	pF
CB (CB0 ~ CB7)	C _{OUT2}	5	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

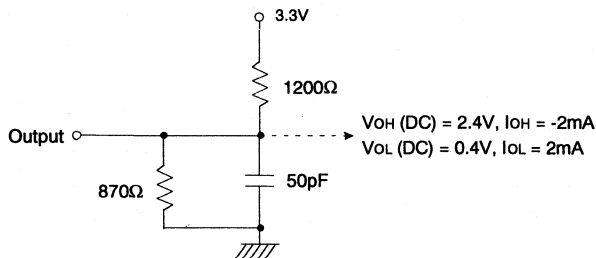
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\text{min})$ $I_{OL} = 0 \text{ mA}$		1,080	990	990	mA	1
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL}(\text{max})$, $t_{CC} = 15\text{ns}$		9			mA	
	ICC2PS	$CKE \ \& \ CLK \leq V_{IL}(\text{max})$, $t_{CC} = \infty$		9				
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH}(\text{min})$, $\overline{CS} \geq V_{IH}(\text{min})$, $t_{CC} = 15\text{ns}$ Input signals are changed one time during 30ns		135			mA	
	ICC2NS	$CKE \geq V_{IH}(\text{min})$, $CLK \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable		63				
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL}(\text{max})$, $t_{CC} = 15\text{ns}$		45			mA	
	ICC3PS	$CKE \ \& \ CLK \leq V_{IL}(\text{max})$, $t_{CC} = \infty$		45				
Active standby current in non power-down mode (One bank active)	ICC3N	$CKE \geq V_{IH}(\text{min})$, $\overline{CS} \geq V_{IH}(\text{min})$, $t_{CC} = 15\text{ns}$ Input signals are changed one time during 30ns		270			mA	
	ICC3NS	$CKE \geq V_{IH}(\text{min})$, $CLK \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable		180			mA	
Operating current (Burst mode)	ICC4	$I_{OL} = 0 \text{ mA}$ Page burst 2Banks activated $t_{CCD} = 2CLKs$	3	1,350	1,120	1,120	mA	1
			2	1,030	1,120	1,030		
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\text{min})$		1,800			mA	2
Self refresh current	ICC6	$CKE \leq 0.2V$		13			mA	

Notes : 1. Measured with outputs open.

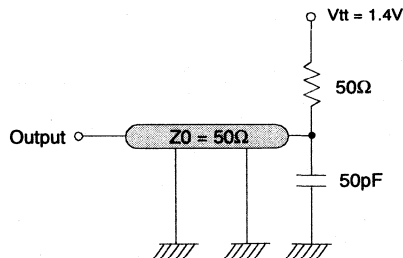
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4	
	CAS latency=2	1					

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1, 2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA _{0,1}	A ₁₀ /AP	A ₁₁ , A ₉ ~ A ₀	Note	
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3	
	Self refresh	Entry		L									3	
		Exit	L	H	L	H	H	H	X	X			3	
					H	X	X	X					3	
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A ₀ ~ A ₉)	4	
	Auto precharge enable										H		4,5	
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A ₀ ~ A ₉)	4	
	Auto precharge enable										H		4,5	
Burst stop			H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X		
	All banks									X	H			
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X				
					L	V	V	V						
Precharge power down mode		Entry	H	L	H	X	X	X	X	X				
					L	H	H	H						
		Exit	L	H	H	X	X	X	X					
					L	V	V	V						
DQM			H	X					V	X			7	
No operation command			H	X	H	X	X	X	X	X				
					L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

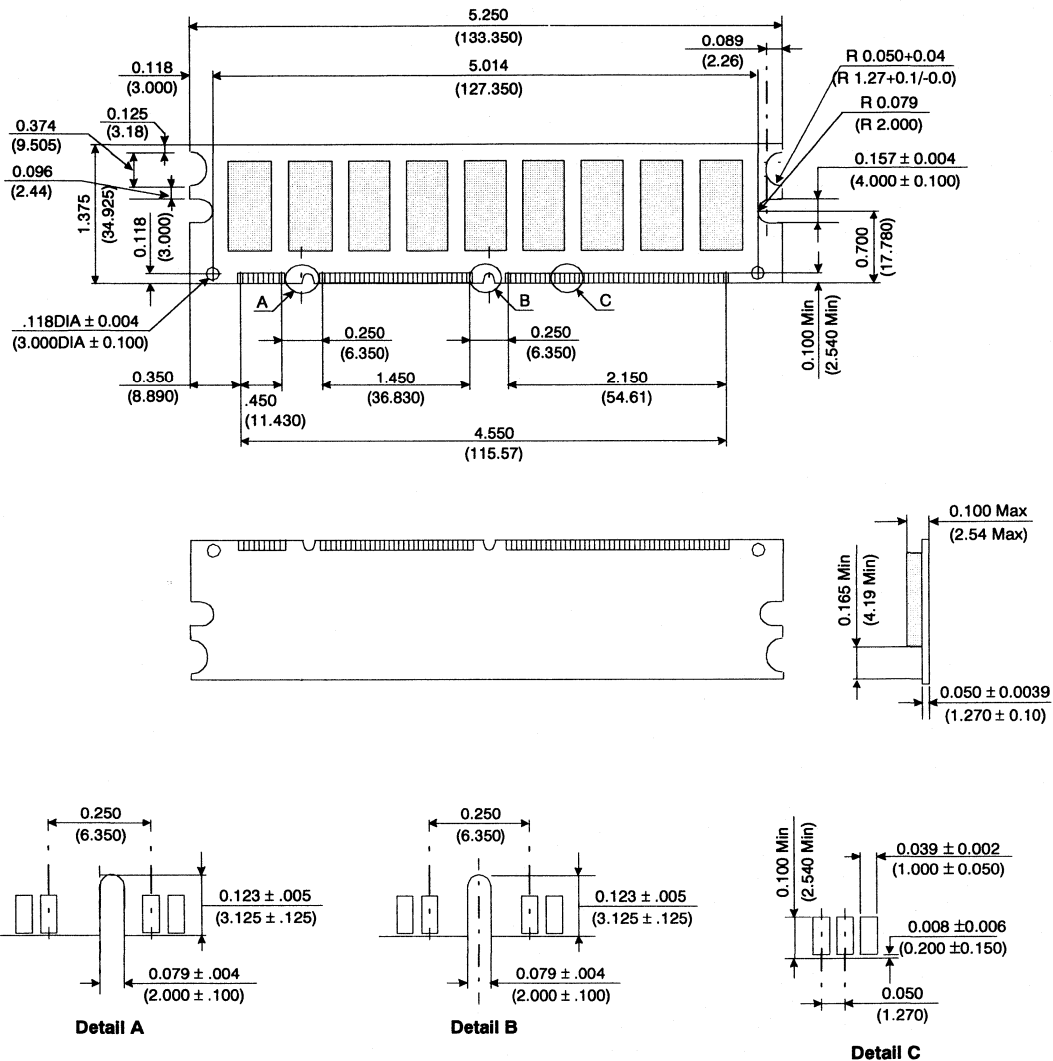
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC100 Unbuffered DIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832M

M374S1723MTS-C80/C1H/C1L

- Organization : 16Mx72
- Composition : 16Mx8 *9
- Used component part # : K4S280832M-TC80/C1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	72 bits			48h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

SERIAL PRESENCE DETECT

PC100 Unbuffered DIMM

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			22h	28h	58h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	7			37h			
77	 Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	 Manufacturer part # (Module depth)	7			37h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	M			4Dh			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	 Manufacturer revision code (For component)	M-die (1st Gen.)			4Dh			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M366S3323MT0 SDRAM DIMM

32Mx64 SDRAM DIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S3323MT0 is a 32M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S3323MT0 consists of sixteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S3323MT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S3323MT0-C80	125MHz (8ns @ CL=3)
M366S3323MT0-C1H	100MHz (10ns @ CL=2)
M366S3323MT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

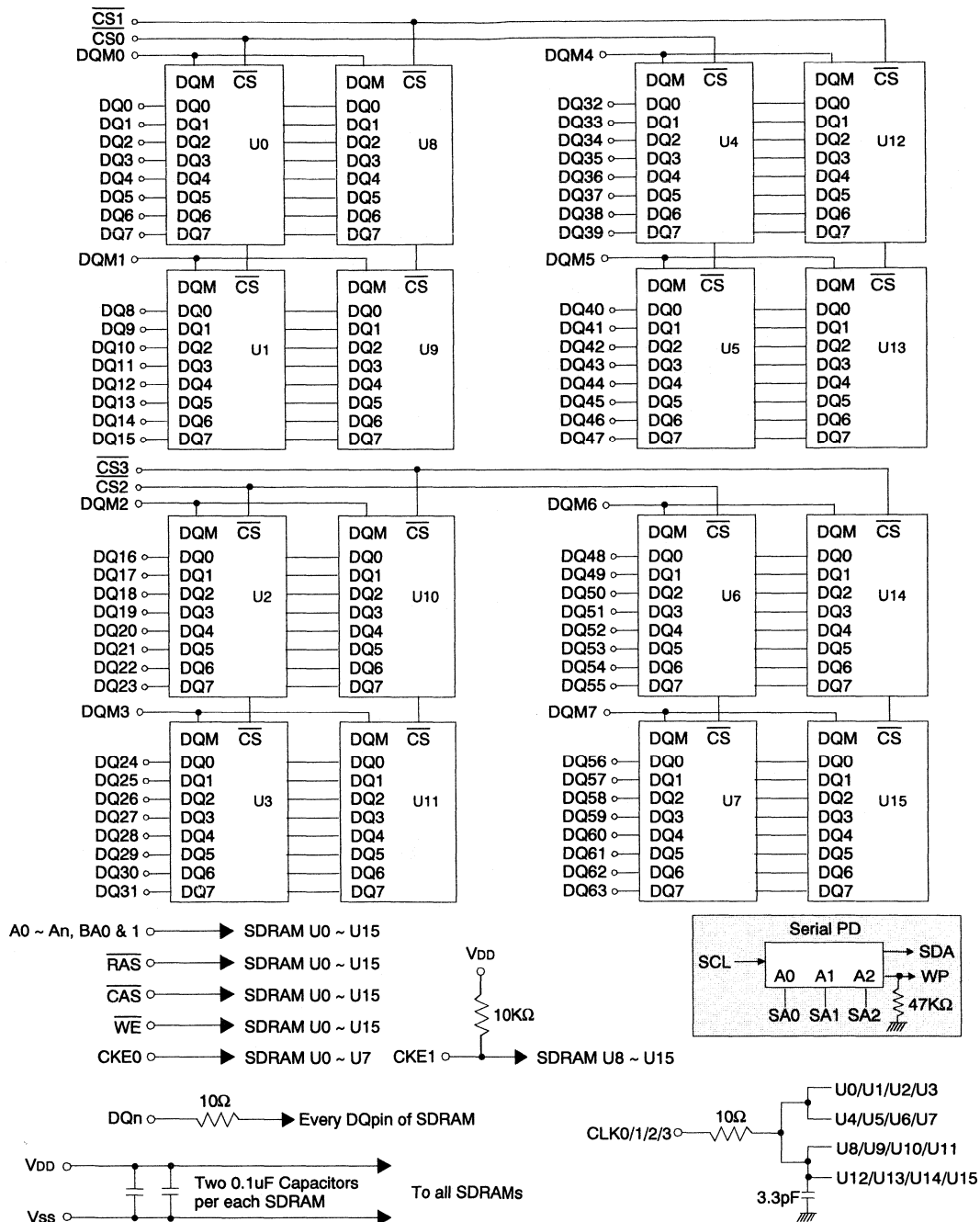
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	16	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-16	-	16	µA	3
Input leakage current (I/O pins)	I _{IL}	-3	-	3	µA	3,4

- Notes :**
1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	60	90	pF
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	C _{IN}	60	90	pF
CKE (CKE0 ~ CKE1)	C _{CKE}	35	55	pF
Clock (CLK0 ~ CLK3)	C _{CLK}	25	35	pF
CS (CS0 ~ CS3)	C _{CS}	25	35	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	15	25	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	10	20	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

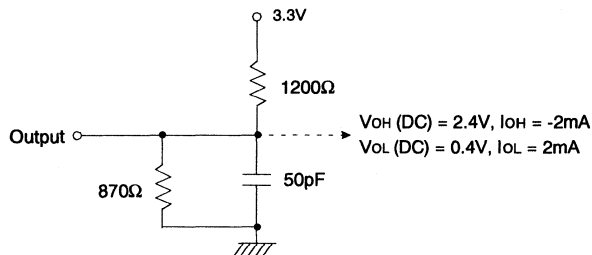
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	I _{CC1}	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		1,200	1,120	1,120	mA	1
Precharge standby current in power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), tcc = 15ns		16			mA	
	I _{CC2PS}	CKE & CLK ≤ V _{IL} (max), tcc = ∞		16				
Precharge standby current in non power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), CS ≥ V _{IH} (min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I _{CC2NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), tcc = ∞ Input signals are stable		112				
Active standby current in power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), tcc = 15ns		80			mA	
	I _{CC3PS}	CKE & CLK ≤ V _{IL} (max), tcc = ∞		80				
Active standby current in non power-down mode (One bank active)	I _{CC3N}	CKE ≥ V _{IH} (min), CS ≥ V _{IH} (min), tcc = 15ns Input signals are changed one time during 30ns		480			mA	
	I _{CC3NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), tcc = ∞ Input signals are stable		320			mA	
Operating current (Burst mode)	I _{CC4}	IOL = 0 mA Page burst 2Banks activated tCCD = 2CLKs	3	1,440	1,240	1,240	mA	1
			2	1,160	1,240	1,160		
Refresh current	I _{CC5}	trc ≥ trc(min)		3,200			mA	2
Self refresh current	I _{CC6}	CKE ≤ 0.2V		24			mA	

Notes : 1. Measured with outputs open.

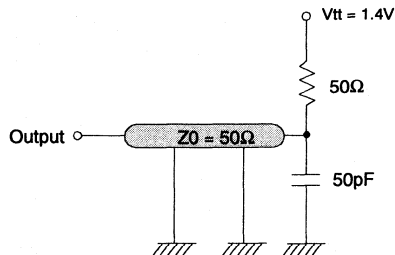
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4	
	CAS latency=2	1					

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set		H	X	L	L	L	L	X	OP code		1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	L		3									
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X		6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

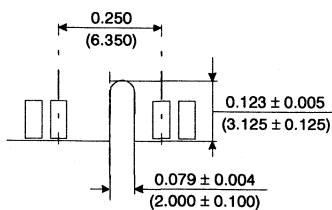
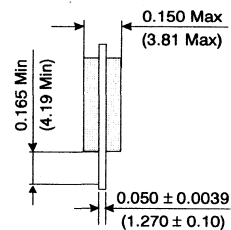
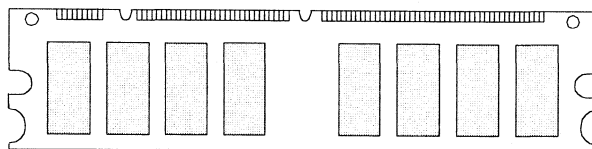
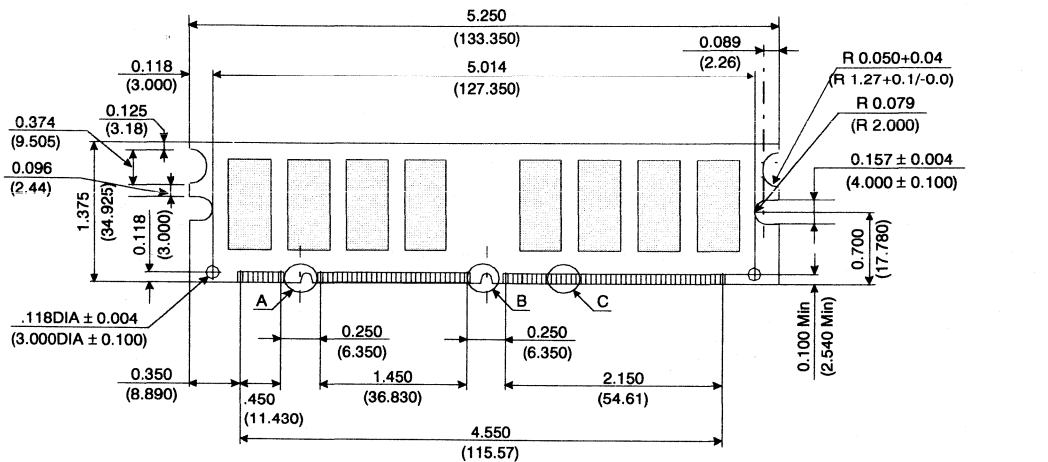
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

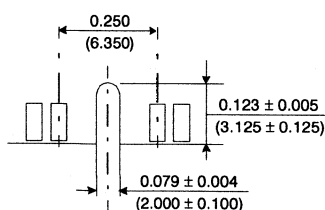
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

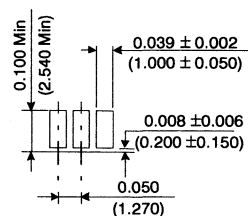
Units : Inches (Millimeters)



Detail A



Detail B



Detail C

Tolerances : ± .005(.13) unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
 SDRAM Part No. : K4S280832M

M366S3323MT0-C80/C1H/C1L

- Organization : 32Mx64
- Composition : 16Mx8 *16
- Used component part # : K4S280832M-TC80/C1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of S ² D memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

SERIAL PRESENCE DETECT

PC100 Unbuffered DIMM

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			11h	17h	47h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	3			33h			
80	 Manufacturer part # (Module depth)	3			33h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	M			4Dh			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	 Manufacturer revision code (For component)	M-die (1st Gen.)			4Dh			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S3323MT0 SDRAM DIMM

32Mx72 SDRAM DIMM with ECC based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S3323MT0 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S3323MT0 consists of eighteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S3323MT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S3323MT0-C80	125MHz (8ns @ CL=3)
M374S3323MT0-C1H	100MHz (10ns @ CL=2)
M374S3323MT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

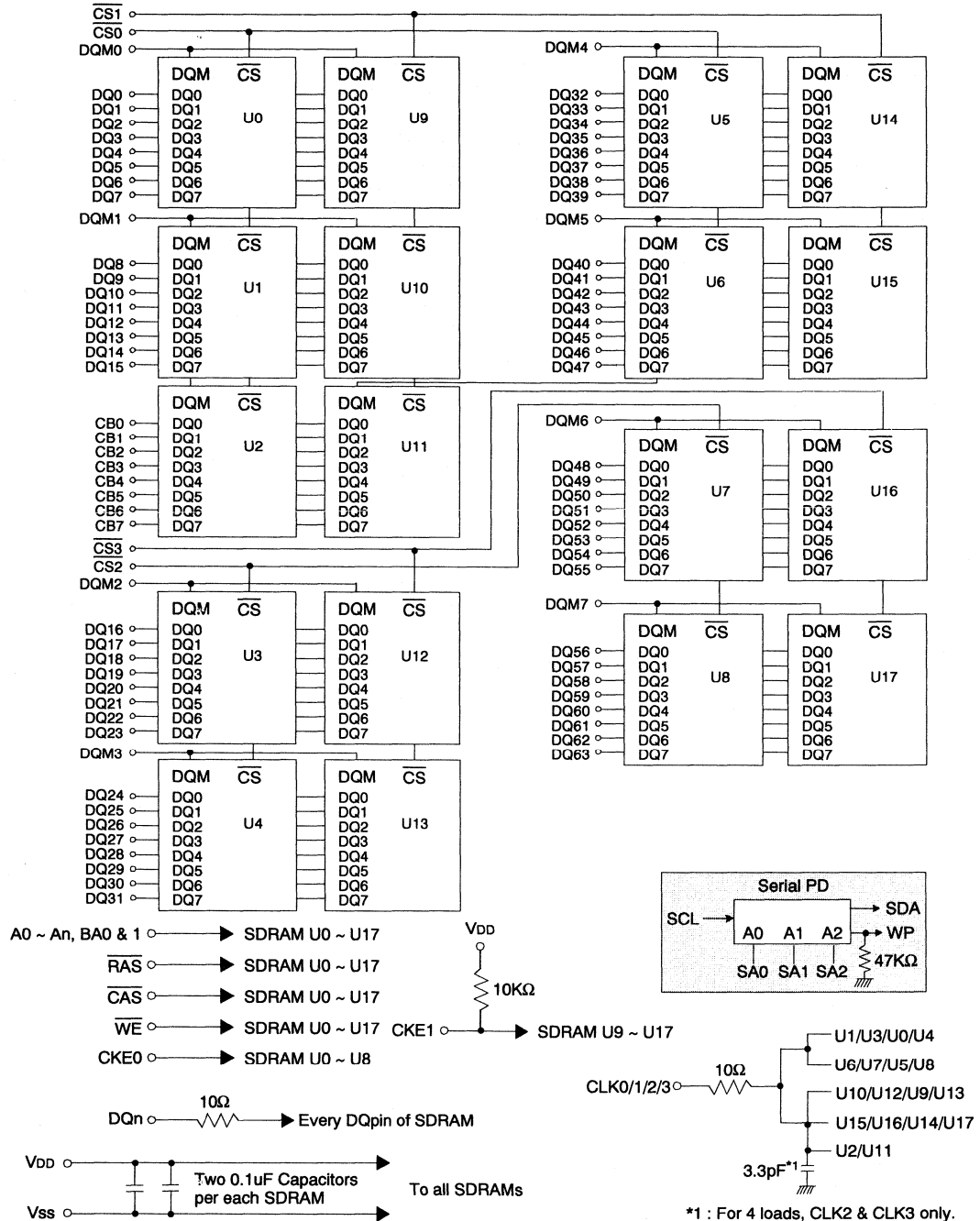
* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
Vdd/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-18	-	18	uA	3
Input leakage current (I/O pins)	I _{IL}	-3	-	3	uA	3,4

- Notes :**
1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 4. Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, 0V ≤ V_{OUT} ≤ VDDQ.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	CADD	65	95	pF
RAS, CAS, WE	CIN	65	95	pF
CKE (CKE0 ~ CKE1)	CCKE	40	60	pF
Clock (CLK0 ~ CLK3)	CCLK	30	40	pF
CS (CS0 ~ CS3)	CCS	30	40	pF
DQM (DQM0 ~ DQM7)	CDQM	15	25	pF
DQ (DQ0 ~ DQ63)	CDOUT1	10	20	pF
CB (CB0 ~ CB7)	CDOUT2	10	20	pF

DC CHARACTERISTICS

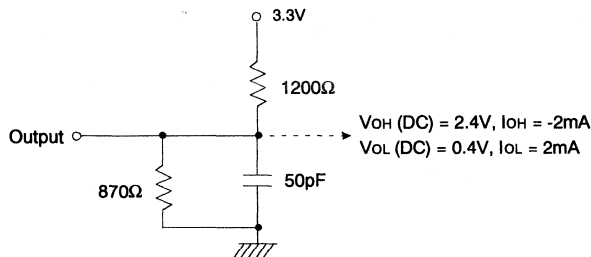
(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		1,350	1,260	1,260	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 15ns		18			mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞		18				
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		270			mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		126				
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 15ns		90			mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞		90				
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 15ns Input signals are changed one time during 30ns		540			mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		360			mA	
Operating current (Burst mode)	Icc4	IOL = 0 mA Page burst 2Banks activated tccd = 2CLKs	3	1,620	1,390	1,390	mA	1
			2	1,300	1,390	1,300		
Refresh current	Icc5	trc ≥ trc(min)		3,600			mA	2
Self refresh current	Icc6	CKE ≤ 0.2V		27			mA	

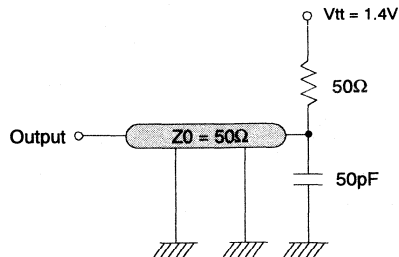
- Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4	
	CAS latency=2	1					

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1,2
	CAS latency=2			6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X	X	3	
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

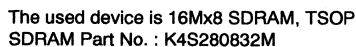
Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Units : Inches (Millimeters)



M374S3323MT0-C80/C1H/C1L

- Organization : 32Mx72
- Composition : 16Mx8 *18
- Used component part # : K4S280832M-TC80/C1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	72 bits			48h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			23h	29h	59h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	7			37h			
77	 Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	3			33h			
80	 Manufacturer part # (Module depth)	3			33h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	M			4Dh			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	 Manufacturer revision code (For component)	M-die (1st Gen.)			4Dh			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M366S1723ATS SDRAM DIMM

16Mx64 SDRAM DIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1723ATS is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1723ATS consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.22 uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S1723ATS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S1723ATS-C80	125MHz (8ns @ CL=3)
M366S1723ATS-C1H	100MHz (10ns @ CL=2)
M366S1723ATS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

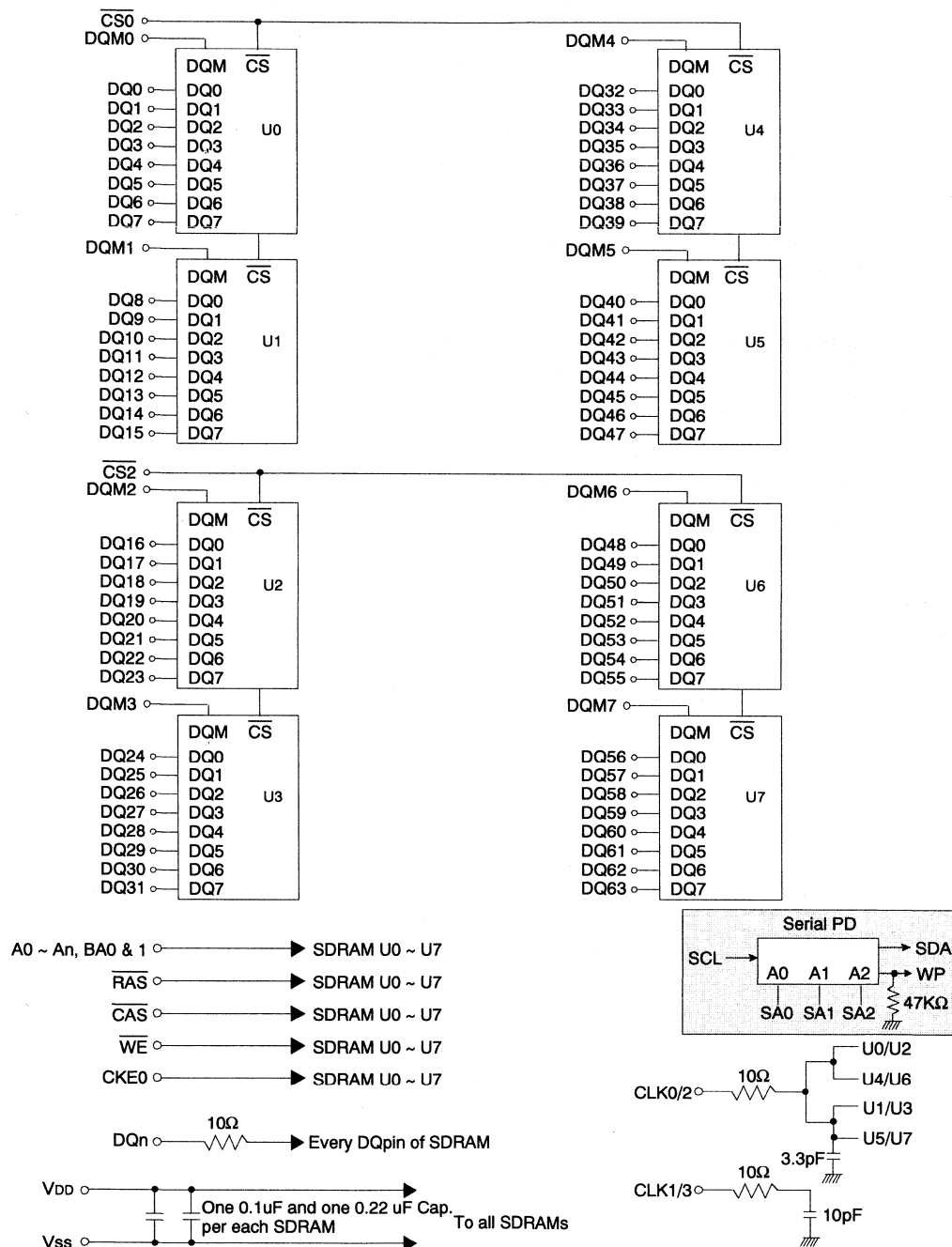
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	CADD	25	45	pF
RAS, CAS, WE	CIN	25	45	pF
CKE (CKE0)	CCKE	25	45	pF
Clock (CLK0, CLK2)	CCLK	15	21	pF
CS (CS0, CS2)	Ccs	15	25	pF
DQM (DQM0 ~ DQM7)	CDQM	8	12	pF
DQ (DQ0 ~ DQ63)	COUT	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	I _{CC1}	Burst length = 1 trc ≥ trc(min) Io = 0 mA	960	880	880	mA	1
Precharge standby current in power-down mode	I _{CC2P}	CKE ≤ VIL(max), tcc = 10ns	8			mA	
	I _{CC2PS}	CKE & CLK ≤ VIL(max), tcc = ∞	8				
Precharge standby current in non power-down mode	I _{CC2N}	CKE ≥ VIH(min), $\overline{CS} \geq V_{IH}(\min)$, tcc = 10ns Input signals are changed one time during 20ns	160			mA	
	I _{CC2NS}	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	56				
Active standby current in power-down mode	I _{CC3P}	CKE ≤ VIL(max), tcc = 10ns	40			mA	
	I _{CC3PS}	CKE & CLK ≤ VIL(max), tcc = ∞	40				
Active standby current in non power-down mode (One bank active)	I _{CC3N}	CKE ≥ VIH(min), $\overline{CS} \geq V_{IH}(\min)$, tcc = 10ns Input signals are changed one time during 20ns	240			mA	
	I _{CC3NS}	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	160			mA	
Operating current (Burst mode)	I _{CC4}	Io = 0 mA Page burst 4Banks activated tCCD = 2CLKs	1,160	1,000	1,000	mA	1
Refresh current	I _{CC5}	trc ≥ trc(min)	1,760	1,680	1,680	mA	2
Self refresh current	I _{CC6}	CKE ≤ 0.2V	12			mA	

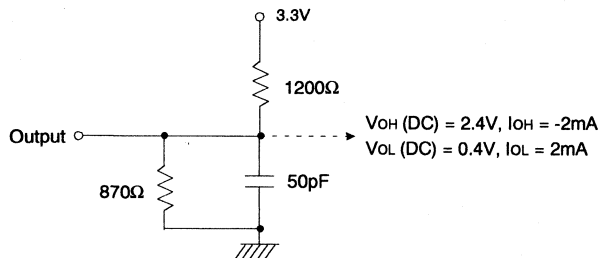
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

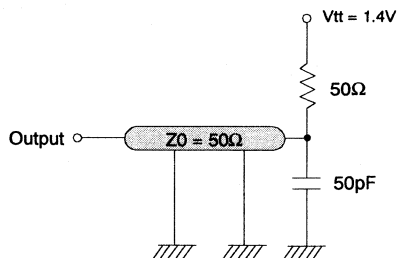
3. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4	
	CAS latency=2	-	1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .

SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

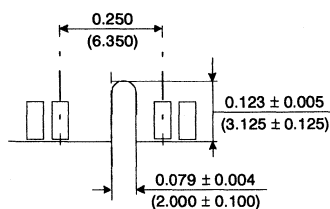
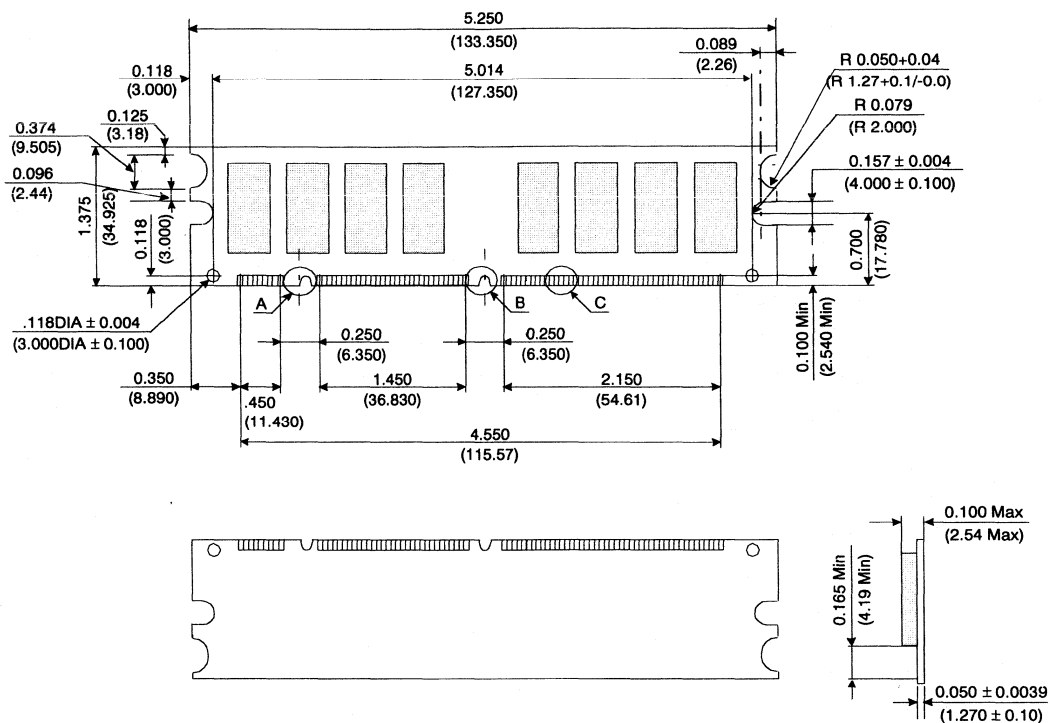
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

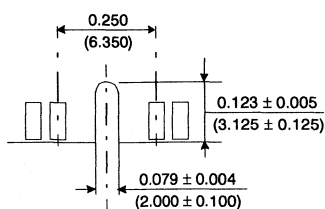
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

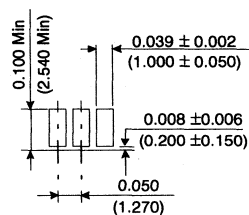
Units : Inches (Millimeters)



Detail A



Detail B



Detail C

Tolerances : $\pm .005$ (.13) unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832A

M366S1723ATS-C80/C1H/C1L

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832A-TC80/C1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuration type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			10h	16h	46h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	 Manufacturer part # (Module depth)	7			37h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	A			41h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M374S1723ATS SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S1723ATS is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S1723ATS consists of nine CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.22 uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S1723ATS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S1723ATS-C80	125MHz (8ns @ CL=3)
M374S1723ATS-C1H	100MHz (10ns @ CL=2)
M374S1723ATS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/A9	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	*CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

- * These pins are not used in this module.
 ** These pins should be NC in the system which does not support SPD.

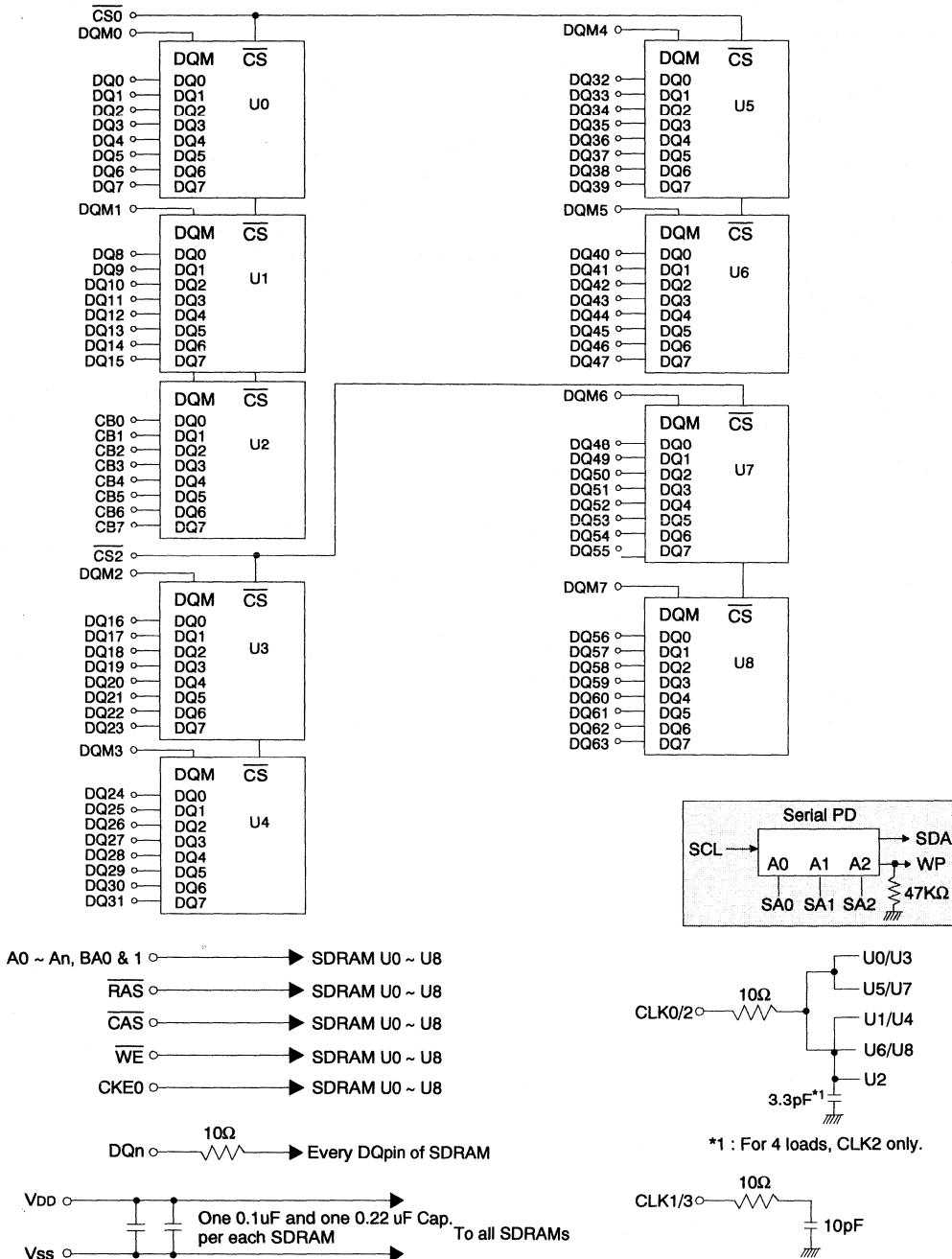
* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Check bit	Check bits for ECC.
WP	Write protection	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	28	50	pF
RAS, CAS, WE	C _{IN}	28	50	pF
CKE (CKE0)	C _{CKE}	28	50	pF
Clock (CLK0, CLK2)	C _{CLK}	18	25	pF
CS (CS0, CS2)	C _{CS}	18	30	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	8	10	pF
DQ (DQ0 ~ DQ63)	C _{OUT1}	9	12	pF
CB (CB0 ~ CB7)	C _{OUT2}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,080	990	990	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	9			mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	9				
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	180			mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	63				
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	45			mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	45				
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	270			mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	180			mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,305	1,125	1,125	mA	1
Refresh current	Icc5	trc ≥ trc(min)	1,980	1,890	1,890	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	14			mA	

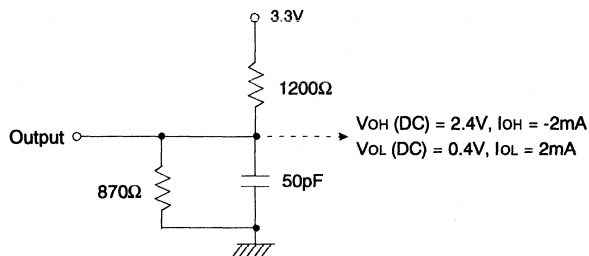
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

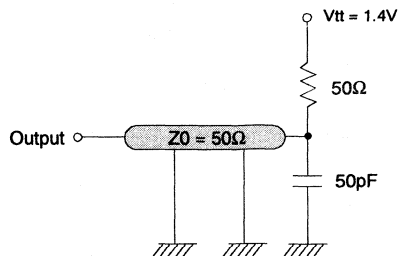
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4	
	CAS latency=2	-	1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L, $t_{RD}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .

SAMSUNG recommends $t_{RD}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1, 2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

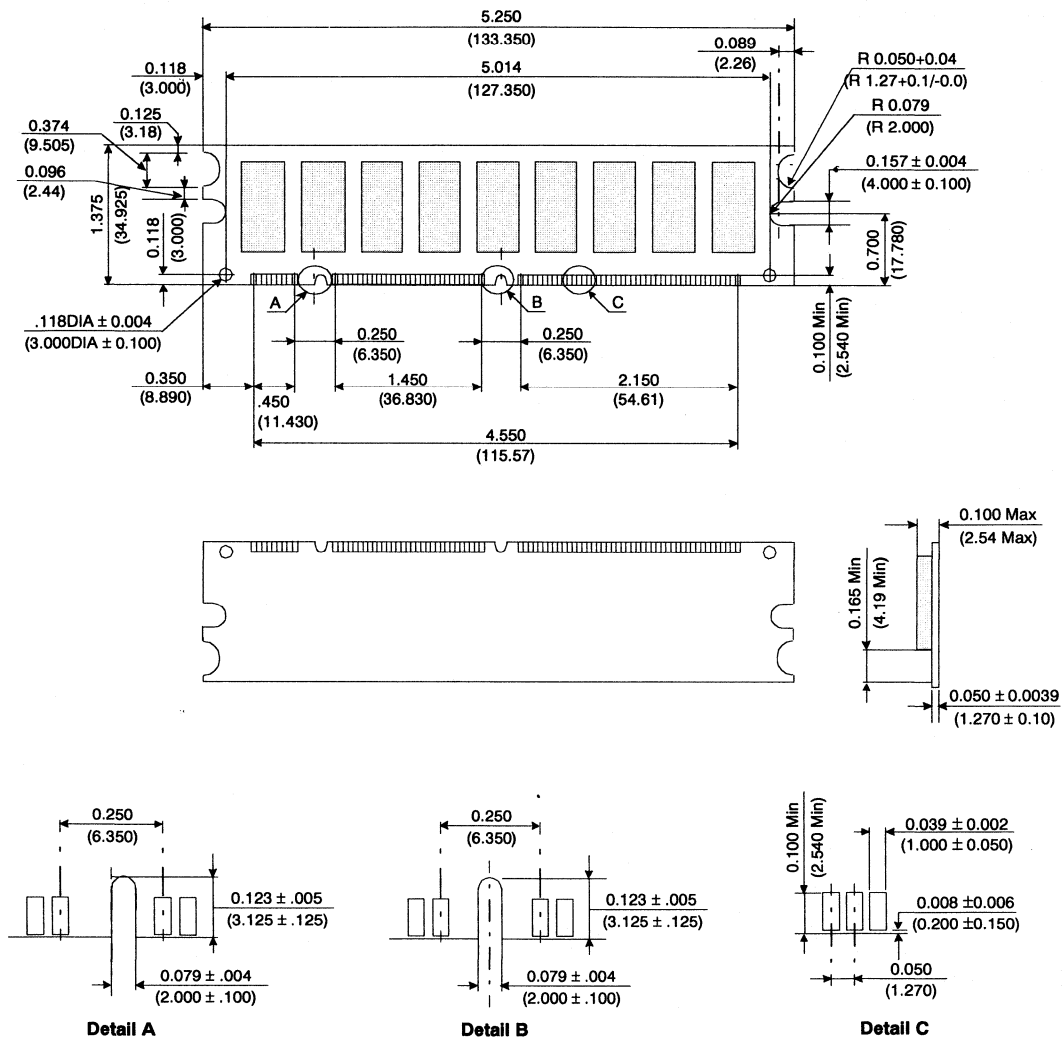
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC100 Unbuffered DIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832A

M374S1723ATS-C80/C1H/C1L

- Organization : 16Mx72
- Composition : 16Mx8 *9
- Used component part # : K4S280832A-TC80/C1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	72 bits			48h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			22h	28h	58h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	7			37h			
77	 Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	 Manufacturer part # (Module depth)	7			37h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	A			41h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M366S3323AT0 SDRAM DIMM

32Mx64 SDRAM DIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S3323AT0 is a 32M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S3323AT0 consists of sixteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S3323AT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S3323AT0-C80	125MHz (8ns @ CL=3)
M366S3323AT0-C1H	100MHz (10ns @ CL=2)
M366S3323AT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

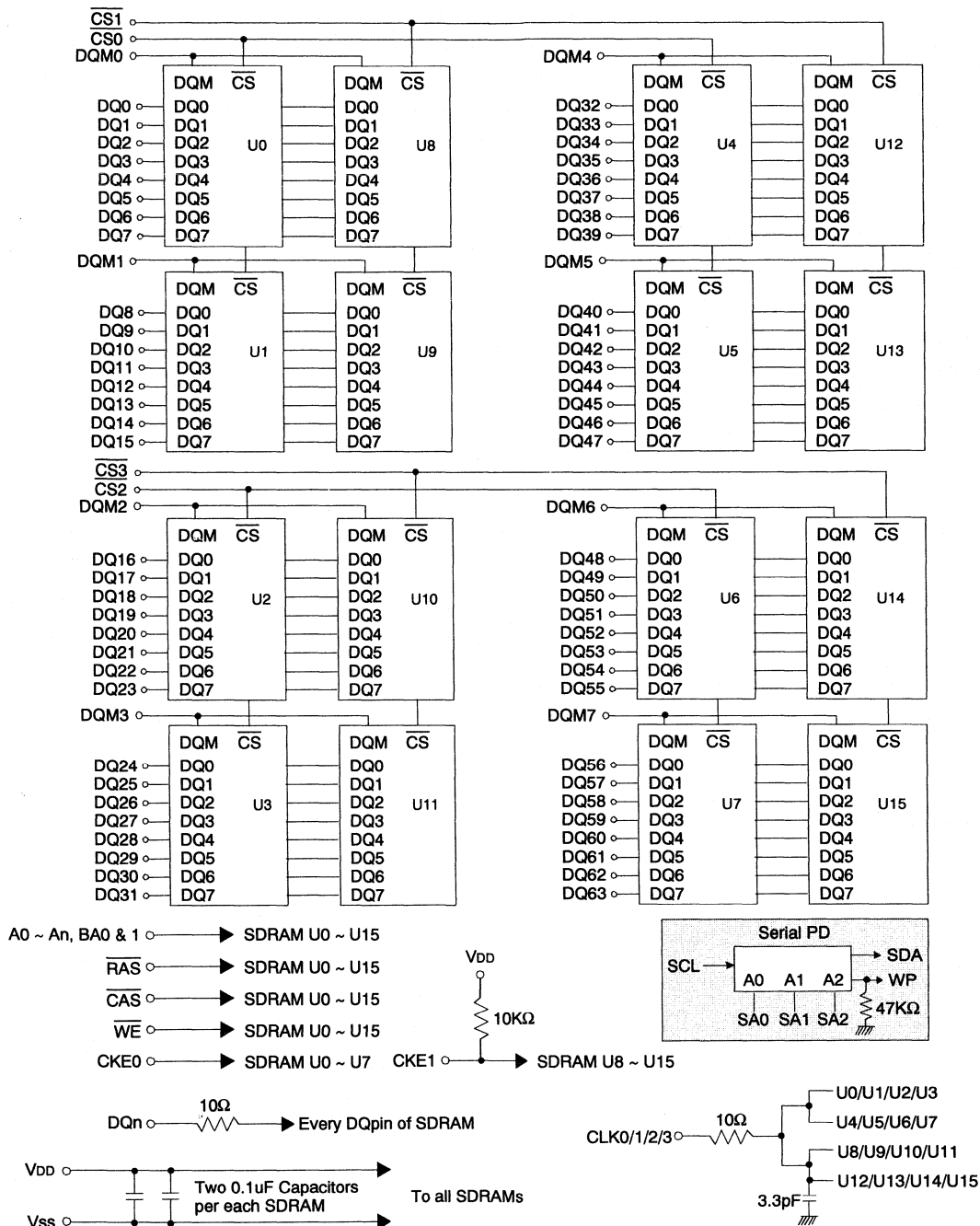
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	16	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	45	85	pF
RAS, CAS, WE	C _{IN}	45	85	pF
CKE (CKE0 ~ CKE1)	C _{CKE}	25	45	pF
Clock (CLK0 ~ CLK3)	C _{CLK}	15	21	pF
CS (CS0 ~ CS3)	C _{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	10	15	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	13	18	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,200	1,120	1,120	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	16			mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	16				
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	320			mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	112				
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	80			mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	80				
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	480			mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	320			mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,440	1,240	1,240	mA	1
Refresh current	Icc5	trc ≥ trc(min)	2,000	1,920	1,920	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	24			mA	

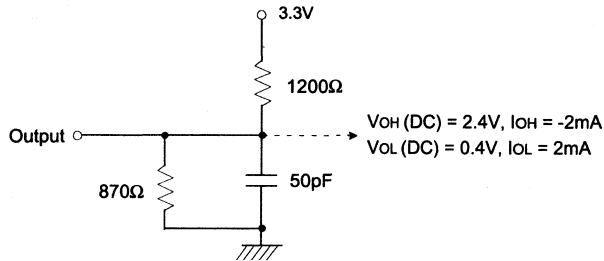
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

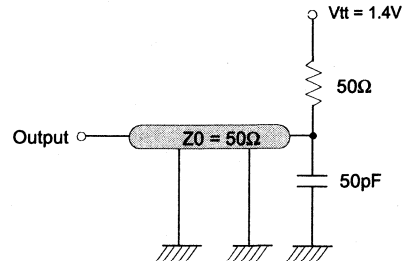
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4	
	CAS latency=2	-	1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .

SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.
 - Assumed input rise and fall time $(t_r \& t_f) = 1$ ns.
If $t_r \& t_f$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA _{0,1}	A ₁₀ /AP	A ₁₁ , A ₉ ~ A ₀	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A ₀ ~ A ₉)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A ₀ ~ A ₉)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

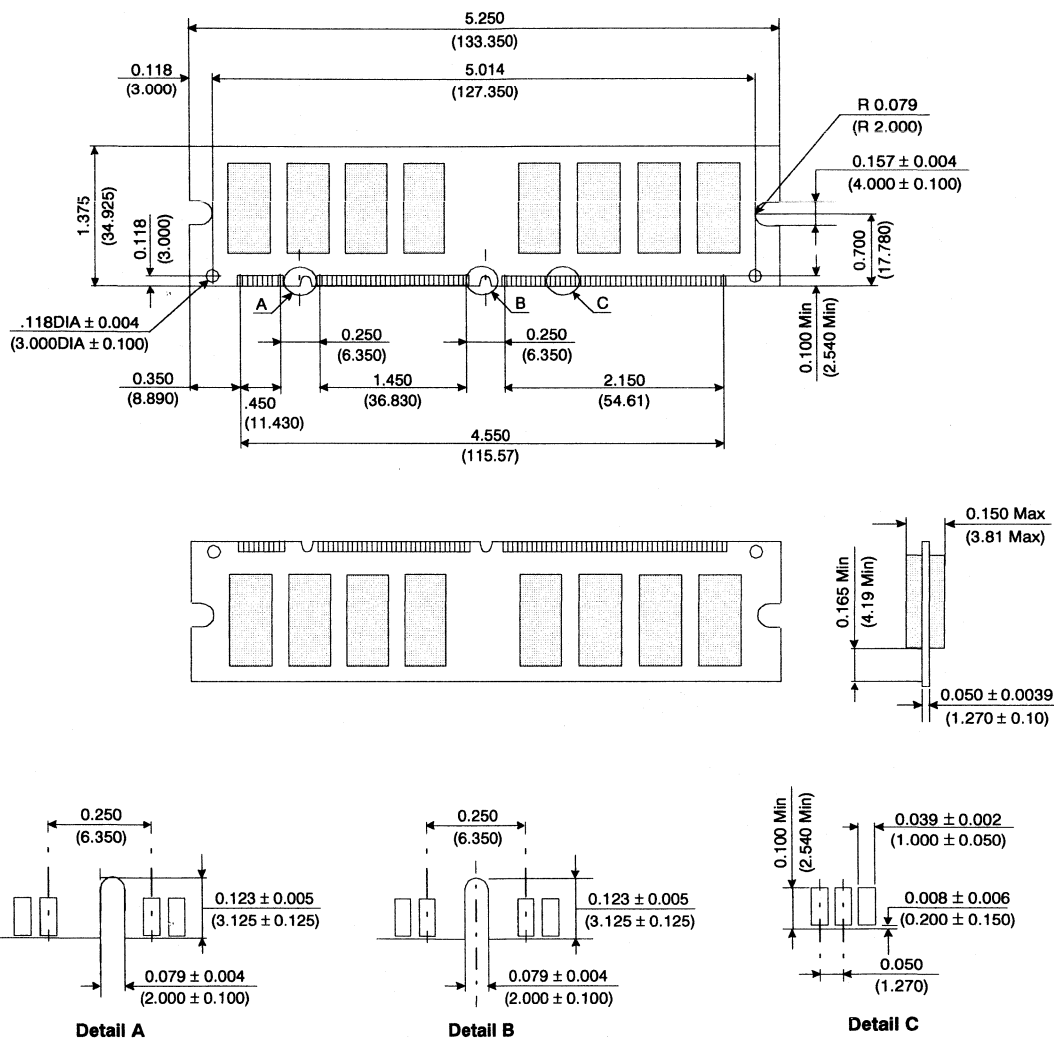
Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Units : Inches (Millimeters)



The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832A

M366S3323A70-C80/C1H/C1L

- Organization : 32Mx64
- Composition : 16Mx8 *16
- Used component part # : K4S280832A-TC80/C1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			11h	17h	47h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	3			33h			
80	 Manufacturer part # (Module depth)	3			33h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	A			41h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S3323AT0 SDRAM DIMM

32Mx72 SDRAM DIMM with ECC based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S3323AT0 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S3323AT0 consists of eighteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S3323AT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S3323AT0-C80	125MHz (8ns @ CL=3)
M374S3323AT0-C1H	100MHz (10ns @ CL=2)
M374S3323AT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

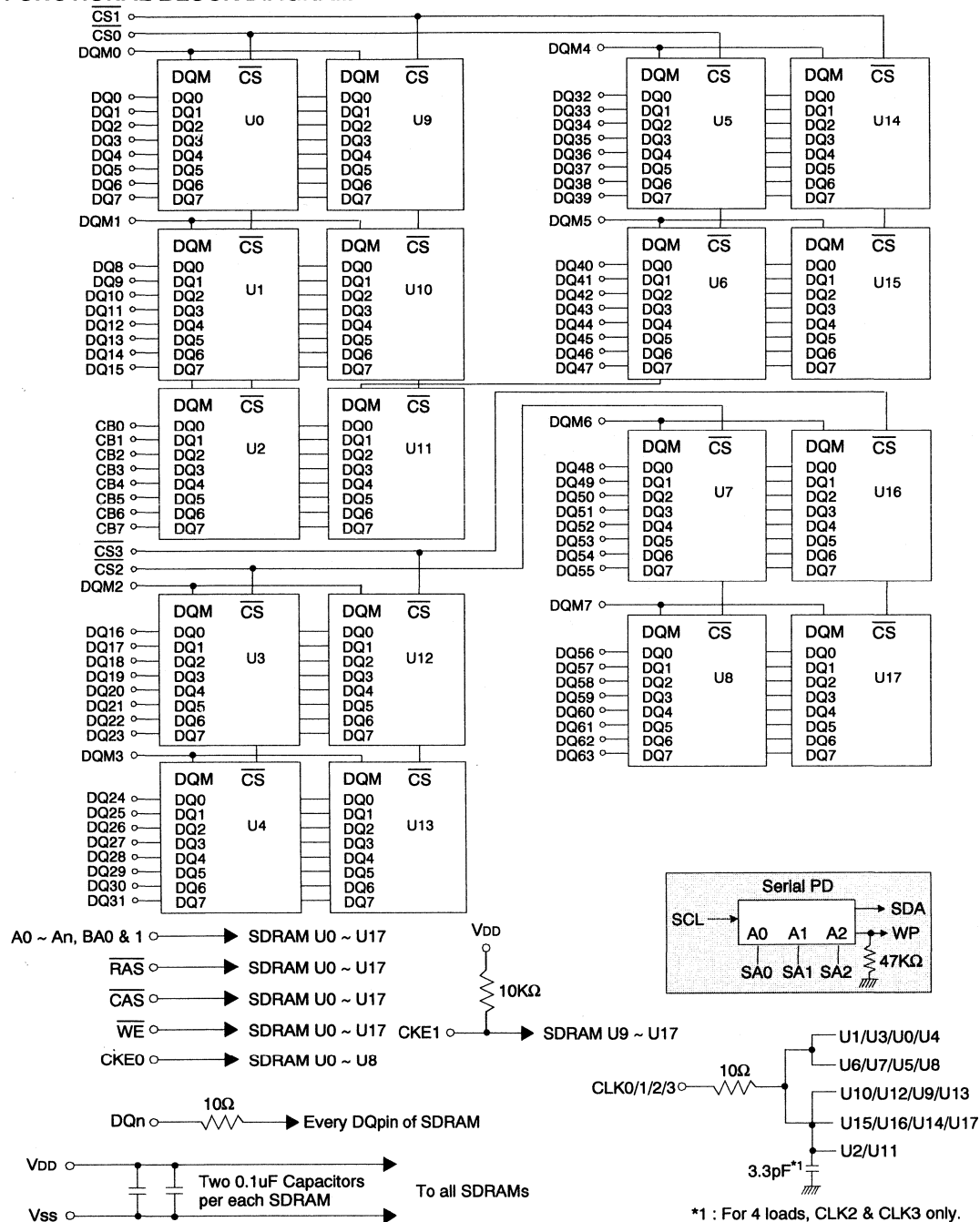
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	50	95	pF
RAS, CAS, WE	C _{IN}	50	95	pF
CKE (CKE0 ~ CKE1)	C _{CKE}	28	50	pF
Clock (CLK0 ~ CLK3)	C _{CLK}	18	25	pF
CS (CS0 ~ CS3)	C _{CS}	18	30	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	13	20	pF
DQ (DQ0 ~ DQ63)	C _{OUT1}	13	18	pF
CB (CB0 ~ CB7)	C _{OUT2}	13	18	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,350	1,260	1,260	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	18			mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	18				
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	360			mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	126				
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	90			mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	90				
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	540			mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	360			mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,575	1,395	1,395	mA	1
Refresh current	Icc5	trc ≥ trc(min)	2,250	2,160	2,160	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	27			mA	

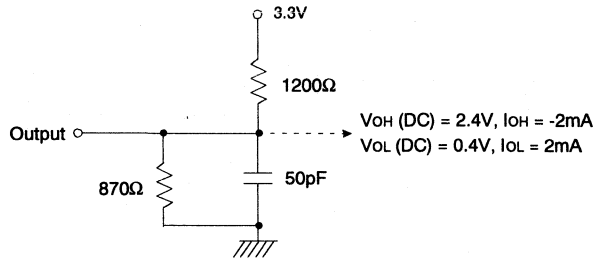
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

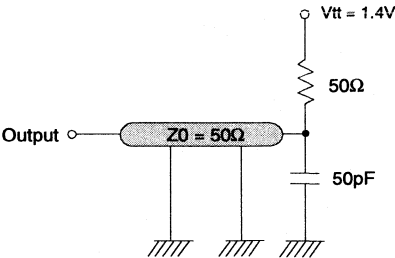
3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

- Notes :** 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
- SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	toH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time $(t_r \text{ \& } t_f) = 1$ ns.If $t_r \text{ \& } t_f$ is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
	H				X	X	X	3					
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

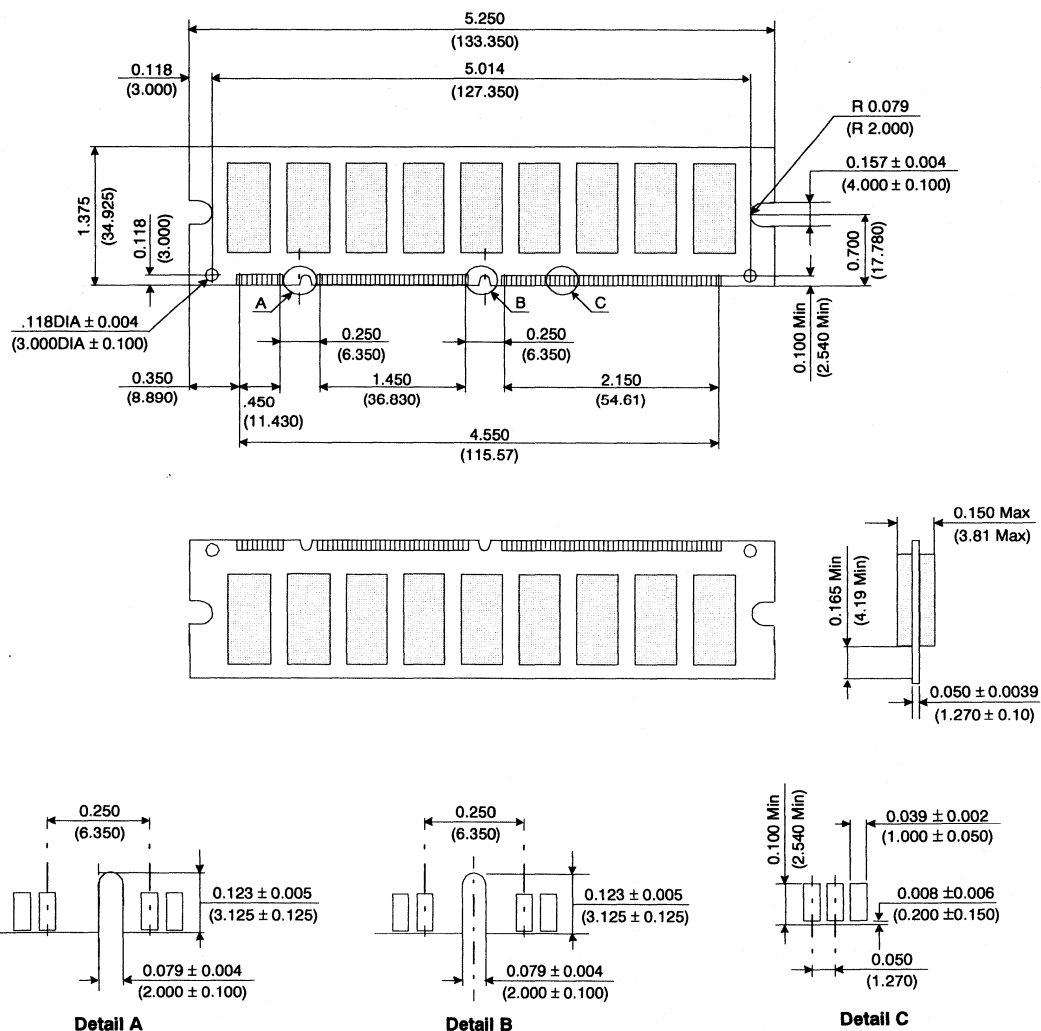
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)

Tolerances : ± 0.005 (.13) unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
 SDRAM Part No. : K4S280832A

M374S3323AT0-C80/C1H/C1L

- Organization : 32Mx72
- Composition : 16Mx8 *18
- Used component part # : K4S280832A-TC80/C1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	72 bits			48h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

SERIAL PRESENCE DETECT

PC100 Unbuffered DIMM

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			23h	29h	59h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	7			37h			
77	 Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	3			33h			
80	 Manufacturer part # (Module depth)	3			33h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	A			41h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M366S0924BTS SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S0924BTS is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S0924BTS consists of four CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S0924BTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S0924BTS-C80	125MHz (8ns @ CL=3)
M366S0924BTS-C1H	100MHz (10ns @ CL=2)
M366S0924BTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,000mil) , single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	*CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	Vdd	77	DQ31	105	*CB4	133	Vdd	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	Vdd	54	Vss	82	**SD	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

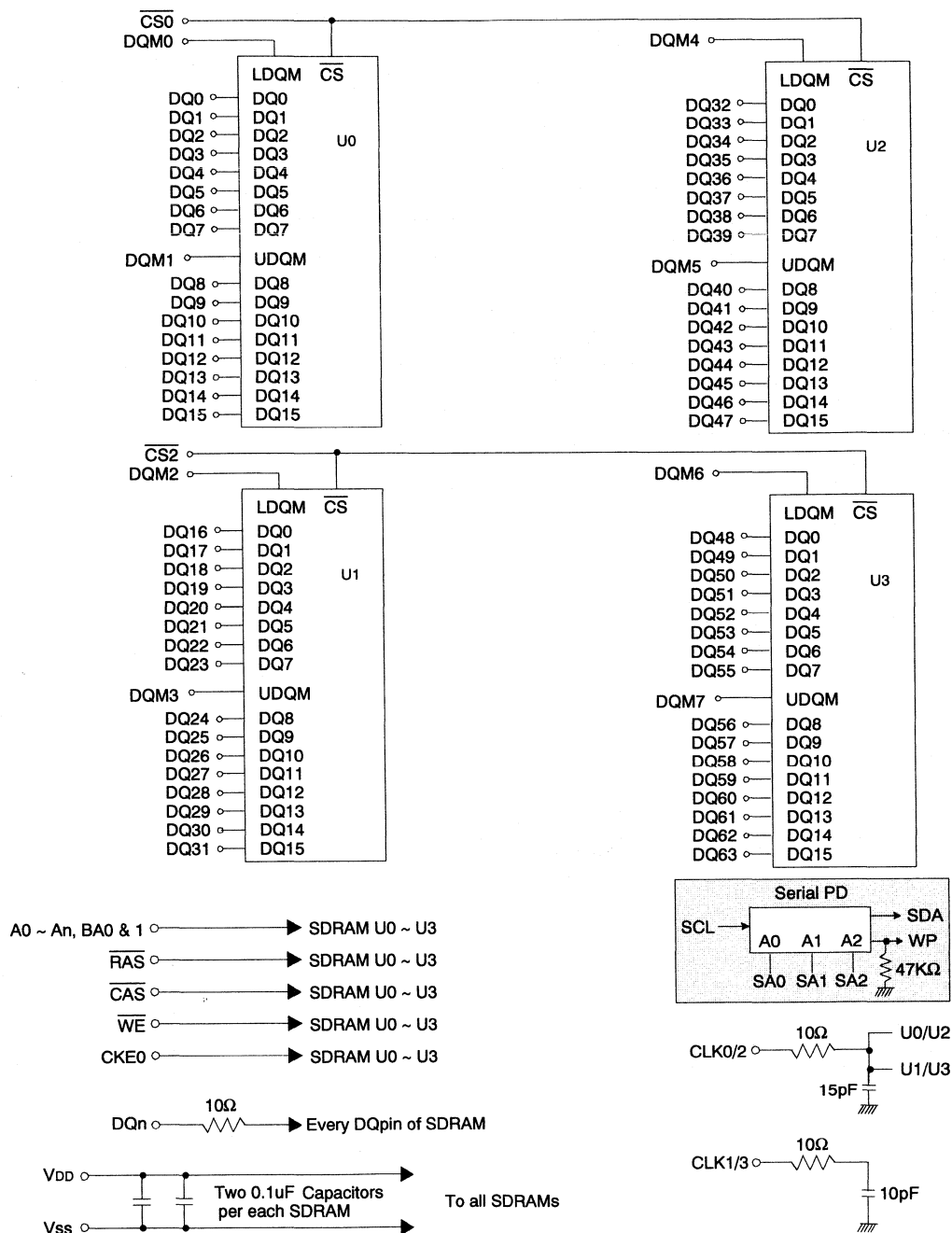
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{CS}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	4	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	CADD	15	25	pF
RAS, CAS, WE	CIN	15	25	pF
CKE (CKE0)	CCKE	15	25	pF
Clock (CLK0, CLK2)	CCLK	10	13	pF
CS (CS0, CS2)	CCS	10	15	pF
DQM (DQM0 ~ DQM7)	CDQM	8	10	pF
DQ (DQ0 ~ DQ63)	COUT	9	12	pF

DC CHARACTERISTICS

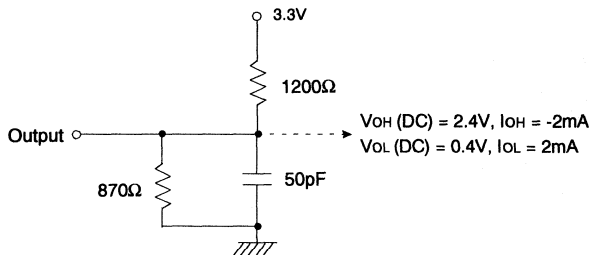
(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	600	560	560	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	4			mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	4				
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	80			mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	28				
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	20			mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	20				
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	120			mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	80			mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	680	580	580	mA	1
Refresh current	Icc5	trc ≥ trc(min)	880	840	840	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	6			mA	

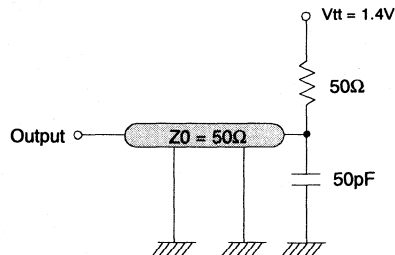
- Notes :**
1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .

SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H		4,5	
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H		4,5	
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

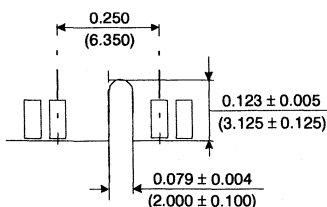
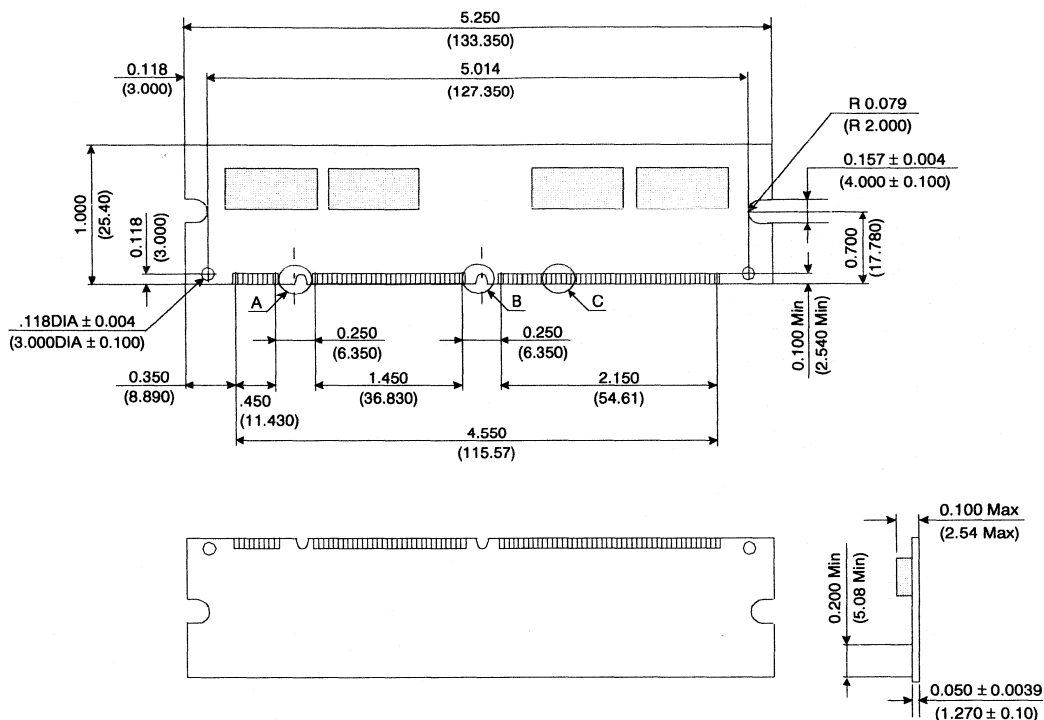
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

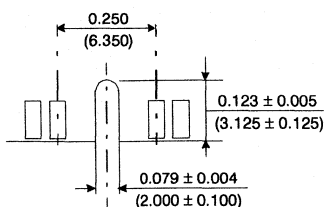
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

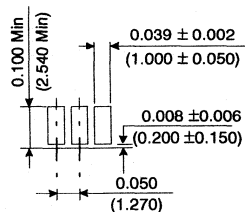
Units : Inches (Millimeters)



Detail A



Detail B



Detail C

Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
 SDRAM Part No. : K4S281632B

M366S0924BTS-C80/C1H/C1L

- Organization : 8Mx64
- Composition : 8Mx16 *4
- Used component part # : K4S281632B-TC80/C1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec.Ver.1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			07h	0Dh	3Dh	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	0			30h			
80	 Manufacturer part # (Module depth)	9			39h			
81	Manufacturer part # (Refresh, # of banks in Comp. & Interface)	2			32h			
82	Manufacturer part # (Composition component)	4			34h			
83	Manufacturer part # (Component revision)	B			42h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsung's own purpose.

M366S1724BT0 SDRAM DIMM

16Mx64 SDRAM DIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1724BT0 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1724BT0 consists of eight CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S1724BT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S1724BT0-C80	125MHz (8ns @ CL=3)
M366S1724BT0-C1H	100MHz (10ns @ CL=2)
M366S1724BT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

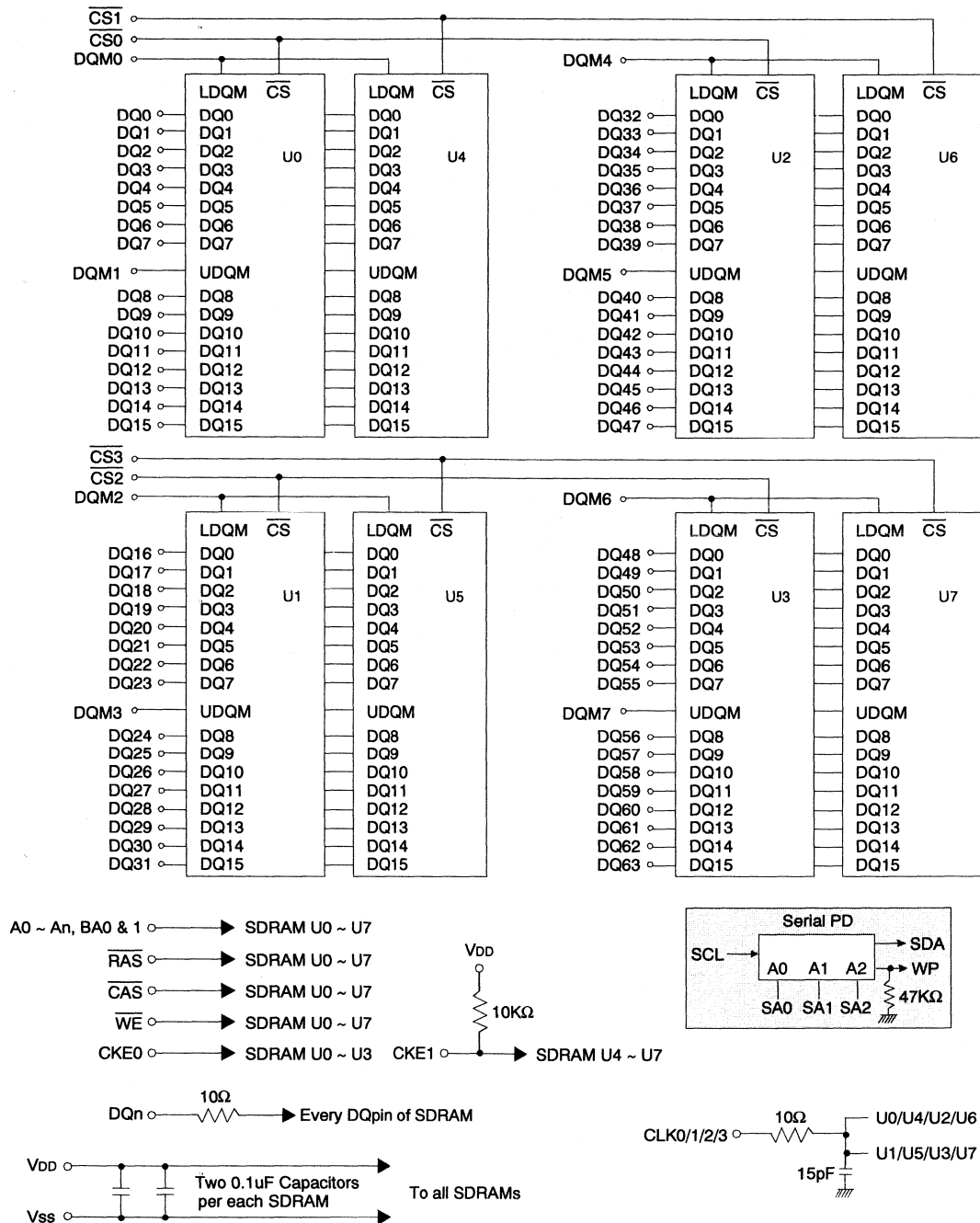
** These pins should be NC in the system which does not support SPD.

* SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	μA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	25	45	pF
RAS, CAS, WE	C _{IN}	25	45	pF
CKE (CKE0)	C _{CKE}	15	25	pF
Clock (CLK0, CLK2)	C _{CLK}	10	13	pF
CS (CS0, CS2)	C _{CS}	10	15	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	8	10	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	9	12	pF

DC CHARACTERISTICS(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	720	680	680	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	8			mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	8				
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	160			mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	56				
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	40			mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	40				
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	240			mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	160			mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	800	700	700	mA	1
Refresh current	Icc5	trc ≥ trc(min)	1,000	960	960	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	12			mA	

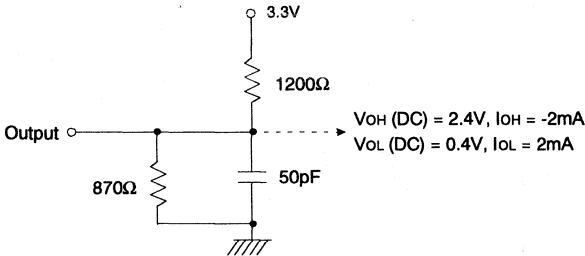
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

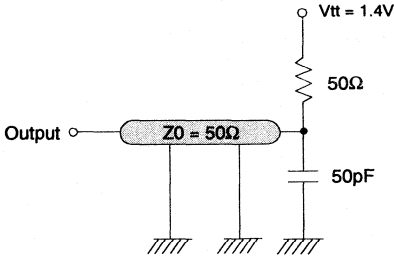
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (V _{Ih} /V _{Il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

- Notes :** 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L, t_{RDL}=1CLK and t_{DAL}=1CLK+20ns is also supported .
- SAMSUNG recommends t_{RDL}=2CLK and t_{DAL}=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1, 2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L	L	L	L	H	X	X		3	
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

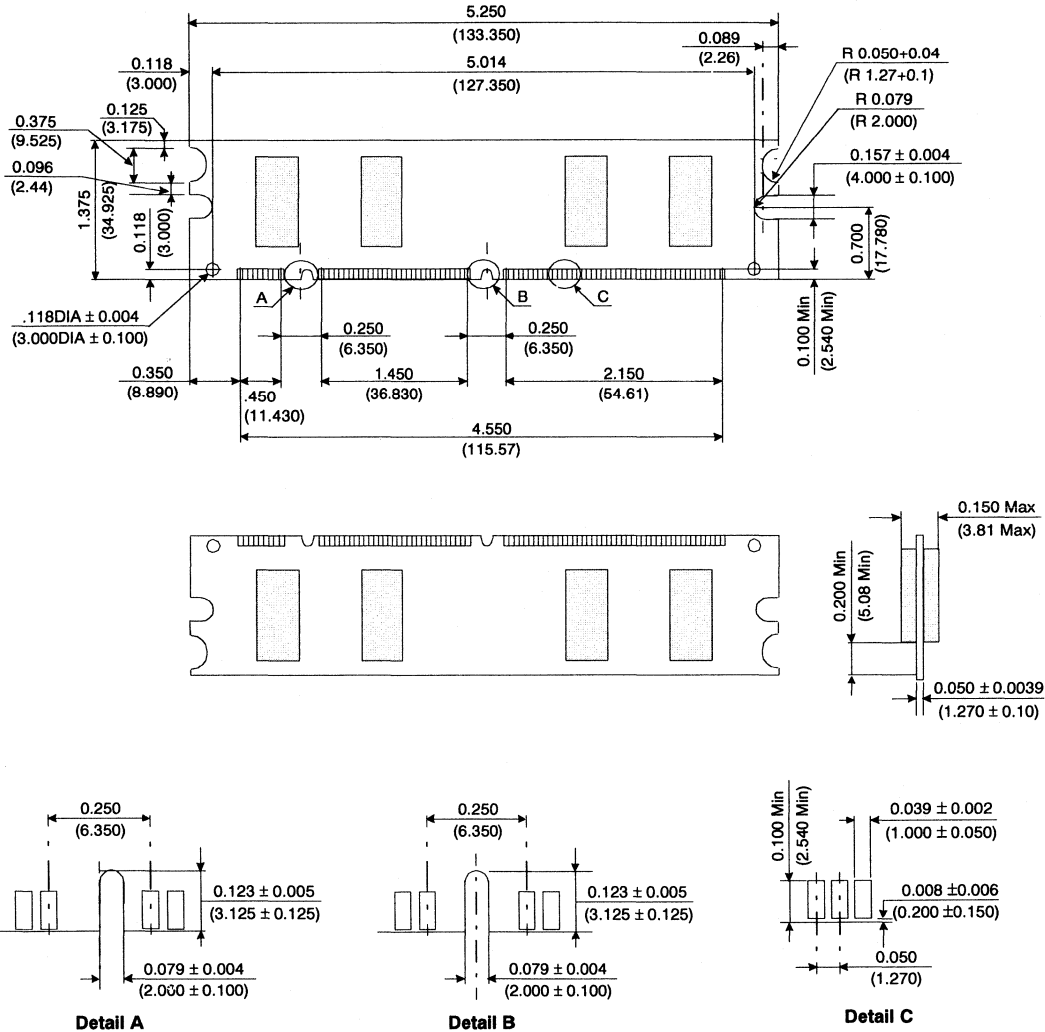
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
SDRAM Part No. : K4S281632B

M366S1724BT0-C80/C1H/C1L

- Organization : 16Mx64
- Composition : 8Mx16 *8
- Used component part # : K4S281632B-TC80/C1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 64MB			10h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			08h	0Eh	3Eh	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	 Manufacturer part # (Module depth)	7			37h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	4			34h			
83	Manufacturer part # (Component revision)	B			42h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S1723BTS SDRAM DIMM

16Mx64 SDRAM DIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1723BTS is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1723BTS consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.22 uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S1723BTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S1723BTS-C80	125MHz (8ns @ CL=3)
M366S1723BTS-C1H	100MHz (10ns @ CL=2)
M366S1723BTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

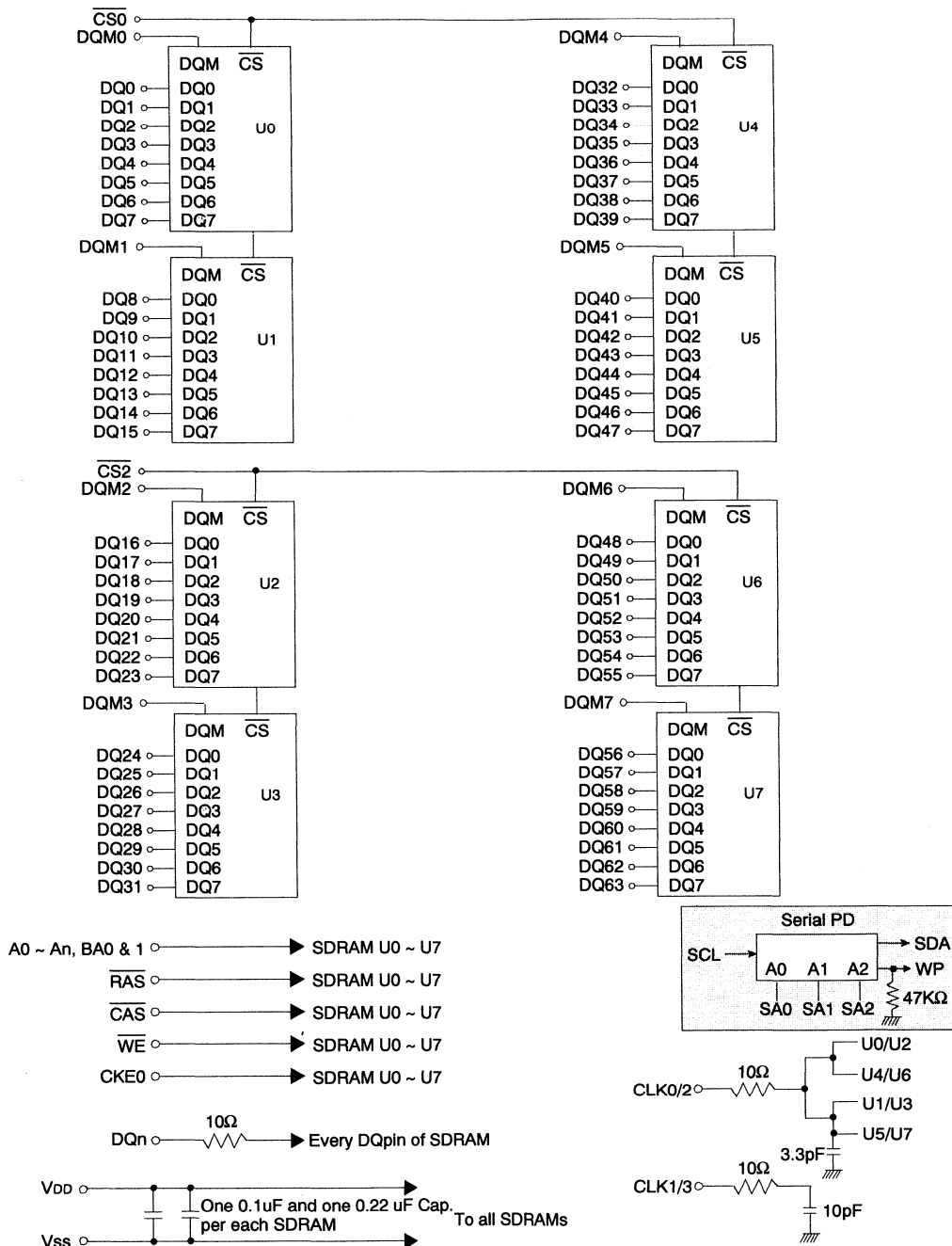
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	25	45	pF
RAS, CAS, WE	C _{IN}	25	45	pF
CKE (CKE0)	C _{CKE}	25	45	pF
Clock (CLK0, CLK2)	C _{CLK}	15	21	pF
CS (CS0, CS2)	C _{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	8	12	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	9	12	pF

DC CHARACTERISTICS(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	960	880	880	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	8			mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	8				
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	160			mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	56				
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	40			mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	40				
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	240			mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	160			mA	
Operating current (Burst mode)	ICC4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,160	1,000	1,000	mA	1
Refresh current	ICC5	trc ≥ trc(min)	1,760	1,680	1,680	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	12			mA	

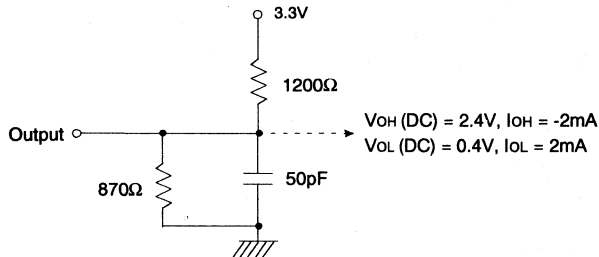
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

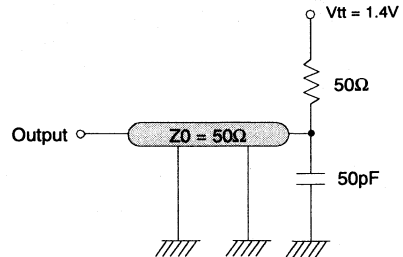
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -80/1H/1L, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .
SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3	
	Entry		L									3	
	Self refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable									H		4,5	
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable									H		4,5	
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X		
	All banks								X	H			
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

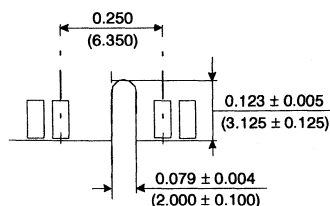
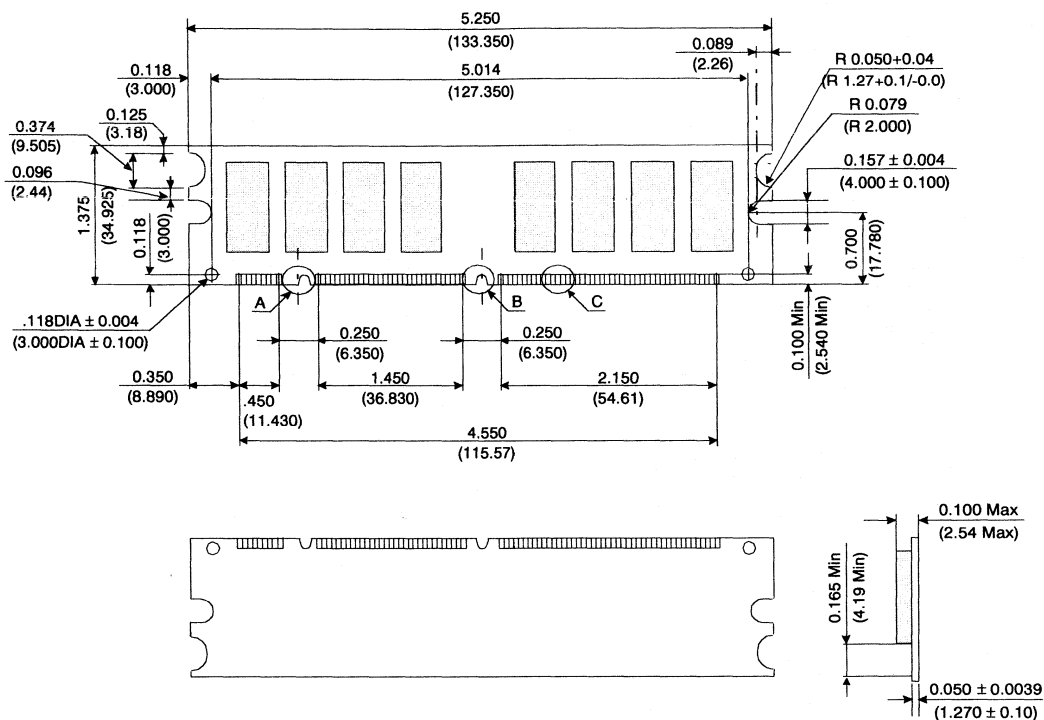
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

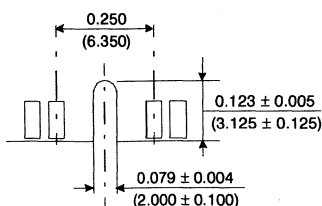
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

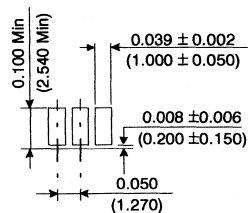
Units : Inches (Millimeters)



Detail A



Detail B



Detail C

Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832B

M366S1723BTS-C80/C1H/C1L

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832B-TC80/C1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1 CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			10h	16h	46h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	 Manufacturer part # (Module depth)	7			37h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	B			42h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S1723BTS SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S1723BTS is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S1723BTS consists of nine CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.22 uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S1723BTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S1723BTS-C80	125MHz (8ns @ CL=3)
M374S1723BTS-C1H	100MHz (10ns @ CL=2)
M374S1723BTS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

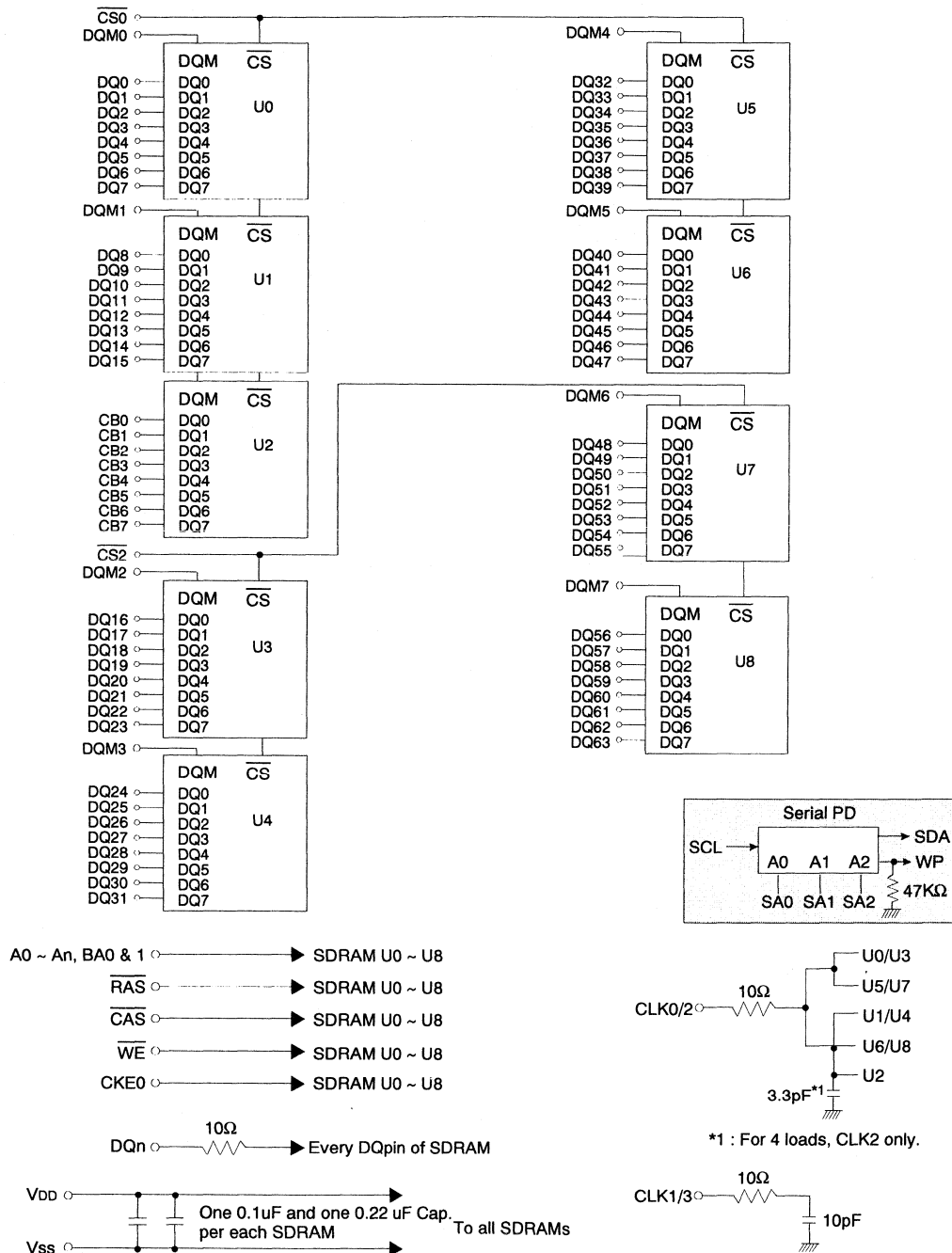
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ VDDQ.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	28	50	pF
RAS, CAS, WE	C _{IN}	28	50	pF
CKE (CKE0)	C _{CKE}	28	50	pF
Clock (CLK0, CLK2)	C _{CLK}	18	25	pF
CS (CS0, CS2)	C _{CS}	18	30	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	8	10	pF
DQ (DQ0 ~ DQ63)	C _{OUT1}	9	12	pF
CB (CB0 ~ CB7)	C _{OUT2}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,080	990	990	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	9			mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	9				
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	180			mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	63				
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	45			mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	45				
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	270			mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	180			mA	
Operating current (Burst mode)	ICC4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,305	1,125	1,125	mA	1
Refresh current	ICC5	trc ≥ trc(min)	1,980	1,890	1,890	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	14			mA	

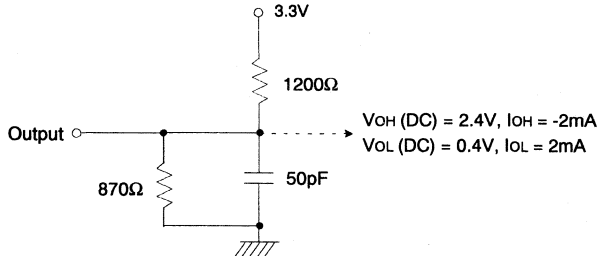
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

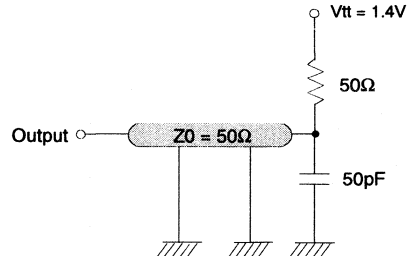
3. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .

SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsac		6		6		6	ns	1, 2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	toH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tss	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	L		L	L	H	X	X	X	X	3		
		Exit	L	H	L	H	H	H	X	X	3		
					H	X	X	X			3		
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H		4,5	
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H		4,5	
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

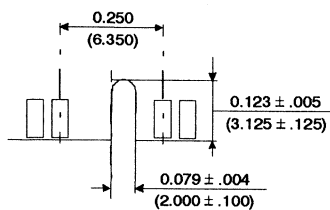
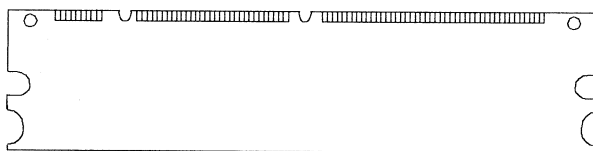
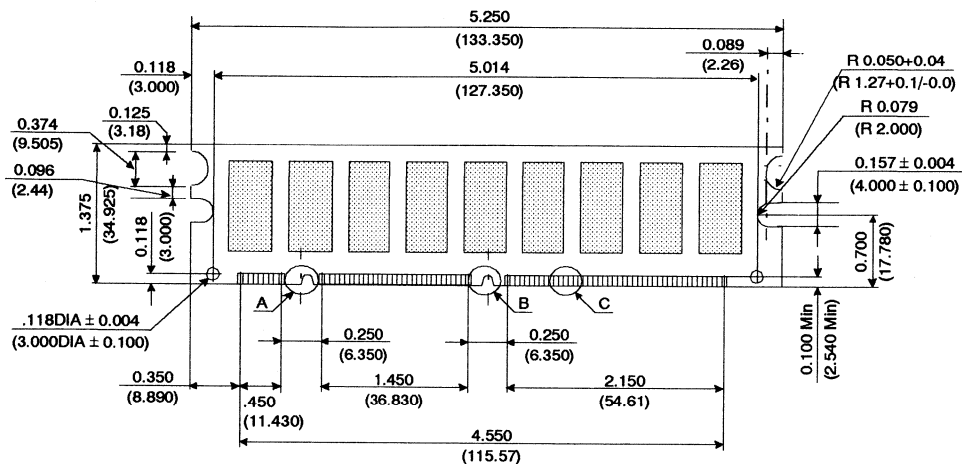
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

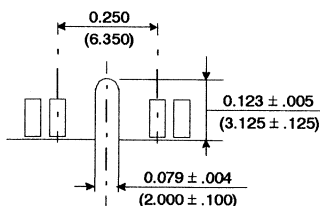
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

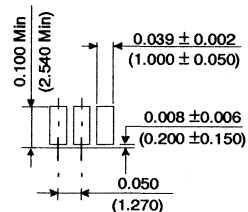
Units : Inches (Millimeters)



Detail A



Detail B



Detail C

Tolerances : ± .005(.13) unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
 SDRAM Part No. : K4S280832B

M374S1723BTS-C80/C1H/C1L

- Organization : 16Mx72
- Composition : 16Mx8 *9
- Used component part # : K4S280832B-TC80/C1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	72 bits			48h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			22h	28h	58h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	7			37h			
77	 Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	1			31h			
80	 Manufacturer part # (Module depth)	7			37h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	B			42h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M366S3323BT0 SDRAM DIMM

32Mx64 SDRAM DIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S3323BT0 is a 32M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S3323BT0 consists of sixteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S3323BT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S3323BT0-C80	125MHz (8ns @ CL=3)
M366S3323BT0-C1H	100MHz (10ns @ CL=2)
M366S3323BT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

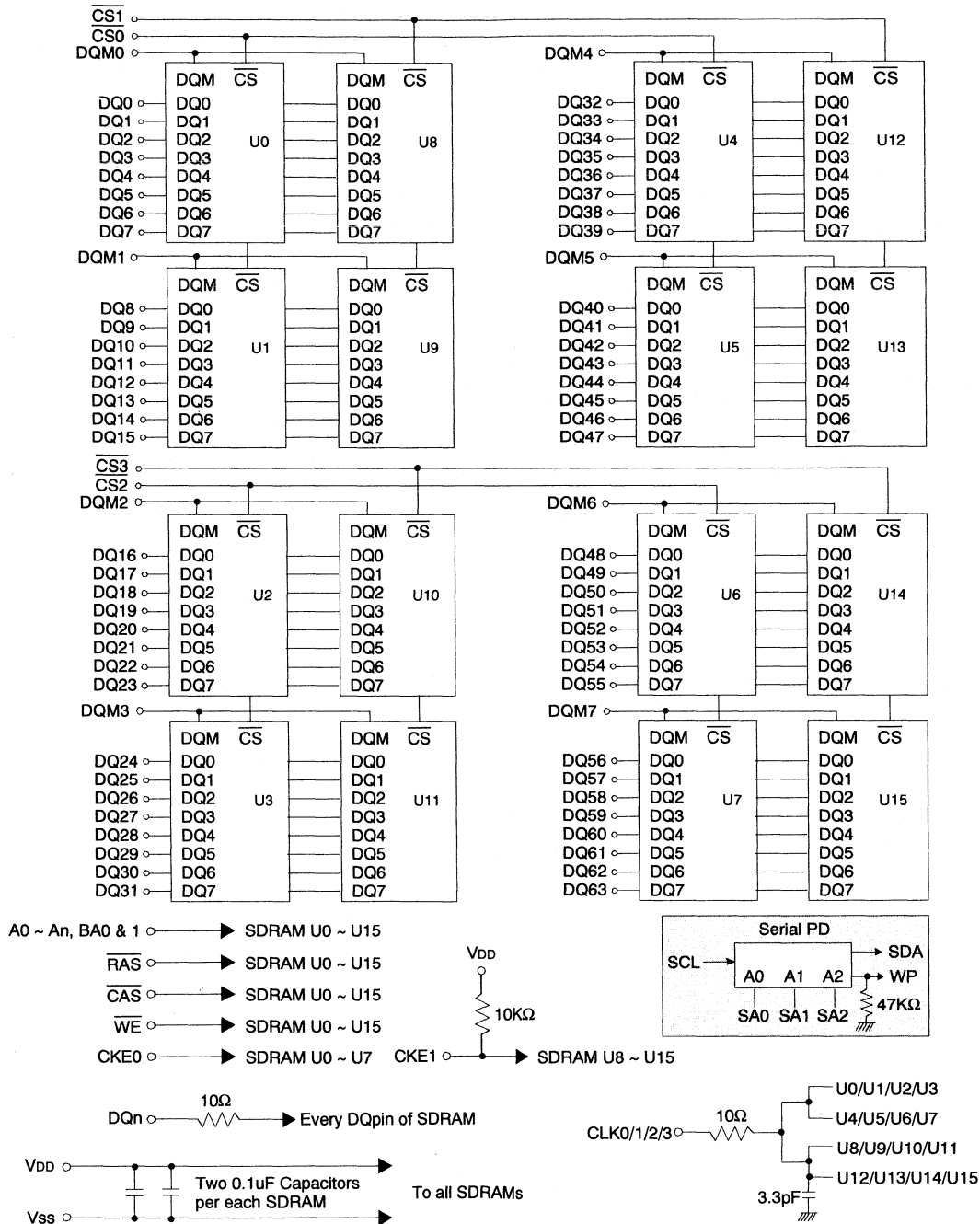
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	16	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	45	85	pF
RAS, CAS, WE	C _{IN}	45	85	pF
CKE (CKE0 ~ CKE1)	C _{CKE}	25	45	pF
Clock (CLK0 ~ CLK3)	C _{CLK}	15	21	pF
CS (CS0 ~ CS3)	C _{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	10	15	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	13	18	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,200	1,120	1,120	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	16			mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	16				
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	320			mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	112				
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	80			mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	80				
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	480			mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	320			mA	
Operating current (Burst mode)	ICC4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,440	1,240	1,240	mA	1
Refresh current	ICC5	trc ≥ trc(min)	2,000	1,920	1,920	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	24			mA	

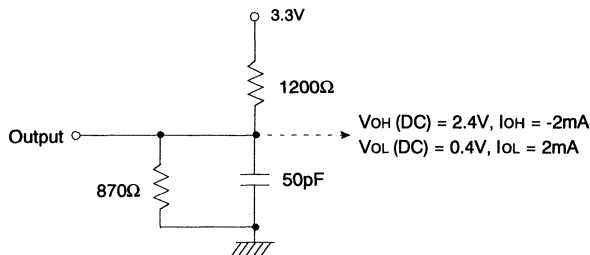
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

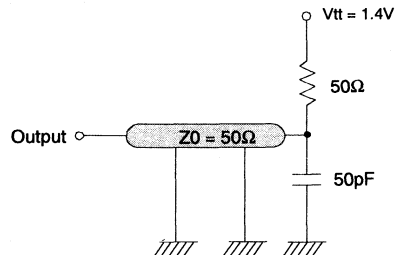
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2				ea	4
	CAS latency=2	-	1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported.

SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsac		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	toH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tss	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tshZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set		H	X	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X	3		
					H	X	X	X			3		
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

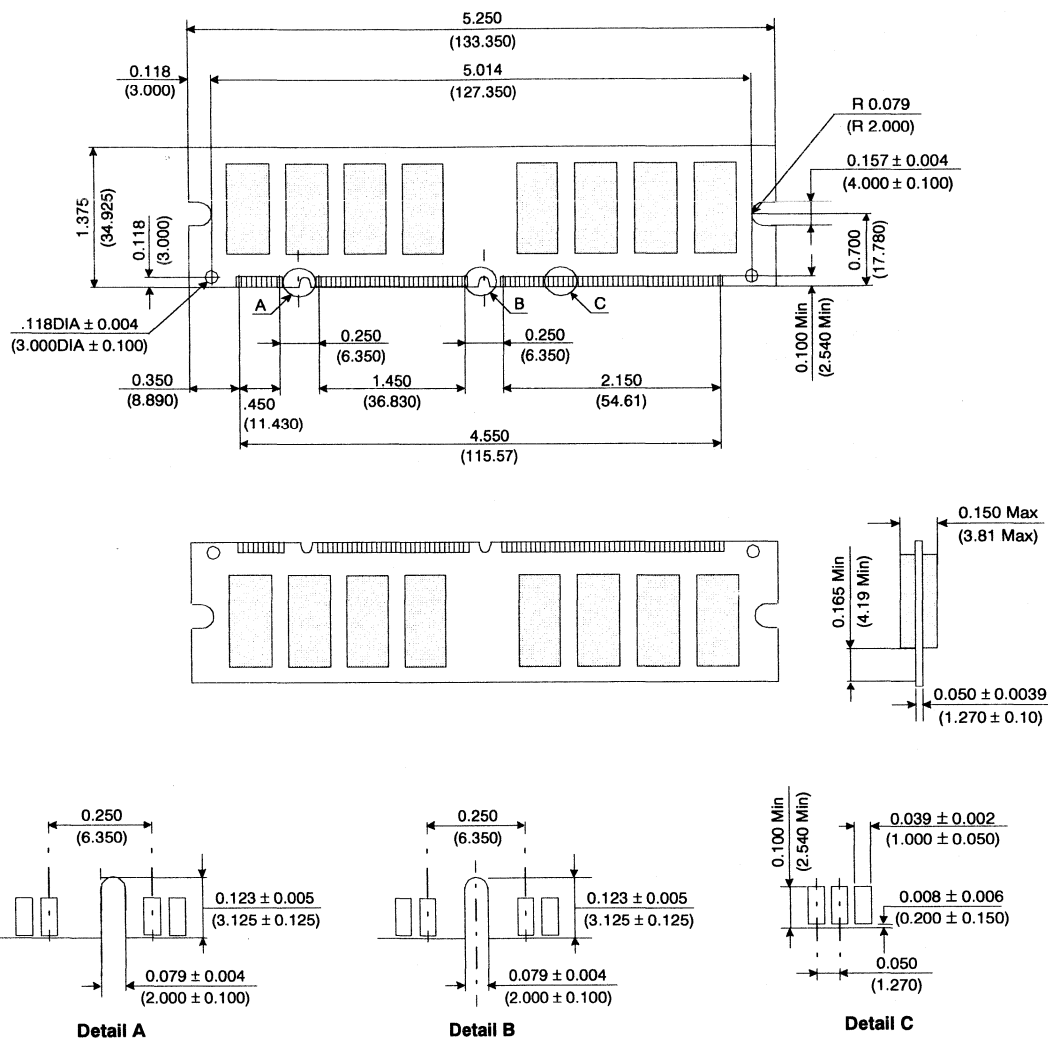
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)

Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
 SDRAM Part No. : K4S280832B

M366S3323BT0-C80/C1H/C1L

- Organization : 32Mx64
- Composition : 16Mx8 *16
- Used component part # : K4S280832B-TC80/C1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			11h	17h	47h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	3			33h			
80	 Manufacturer part # (Module depth)	3			33h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	B			42h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M374S3323BT0 SDRAM DIMM

32Mx72 SDRAM DIMM with ECC based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S3323BT0 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S3323BT0 consists of eighteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S3323BT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S3323BT0-C80	125MHz (8ns @ CL=3)
M374S3323BT0-C1H	100MHz (10ns @ CL=2)
M374S3323BT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

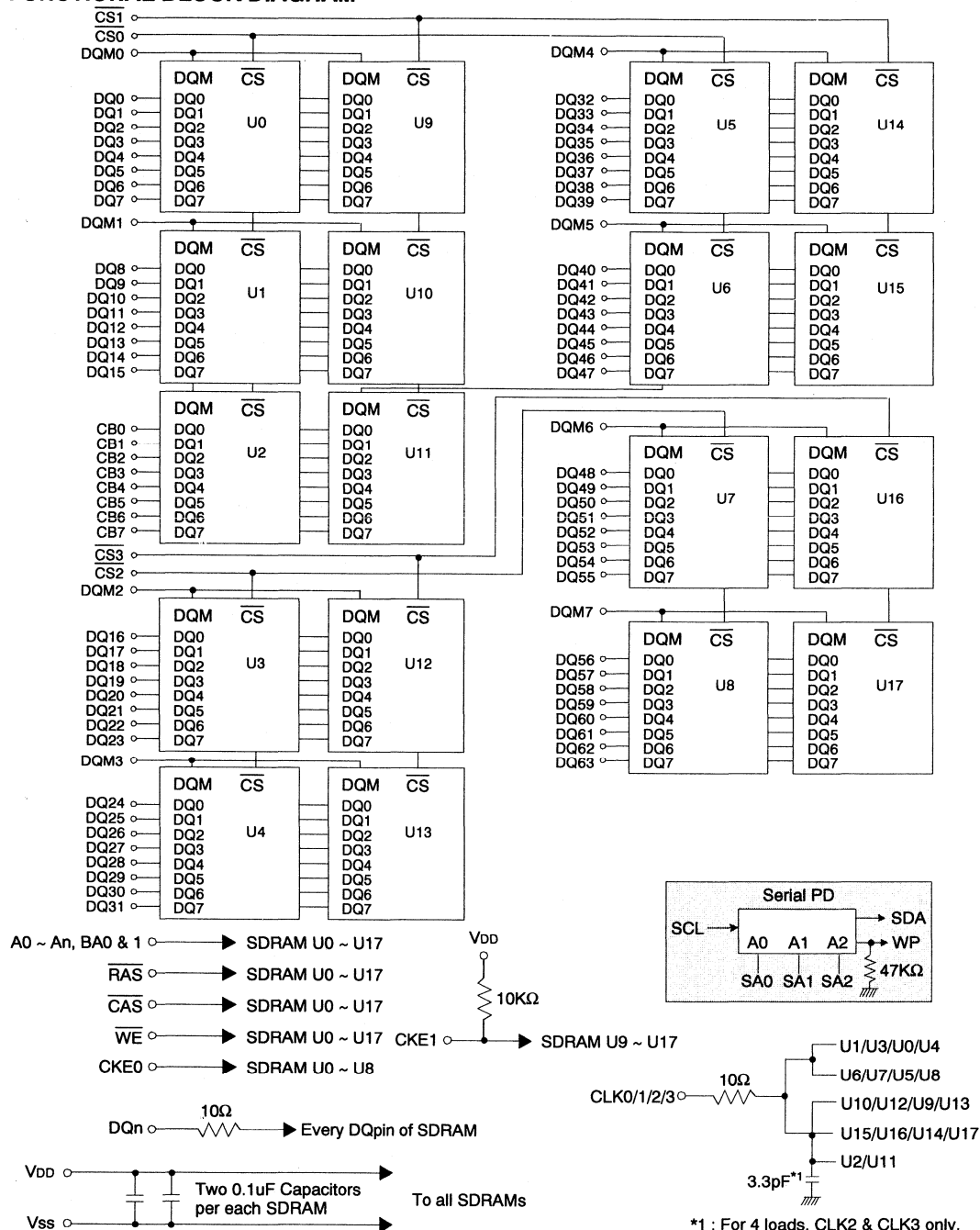
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	50	95	pF
RAS, CAS, WE	C _{IN}	50	95	pF
CKE (CKE0 ~ CKE1)	C _{CKE}	28	50	pF
Clock (CLK0 ~ CLK3)	C _{CLK}	18	25	pF
CS (CS0 ~ CS3)	C _{CS}	18	30	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	13	20	pF
DQ (DQ0 ~ DQ63)	C _{OUT1}	13	18	pF
CB (CB0 ~ CB7)	C _{OUT2}	13	18	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,350	1,260	1,260	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	18			mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	18				
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	360			mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	126				
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	90			mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	90				
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	540			mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	360			mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,575	1,395	1,395	mA	1
Refresh current	Icc5	trc ≥ trc(min)	2,250	2,160	2,160	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	27			mA	

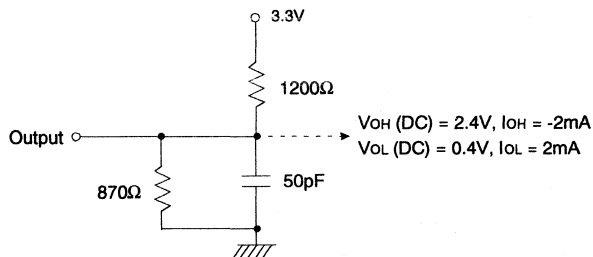
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

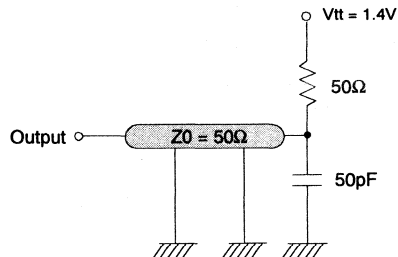
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-	1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .

SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsAC	-	6	-	6	-	6	ns	1,2
	CAS latency=2		-	-	-	6	-	7		
Output data hold time	CAS latency=3	tOH	3	-	3	-	3	-	ns	2
	CAS latency=2		-	-	3	-	3	-		
CLK high pulse width		tCH	3	-	3	-	3	-	ns	3
CLK low pulse width		tCL	3	-	3	-	3	-	ns	3
Input setup time		tSS	2	-	2	-	2	-	ns	3
Input hold time		tSH	1	-	1	-	1	-	ns	3
CLK to output in Low-Z		tSLZ	1	-	1	-	1	-	ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	6	-	6	-	6	ns	
	CAS latency=2		-	-	-	6	-	7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	H	X	X			3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

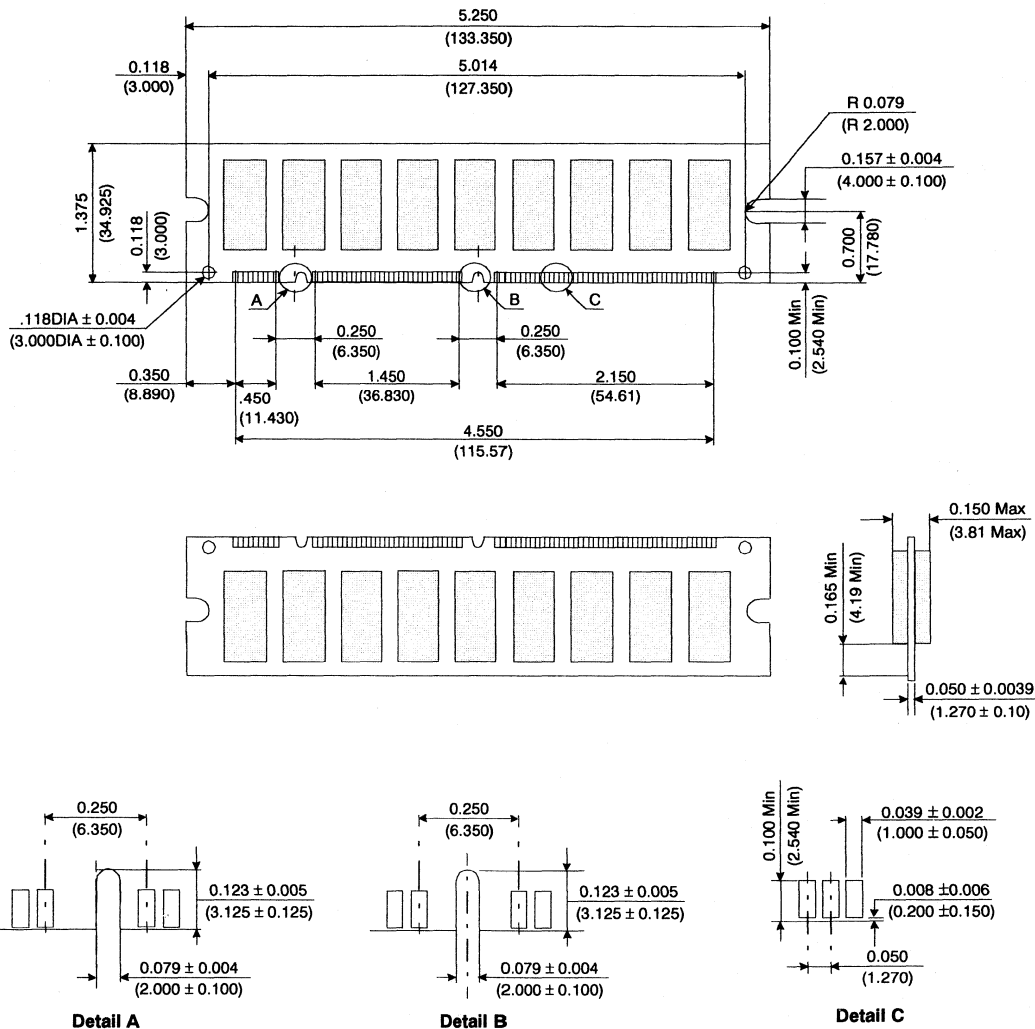
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC100 Unbuffered DIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832B

M374S3323BT0-C80/C1H/C1L

- Organization : 32Mx72
- Composition : 16Mx8 *18
- Used component part # : K4S280832B-TC80/C1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	72 bits			48h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (trRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=trCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 128MB			20h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

SERIAL PRESENCE DETECT

PC100 Unbuffered DIMM

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			23h	29h	59h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	7			37h			
77	 Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	3			33h			
80	 Manufacturer part # (Module depth)	3			33h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	B			42h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			FDh	FFh	FDh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M366S3253ATS SDRAM DIMM

32Mx64 SDRAM DIMM based on 32Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S3253ATS is a 32M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S3253ATS consists of eight CMOS 32M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M366S3253ATS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S3253ATS-C80	125MHz (8ns @ CL=3)
M366S3253ATS-C1H	100MHz (10ns @ CL=2)
M366S3253ATS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

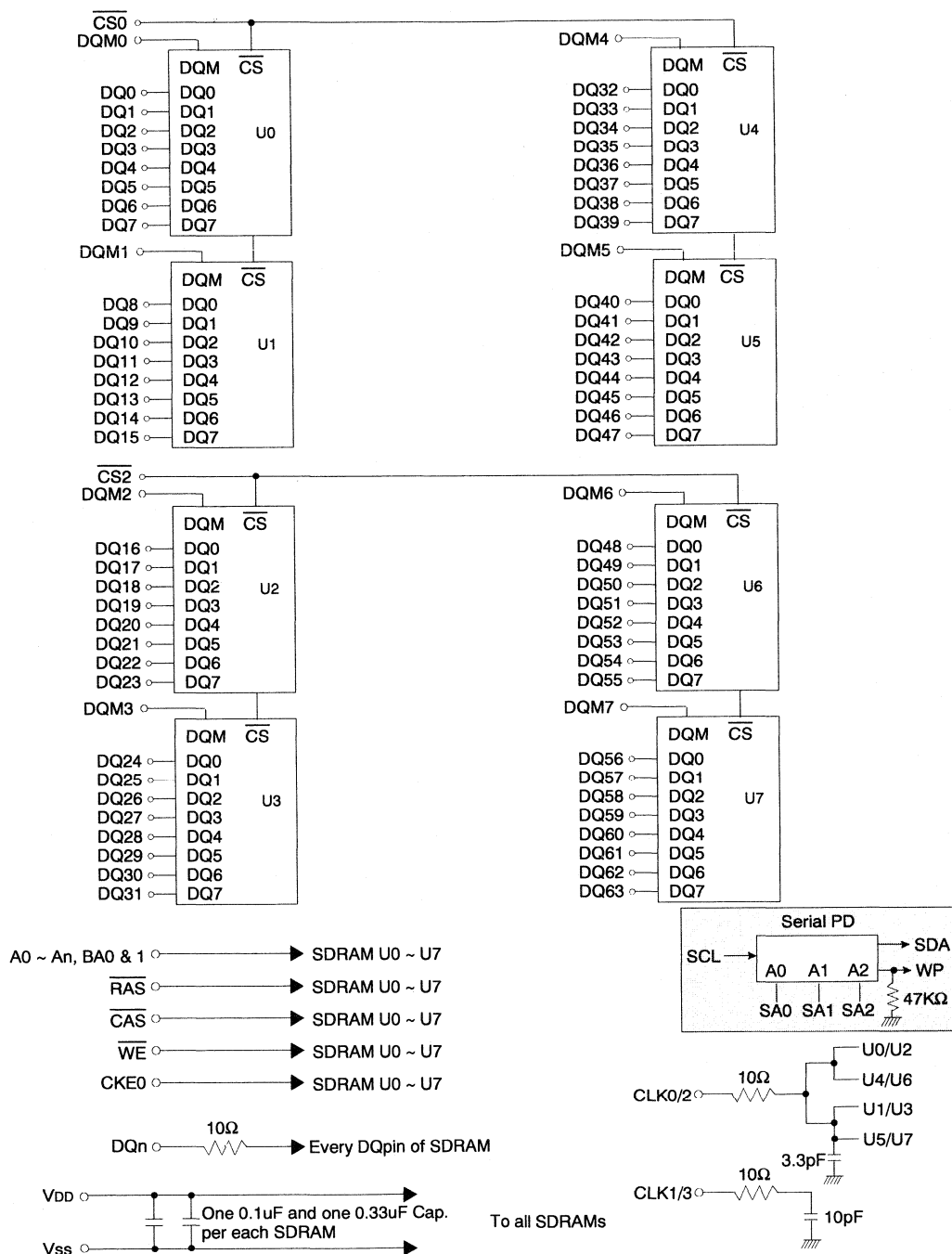
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	C _{ADD}	25	45	pF
RAS, CAS, WE	C _{IN}	25	45	pF
CKE (CKE0)	C _{CKE}	25	45	pF
Clock (CLK0, CLK2)	C _{CLK}	15	21	pF
CS (CS0, CS2)	C _{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	8	12	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	960	880	880	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	16			mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	16				
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	128			mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	112				
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	48			mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	48				
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	240			mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	200			mA	
Operating current (Burst mode)	ICC4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,120	920	920	mA	1
Refresh current	ICC5	trc ≥ trc(min)	1,680	1,600	1,600	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	40			mA	

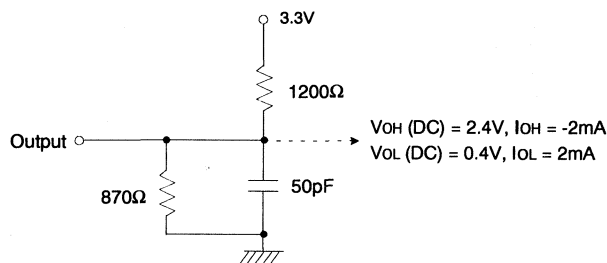
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

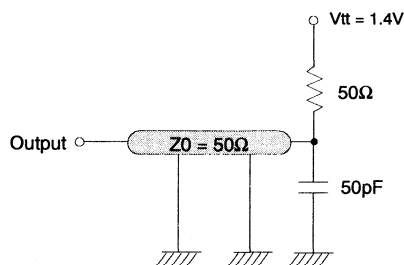
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4	
	CAS latency=2	-	1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK+20ns$ is also supported .

SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + 20ns$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	toH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1$ ns.
If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A12, A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L	L	L	L	H	X	X		3	
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Units : Inches (Millimeters)



717

M366S3253ATS-C80/C1H/C1L

- Organization : 32Mx64
- Composition : 32Mx8 * 8
- Used component part # : K4S560832A-TC80/C1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 8K / 64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	7.8us, support self refresh			82h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 256MB			40h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			33h	39h	69h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	3			33h			
80	 Manufacturer part # (Module depth)	2			32h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	5			35h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	A			41h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S (4 Layer PCB)			53h			
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

Note : 1. The bank select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsung's own purpose.

M374S3253ATS SDRAM DIMM

32Mx72 SDRAM DIMM with ECC based on 32Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S3253ATS is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S3253ATS consists of nine CMOS 32M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. One 0.1uF and one 0.33uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M374S3253ATS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S3253ATS-C80	125MHz (8ns @ CL=3)
M374S3253ATS-C1H	100MHz (10ns @ CL=2)
M374S3253ATS-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	*SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	*SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

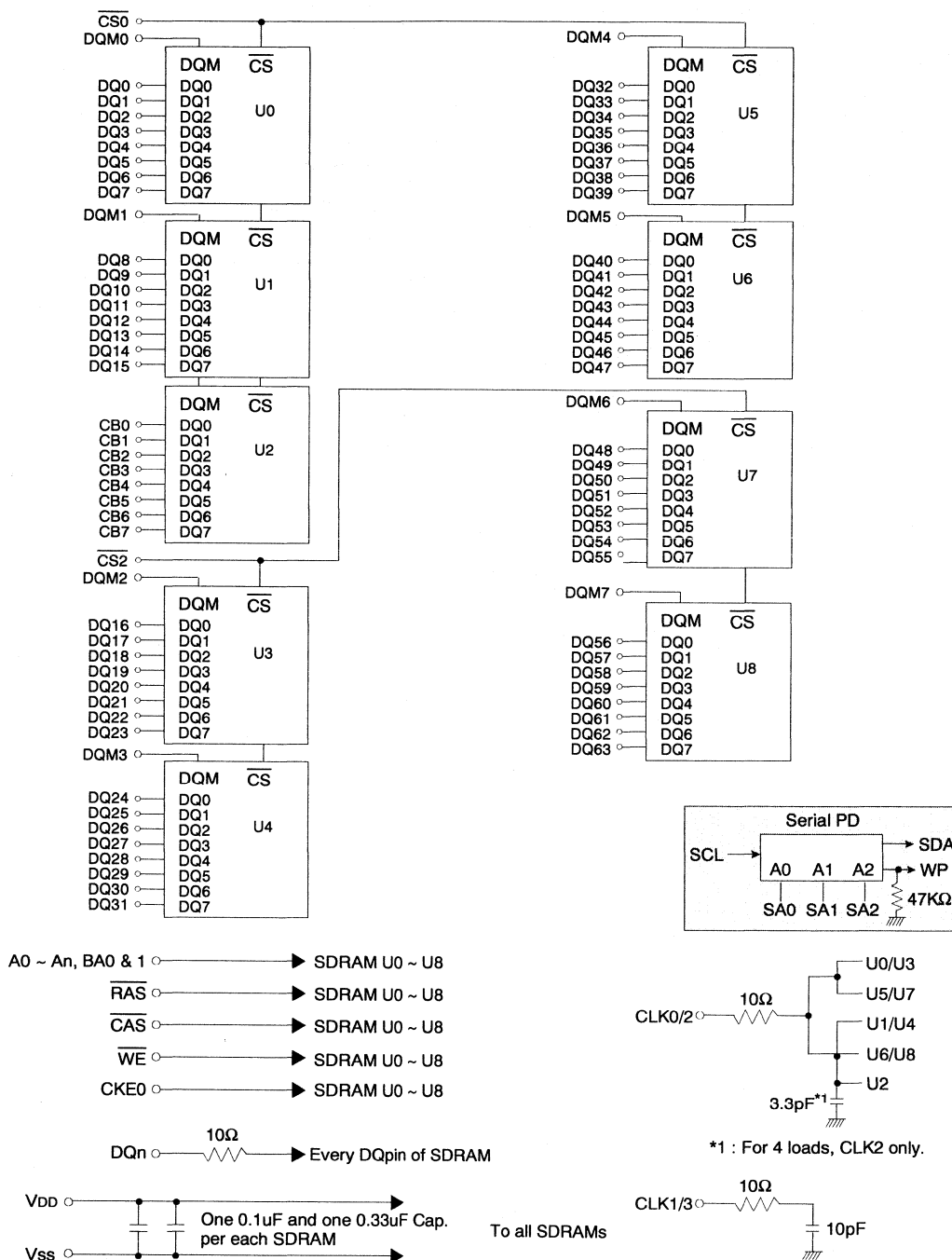
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Check bit	Check bits for ECC.
WP	Write protection	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _d	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	C _{ADD}	28	50	pF
<u>RAS</u> , <u>CAS</u> , <u>WE</u>	C _{IN}	28	50	pF
CKE (CKE0)	C _{CKE}	28	50	pF
Clock (CLK0, CLK2)	C _{CLK}	18	25	pF
CS (CS0, CS2)	C _{CS}	18	30	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	8	10	pF
DQ (DQ0 ~ DQ63)	C _{OUT1}	9	12	pF
CB (CB0 ~ CB7)	C _{OUT2}	9	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC(min)}$ $I_O = 0$ mA	1,080	990	990	mA	1
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL(max)}$, $t_{CC} = 10ns$	18			mA	
	ICC2PS	$CKE \ \& \ CLK \leq V_{IL(max)}$, $t_{CC} = \infty$	18				
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH(min)}$, $\overline{CS} \geq V_{IH(min)}$, $t_{CC} = 10ns$ Input signals are changed one time during 20ns	144			mA	
	ICC2NS	$CKE \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$, $t_{CC} = \infty$ Input signals are stable	126				
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL(max)}$, $t_{CC} = 10ns$	54			mA	
	ICC3PS	$CKE \ \& \ CLK \leq V_{IL(max)}$, $t_{CC} = \infty$	54				
Active standby current in non power-down mode (One bank active)	ICC3N	$CKE \geq V_{IH(min)}$, $\overline{CS} \geq V_{IH(min)}$, $t_{CC} = 10ns$ Input signals are changed one time during 20ns	270			mA	
	ICC3NS	$CKE \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$, $t_{CC} = \infty$ Input signals are stable	225			mA	
Operating current (Burst mode)	ICC4	$I_O = 0$ mA Page burst 4Banks activated $t_{CCD} = 2CLKs$	1,260	1,035	1,035	mA	1
Refresh current	ICC5	$t_{RC} \geq t_{RC(min)}$	1,890	1,800	1,800	mA	2
Self refresh current	ICC6	$CKE \leq 0.2V$	45			mA	

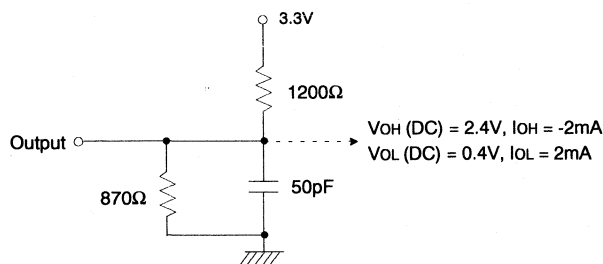
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

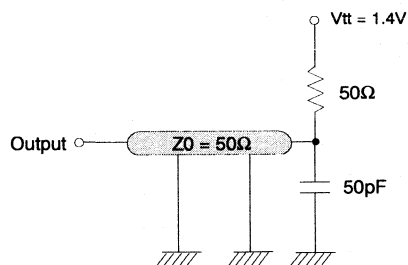
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4	
	CAS latency=2	-	1				

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -80/1H/1L, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .
SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsac		6		6		6	ns	1, 2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	toH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A12, A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

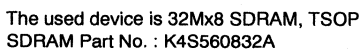
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC100 Unbuffered DIMM

Units : Inches (Millimeters)



M374S3253ATS-C80/C1H/C1L

- Organization : 32Mx72
- Composition : 32Mx8 *9
- Used component part # : K4S560832A-TC80/C1H/C1L
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 8K / 64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	1 Row			01h			
6	Data width of this assembly	72 bits			48h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	7.8 us, support self refresh			82h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	1 Row of 256MB			40h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

SERIAL PRESENCE DETECT

PC100 Unbuffered DIMM

Byte #	Function Described	Function Supported			Hex value			Note
		-B0	-1H	-1L	-B0	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			45h	4Bh	7Bh	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	7			37h			
77	 Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	3			33h			
80	 Manufacturer part # (Module depth)	2			32h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	5			35h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	A			41h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	S			53h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	S			53h			
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

M366S6453AT0 SDRAM DIMM

64Mx64 SDRAM DIMM based on 32Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S6453AT0 is a 64M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S6453AT0 consists of sixteen CMOS 32M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S6453AT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S6453AT0-C80	125MHz (8ns @ CL=3)
M366S6453AT0-C1H	100MHz (10ns @ CL=2)
M366S6453AT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50		
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51		
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD		
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52		
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC		
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF		
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC		
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss		
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53		
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54		
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55		
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss		
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56		
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57		
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58		
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59		
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD		
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60		
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61		
20	DQ15	48	DU	76	DQ30	104	DQ47	132	A13	160	DQ62		
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63		
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss		
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3		
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC		
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0		
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1		
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2		
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD		

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

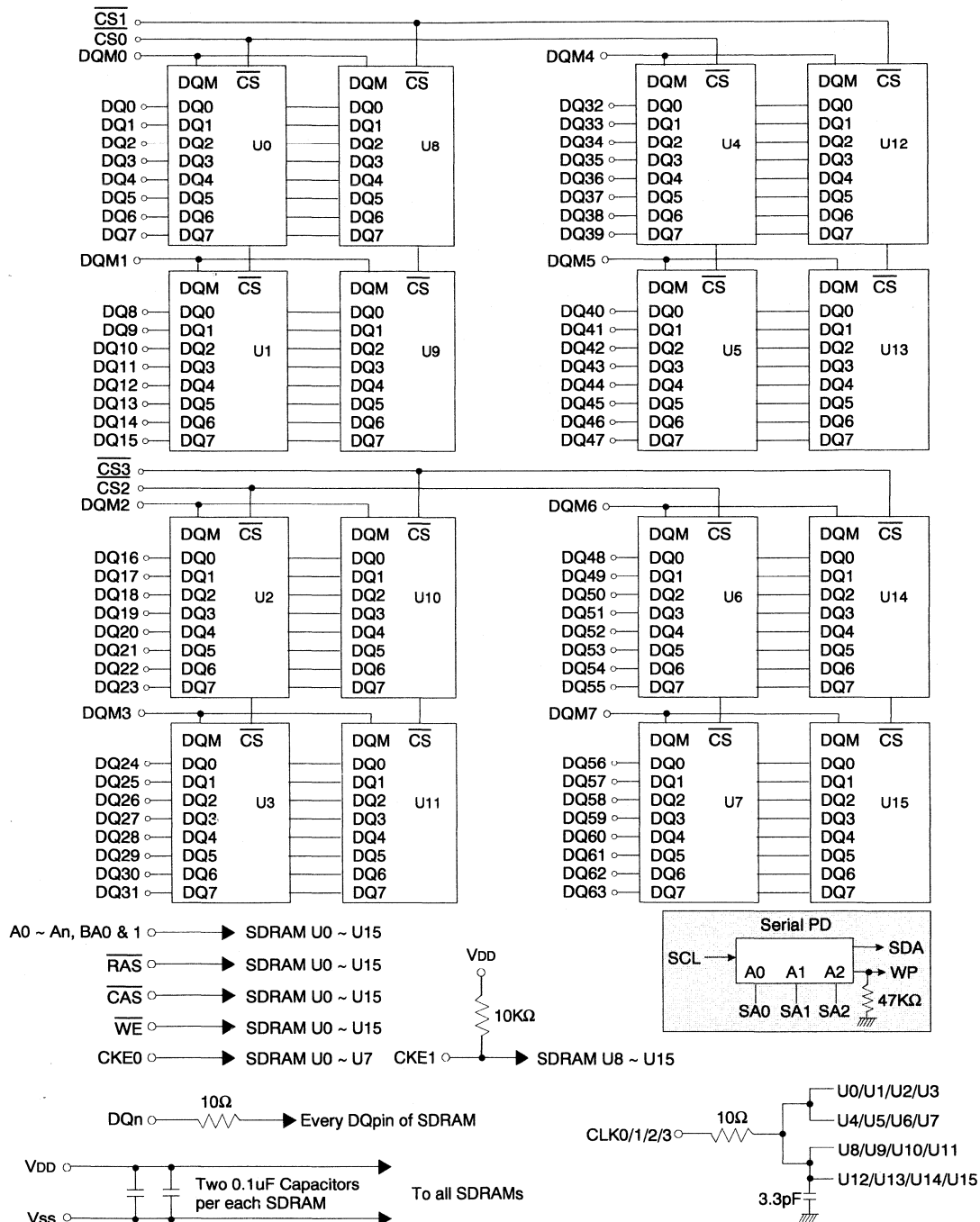
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
WE	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	Pd	16	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	CADD	45	85	pF
RAS, CAS, WE	CIN	45	85	pF
CKE (CKE0 ~ CKE1)	CCKE	25	45	pF
Clock (CLK0 ~ CLK3)	CCLK	15	21	pF
CS (CS0 ~ CS3)	Ccs	15	25	pF
DQM (DQM0 ~ DQM7)	CDQM	10	15	pF
DQ (DQ0 ~ DQ63)	COUT	13	18	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,200	1,120	1,120	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	32			mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	32				
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	256			mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	224				
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	96			mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	96				
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	480			mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	400			mA	
Operating current (Burst mode)	ICC4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,360	1,160	1,160	mA	1
Refresh current	ICC5	trc ≥ trc(min)	1,920	1,840	1,840	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	80			mA	

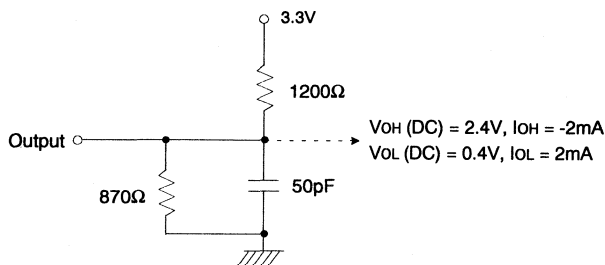
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

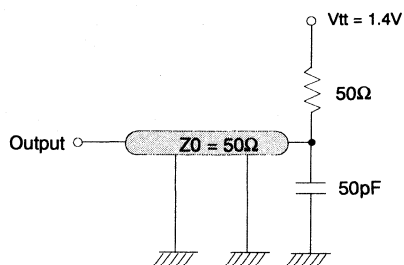
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version			Unit	Note
		-80	-1H	-1L		
Row active to row active delay	tRRD(min)	16	20	20	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	tRCD(min)	20	20	20	ns	1
Row precharge time	tRP(min)	20	20	20	ns	1
Row active time	tRAS(min)	48	50	50	ns	1
	tRAS(max)	100			us	
Row cycle time	tRC(min)	68	70	70	ns	1
Last data in to row precharge	tRDL(min)	2			CLK	2,5
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay	tCDL(min)	1			CLK	2
Last data in to burst stop	tBDL(min)	1			CLK	2
Col. address to col. address delay	tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4
	CAS latency=2	-	1			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. For -80/1H/1L, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK}+20\text{ns}$ is also supported .

SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + 20\text{ns}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tsAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tsLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A12, A11 A9 ~ A0	Note	
Register	Mode register set		H	X	L	L	L	L	X	OP code		1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	L		3									
		Exit	L	H	L	H	H	X	X		3		
											H	X	X
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Burst stop			H	X	L	H	H	L	X	X		6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

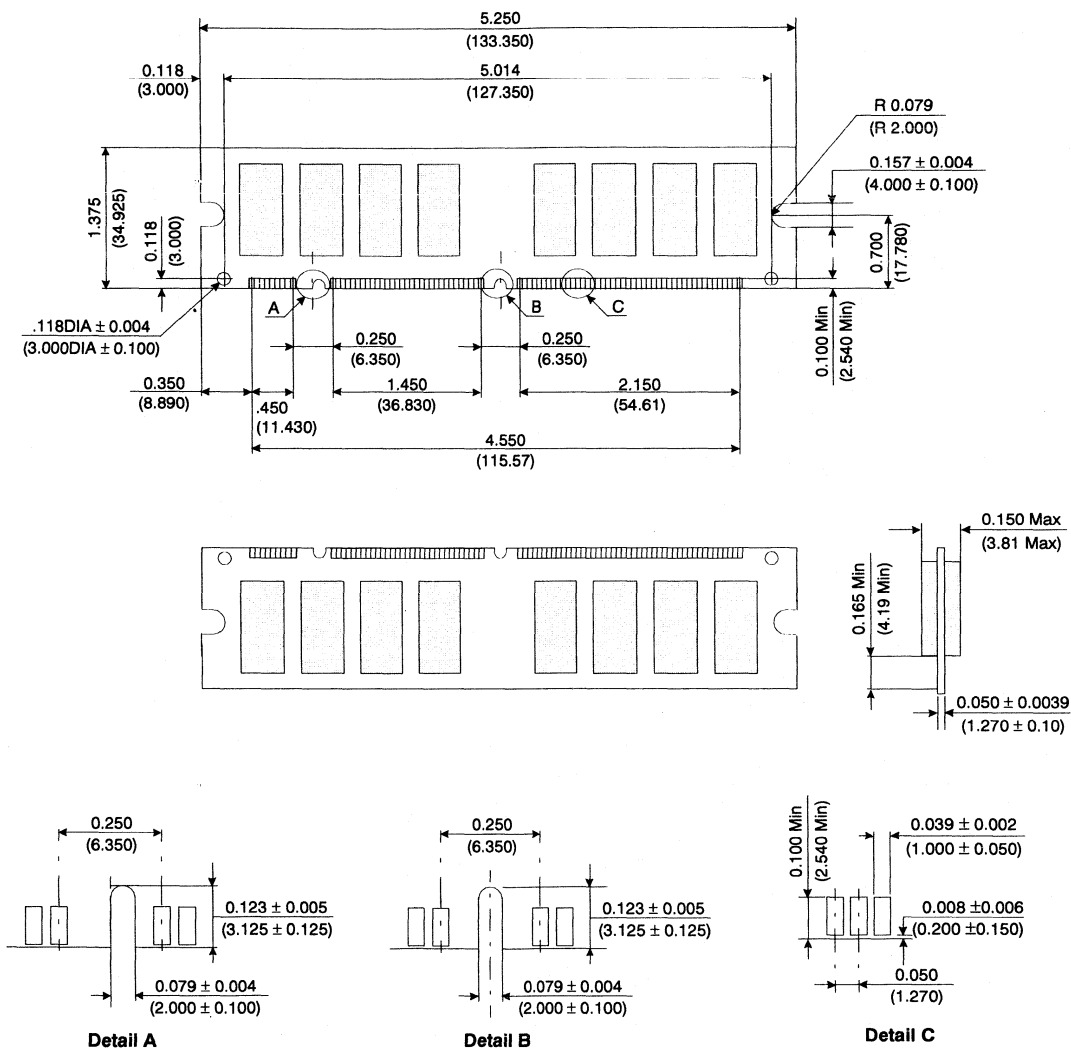
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± .005(.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
 SDRAM Part No. :K4S560832A

M366S6453AT0-C80/C1H/C1L

- Organization : 64Mx64
- Composition : 32Mx8 *16
- Used component part # : K4S560832A-TC80/C1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 8K / 64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	64 bits			40h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuration type	Non parity			00h			
12	Refresh rate & type	7.8us, support self refresh			82h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock@CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock@CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 256MB			40h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			34h	3Ah	6Ah	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	6			36h			
77	 Manufacturer part # (Data bits)	6			36h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	6			36h			
80	 Manufacturer part # (Module depth)	4			34h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	5			35h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	A			41h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M374S6453AT0 SDRAM DIMM

64Mx72 SDRAM DIMM with ECC based on 32Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S6453AT0 is a 64M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S6453AT0 consists of eighteen CMOS 32M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S6453AT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S6453AT0-C80	125MHz (8ns @ CL=3)
M374S6453AT0-C1H	100MHz (10ns @ CL=2)
M374S6453AT0-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

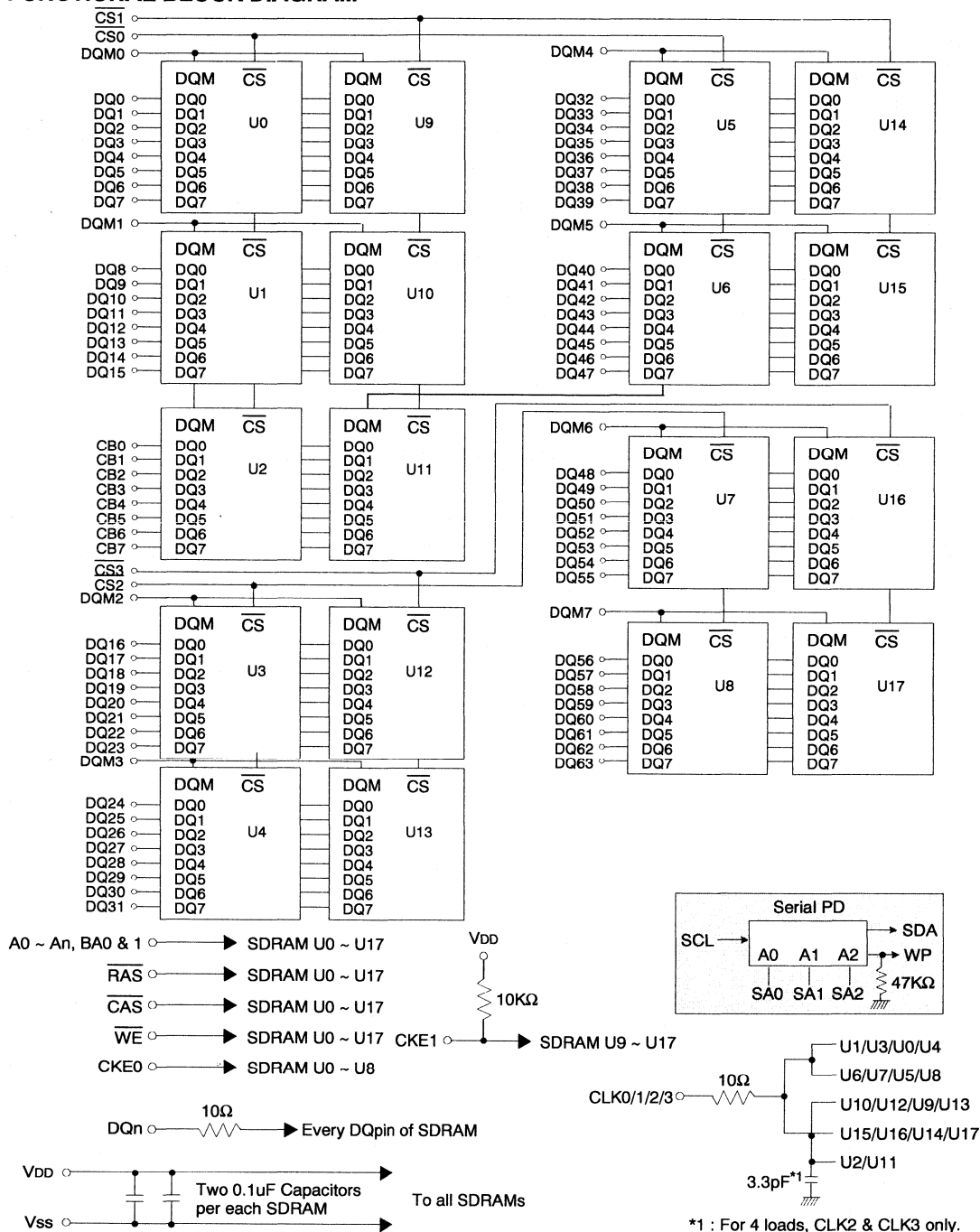
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	PD	18	W
Short circuit current	IOS	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	VIH	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	VIL	-0.3	0	0.8	V	2
Output logic high voltage	VOH	2.4	-	-	V	IOH = -2mA
Output logic low voltage	VOL	-	-	0.4	V	IoL = 2mA
Input leakage current	ILI	-10	-	10	uA	3

Notes : 1. VIH (max) = 5.6V AC. The overshoot voltage duration is $\leq 3\text{ns}$.

2. VIL (min) = -2.0V AC. The undershoot voltage duration is $\leq 3\text{ns}$.

3. Any input $0\text{V} \leq \text{VIN} \leq \text{VDDQ}$.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V $\pm$ 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	CADD	50	95	pF
RAS, CAS, WE	CIN	50	95	pF
CKE (CKE0 ~ CKE1)	CCKE	28	50	pF
Clock (CLK0 ~ CLK3)	CCLK	18	25	pF
CS (CS0 ~ CS3)	CCS	18	30	pF
DQM (DQM0 ~ DQM7)	CDQM	13	20	pF
DQ (DQ0 ~ DQ63)	COUT1	13	18	pF
CB (CB0 ~ CB7)	COUT2	13	18	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-80	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1,350	1,260	1,260	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	36			mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	36				
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	288			mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	252				
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	108			mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	108				
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	540			mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	450			mA	
Operating current (Burst mode)	ICC4	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,530	1,305	1,305	mA	1
Refresh current	ICC5	trc ≥ trc(min)	2,160	2,070	2,070	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	90			mA	

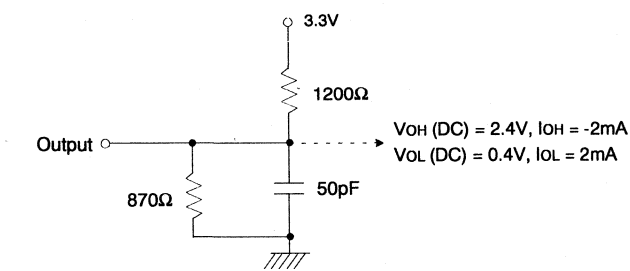
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

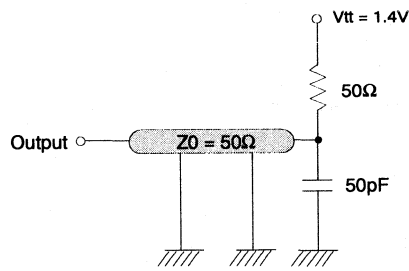
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		tRRD(min)	16	20	20	ns	1
RAS to CAS delay		tRCD(min)	20	20	20	ns	1
Row precharge time		tRP(min)	20	20	20	ns	1
Row active time		tRAS(min)	48	50	50	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	68	70	70	ns	1
Last data in to row precharge		tRDL(min)	2			CLK	2.5
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4	
	CAS latency=2	-	1				

- Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -80/1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
- SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + 20ns.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tSAC		6		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	3		3		3		ns	3
CLK low pulse width		tCL	3		3		3		ns	3
Input setup time		tSS	2		2		2		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		6	ns	
	CAS latency=2			-		6		7		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A12,A11 A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

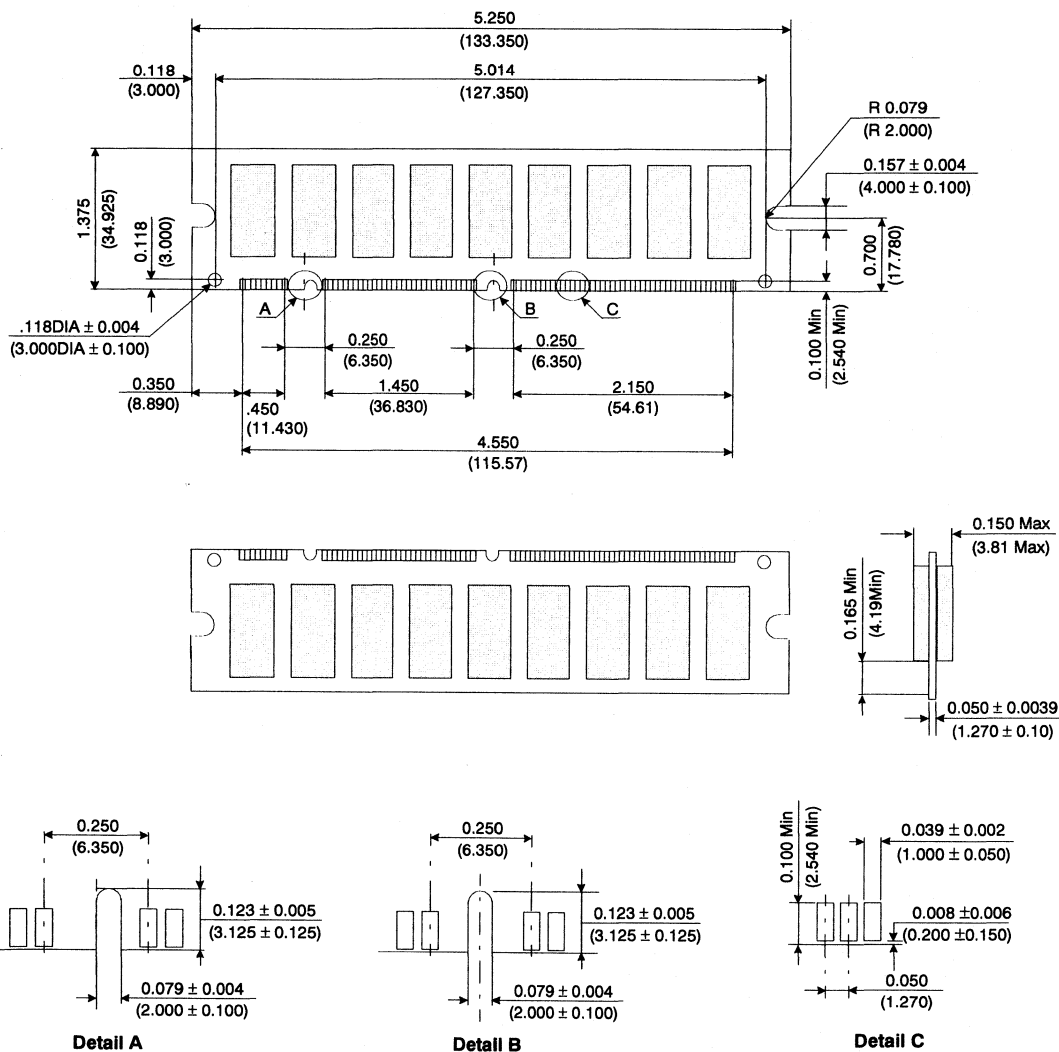
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
 SDRAM Part No. : K4S560832A

M374S6453AT0-C80/C1H/C1L

- Organization : 64Mx72
- Composition : 32Mx8 *18
- Used component part # : K4S560832A-TC80/C1H/C1L
- # of rows in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 8K / 64ms
- Contents ;

Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	10			0Ah			1
5	# of module Rows on this assembly	2 Rows			02h			
6	Data width of this assembly	72 bits			48h			
7	 Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	6ns	60h	60h	60h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	7.8us, support self refresh			82h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	10ns	12ns	C0h	A0h	C0h	2
24	SDRAM access time from clock @CAS latency of 2	6ns	6ns	7ns	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	20ns	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	50ns	30h	32h	32h	
31	Module Row density	2 Rows of 256MB			40h			
32	Command and address signal input setup time	2ns	2ns	2ns	20h	20h	20h	
33	Command and address signal input hold time	1ns	1ns	1ns	10h	10h	10h	
34	Data signal input setup time	2ns	2ns	2ns	20h	20h	20h	

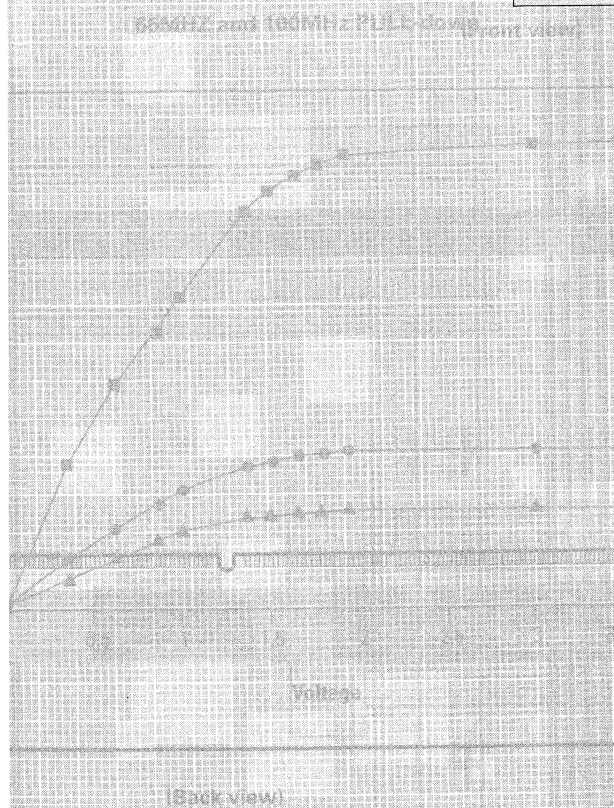
Byte #	Function Described	Function Supported			Hex value			Note
		-80	-1H	-1L	-80	-1H	-1L	
35	Data signal input hold time	1ns	1ns	1ns	10h	10h	10h	
36~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	PC100 SPD Spec. Ver. 1.2A			12h			
63	Checksum for bytes 0 ~ 62	-			46h	4Ch	7Ch	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	 Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	3			33h			
75	Manufacturer part # (Data bits)	Blank			20h			
76	 Manufacturer part # (Data bits)	7			37h			
77	 Manufacturer part # (Data bits)	4			34h			
78	Manufacturer part # (Mode & operating voltage)	S			53h			
79	Manufacturer part # (Module depth)	6			36h			
80	 Manufacturer part # (Module depth)	4			34h			
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	5			35h			
82	Manufacturer part # (Composition component)	3			33h			
83	Manufacturer part # (Component revision)	A			41h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB revision & type)	0			30h			
86	Manufacturer part # (Hyphen)	" - "			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	8	1	1	38h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	0	H	L	30h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank			20h			
91	Manufacturer revision code (For PCB)	0			30h			
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~125	Manufacturer specific data (may be used in future)	Undefined			-			5
126	System frequency for 100MHz	100MHz			64h			
127	PC100 specification details	Detailed 100MHz Information			ADh	AFh	ADh	
128+	Unused storage locations	Undefined			-			5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung 's own purpose.

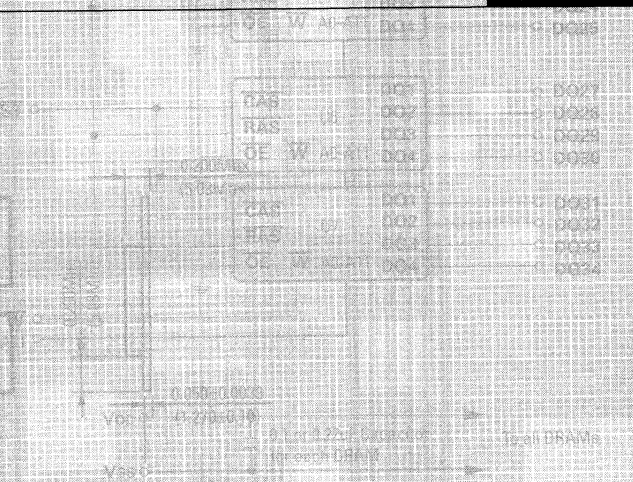


Module Specification

3



PC133 SODIMM



M464S0924BT1 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M464S0924BT1 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S0924BT1 consists of four CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S0924BT1 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M464S0924BT1-L75 /C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,000mil) , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38					111	A10/AP	112	A11
19	DQ7	20	DQ39	61	CLK0	62	CKE0	113	VDD	114	VDD
21	Vss	22	Vss	63	VDD	64	VDD	115	DQM2	116	DQM6
23	DQM0	24	DQM4	65	RAS	66	CAS	117	DQM3	118	DQM7
25	DQM1	26	DQM5	67	WE	68	*CKE1	119	Vss	120	Vss
27	VDD	28	VDD	69	CS0	70	*A12	121	DQ24	122	DQ56
29	A0	30	A3	71	*CS1	72	*A13	123	DQ25	124	DQ57
31	A1	32	A4	73	DU	74	*CLK1	125	DQ26	126	DQ58
33	A2	34	A5	75	Vss	76	Vss	127	DQ27	128	DQ59
35	Vss	36	Vss	77	NC	78	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	79	NC	80	NC	131	DQ28	132	DQ60
39	DQ9	40	DQ41	81	VDD	82	VDD	133	DQ29	134	DQ61
41	DQ10	42	DQ42	83	DQ16	84	DQ48	135	DQ30	136	DQ62
43	DQ11	44	DQ43	85	DQ17	86	DQ49	137	DQ31	138	DQ63
45	VDD	46	VDD	87	DQ18	88	DQ50	139	Vss	140	Vss
47	DQ12	48	DQ44	89	DQ19	90	DQ51	141	**SDA	142	**SCL
49	DQ13	50	DQ45	91	Vss	92	Vss	143	VDD	144	VDD
				93	DQ20	94	DQ52				

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address storable
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

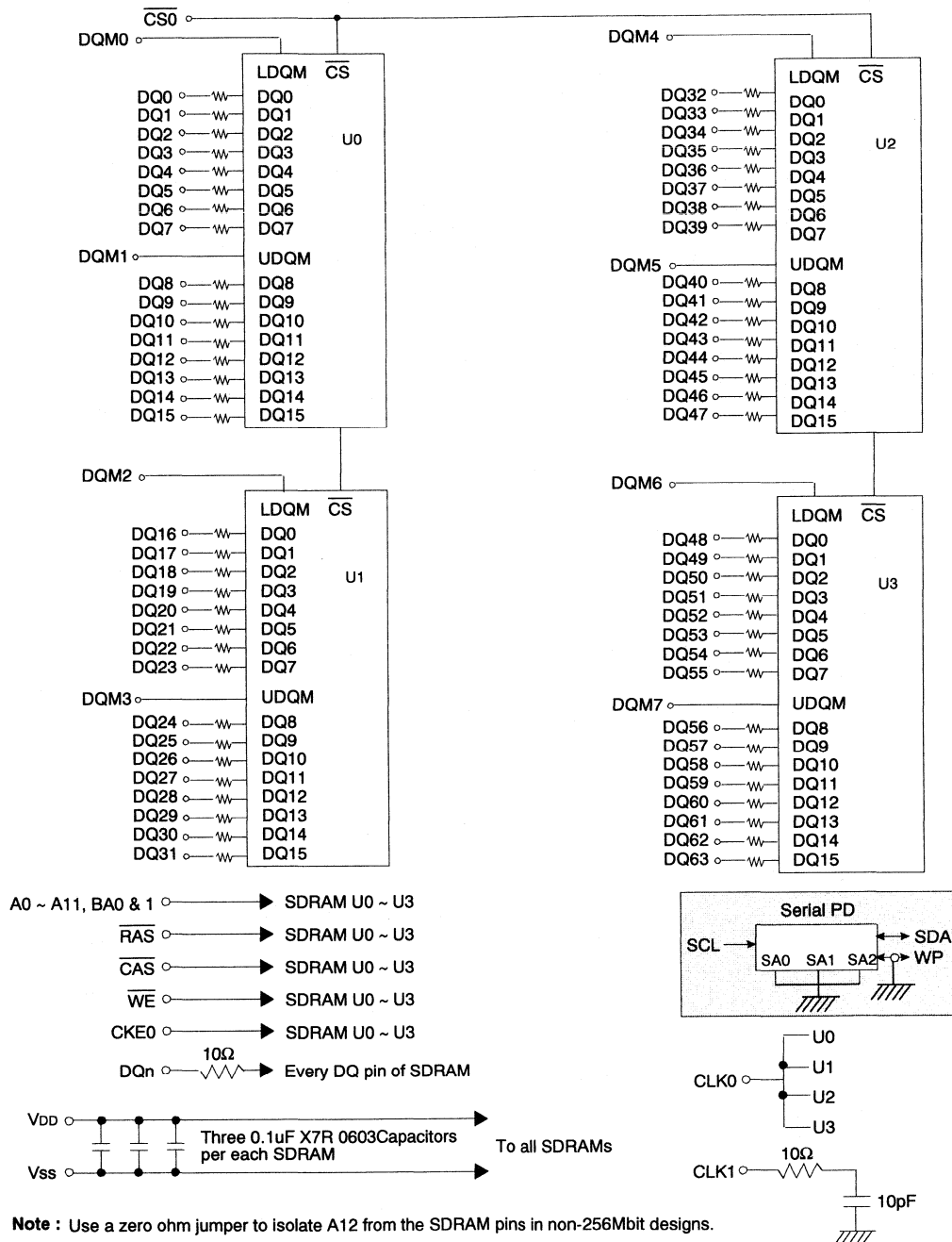
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	4	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	15	25	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	15	25	pF
Input capacitance (CKE ₀)	C _{IN3}	15	25	pF
Input capacitance (CLK ₀)	C _{IN4}	15	21	pF
Input capacitance (CS ₀)	C _{IN5}	15	25	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	10	12	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	10	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	I _{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}(\text{min})$ $I_O = 0 \text{ mA}$	600	mA	1
Precharge standby current in power-down mode	I _{CC2P}	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	4	mA	
	I _{CC2PS}	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	4		
Precharge standby current in non power-down mode	I _{CC2N}	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	80	mA	
	I _{CC2NS}	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	28		
Active standby current in power-down mode	I _{CC3P}	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	20	mA	
	I _{CC3PS}	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	20		
Active standby current in non power-down mode (One bank active)	I _{CC3N}	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	120	mA	
	I _{CC3NS}	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	80	mA	
Operating current (Burst mode)	I _{CC4}	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	720	mA	1
Refresh current	I _{CC5}	$t_{RC} \geq t_{RC}(\text{min})$	880	mA	2
Self refresh current	I _{CC6}	$\text{CKE} \leq 0.2\text{V}$	C	9	mA
			L	3.2	mA

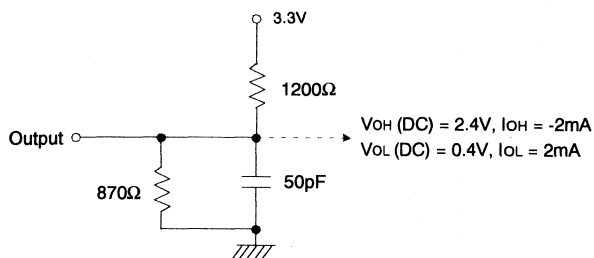
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

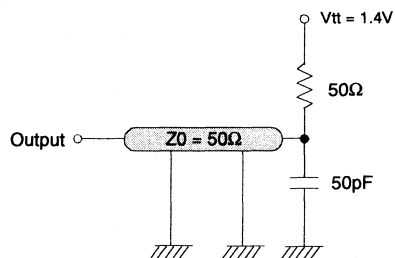
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\min)$	15	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	ns	1
Row active time	$t_{RAS}(\min)$	45	ns	1
	$t_{RAS}(\max)$	100	us	
Row cycle time	$t_{RC}(\min)$	65	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20 ns	-	
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
	CAS latency=2		-			
CLK to valid output delay	CAS latency=3	tSAC		5.4	ns	1,2
	CAS latency=2			-		
Output data hold time	CAS latency=3	tOH	2.7		ns	2
	CAS latency=2		-			
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	
	CAS latency=2			-		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	L		3									
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

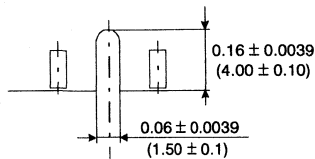
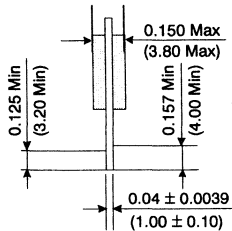
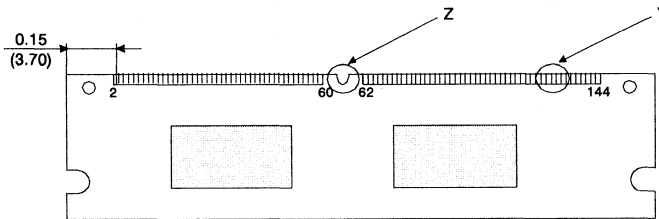
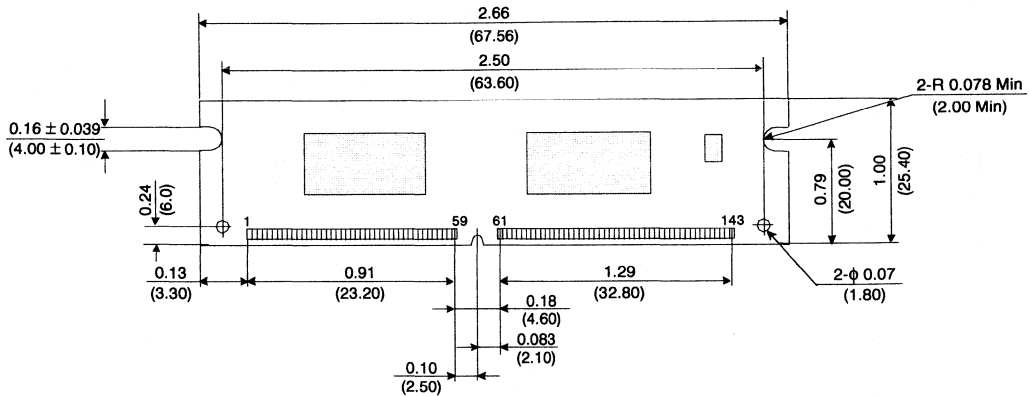
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

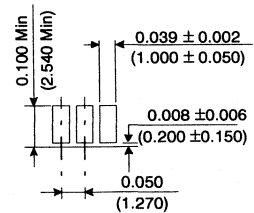
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ± 0.006(.15) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
SDRAM Part No. : K4S281632B

SERIAL PRESENCE DETECT

PC133 SODIMM

M464S0924BT1-L75/C75

- Organization : 8Mx64
- Composition : 8Mx16 *4
- Used component part # : K4S281632B-TL75/TC75
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,000 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 64MB	10h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-75		-75		
35	Data signal input hold time	0.8ns		08h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	JEDEC 2		02h		
63	Checksum for bytes 0 ~ 62	-		94h		
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM Configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	6		36h		
77	 Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	0		30h		
80	 Manufacturer part # (Module depth)	9		39h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	B		42h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	1		31h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	L	C	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7		37h		
89	Manufacturer part # (Minimum cycle time)	5		35h		
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	1		31h		
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)		42h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~12	Manufacturer specific data (may be used in future)	Undefined		-		5
126	Reserved	-		64h		6
127	Reserved	Detailed PC100 Information		8Dh		6
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.
 6. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S1724BT1 SDRAM SODIMM

16Mx64 SDRAM SODIMM based on 8Mx16,4Banks,4K Refresh,3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M464S1724BT1 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S1724BT1 consists of eight CMOS 8M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S1724BT1 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M464S1724BT1-L75/C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,250mil) , double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS1	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

* These pins are not used in this module.

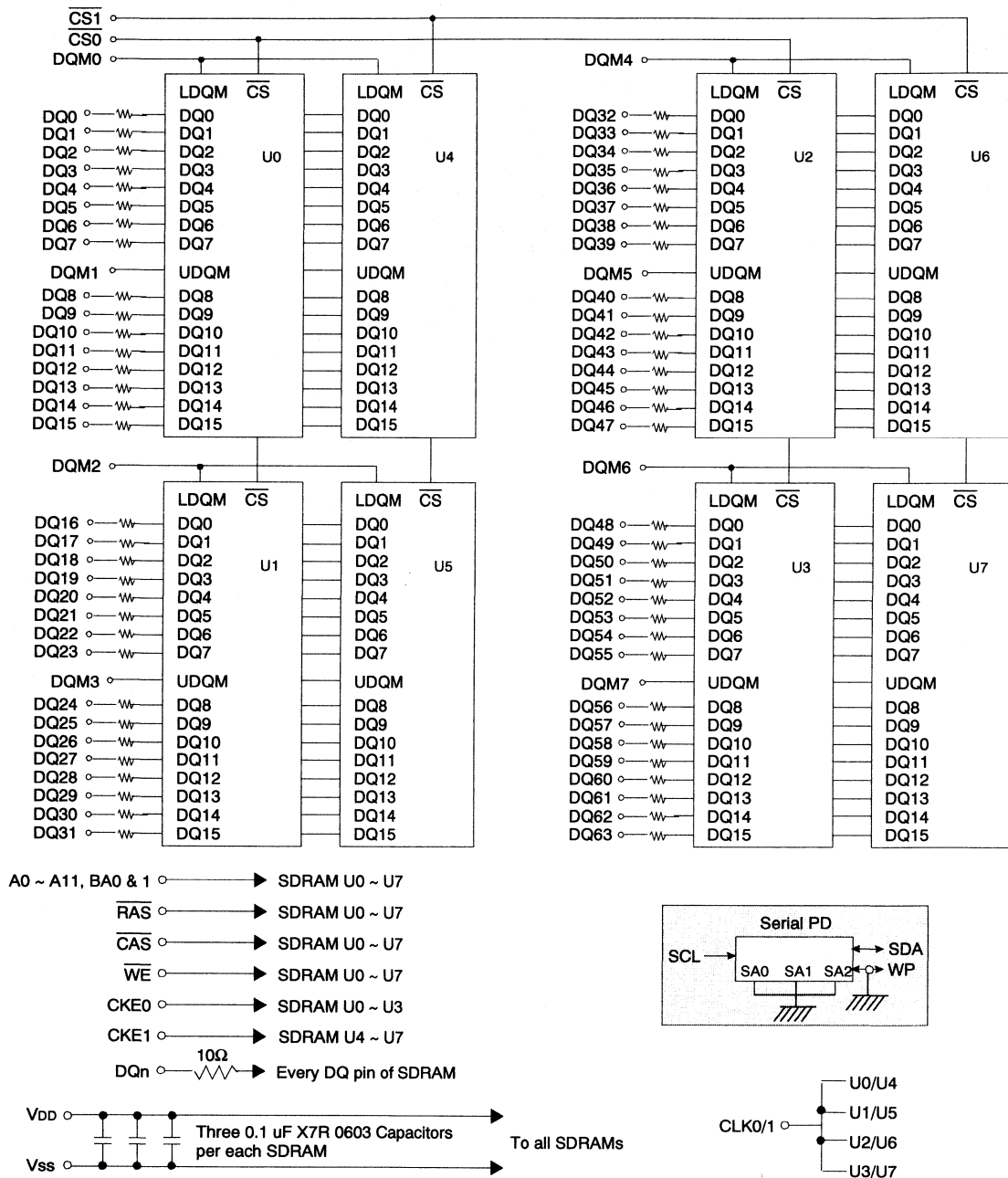
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁)	C _{IN1}	25	45	pF
Input capacitance (<u>RAS</u> , <u>CAS</u> , <u>WE</u>)	C _{IN2}	25	45	pF
Input capacitance (CKE ₀ ~ CKE ₁)	C _{IN3}	15	25	pF
Input capacitance (CLK ₀ ~ CLK ₁)	C _{IN4}	15	21	pF
Input capacitance (CS ₀ ~ CS ₁)	C _{IN5}	15	25	pF
Input capacitance (DQM ₀ ~ DQM ₇)	C _{IN6}	10	12	pF
Data input/output capacitance (DQ ₀ ~ DQ ₆₃)	C _{OUT}	10	12	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}(\min)$ $I_O = 0$ mA	720	mA	1
Precharge standby current in power-down mode	I_{CC2P}	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	8	mA	
	I_{CC2PS}	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	8		
Precharge standby current in non power-down mode	I_{CC2N}	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	160	mA	
	I_{CC2NS}	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	56		
Active standby current in power-down mode	I_{CC3P}	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	40	mA	
	I_{CC3PS}	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	40		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	240	mA	
	I_{CC3NS}	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	160	mA	
Operating current (Burst mode)	I_{CC4}	$I_O = 0$ mA Page burst 4Banks activated $t_{CCD} = 2CLKs$	840	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}(\min)$	1000	mA	2
Self refresh current	I_{CC6}	$CKE \leq 0.2V$	C	12	mA
			L	6.4	mA

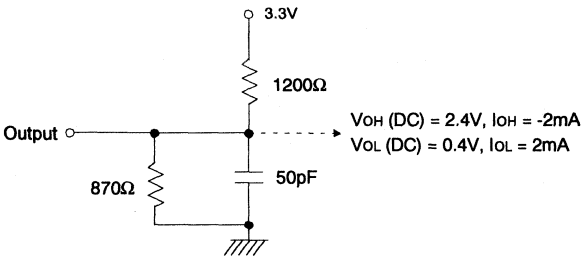
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

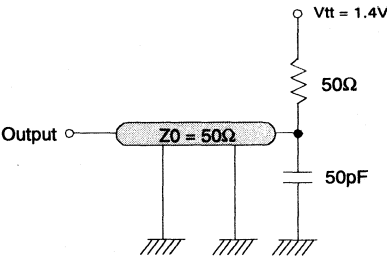
3. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (V _{Ih} /V _{Il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	t _{RRD} (min)	15	ns	1
RAS to CAS delay	t _{RCD} (min)	20	ns	1
Row precharge time	t _{RP} (min)	20	ns	1
Row active time	t _{RAS} (min)	45	ns	1
	t _{RAS} (max)	100	us	
Row cycle time	t _{RC} (min)	65	ns	1
Last data in to row precharge	t _{RDL} (min)	2	CLK	2
Last data in to Active delay	t _{DAL} (min)	2 CLK + 20 ns	-	
Last data in to new col. address delay	t _{CDL} (min)	1	CLK	2
Last data in to burst stop	t _{BDL} (min)	1	CLK	2
Col. address to col. address delay	t _{CCD} (min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	7.5	1000	ns	1
	CAS latency=2		-			
CLK to valid output delay	CAS latency=3	tsAC		5.4	ns	1,2
	CAS latency=2			-		
Output data hold time	CAS latency=3	toH	2.7		ns	2
	CAS latency=2		-			
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tss	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	
	CAS latency=2			-		

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

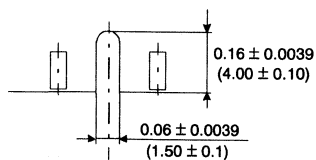
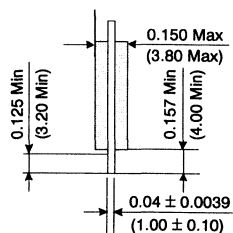
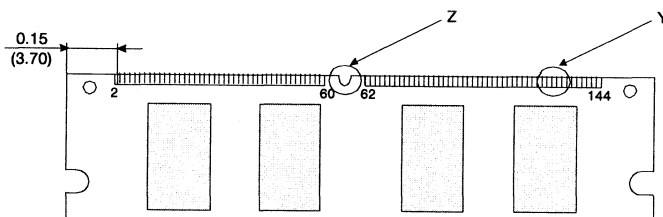
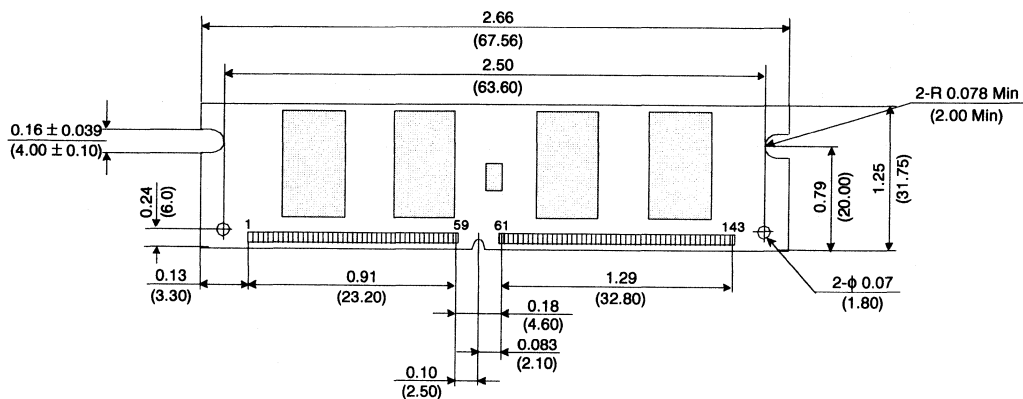
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

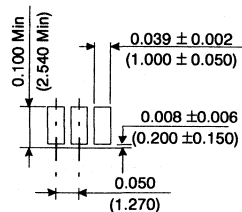
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : $\pm .006(.15)$ unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
SDRAM Part No. : K4S281632B

SERIAL PRESENCE DETECT

PC133 SODIMM

M464S1724BT1-L75/C75

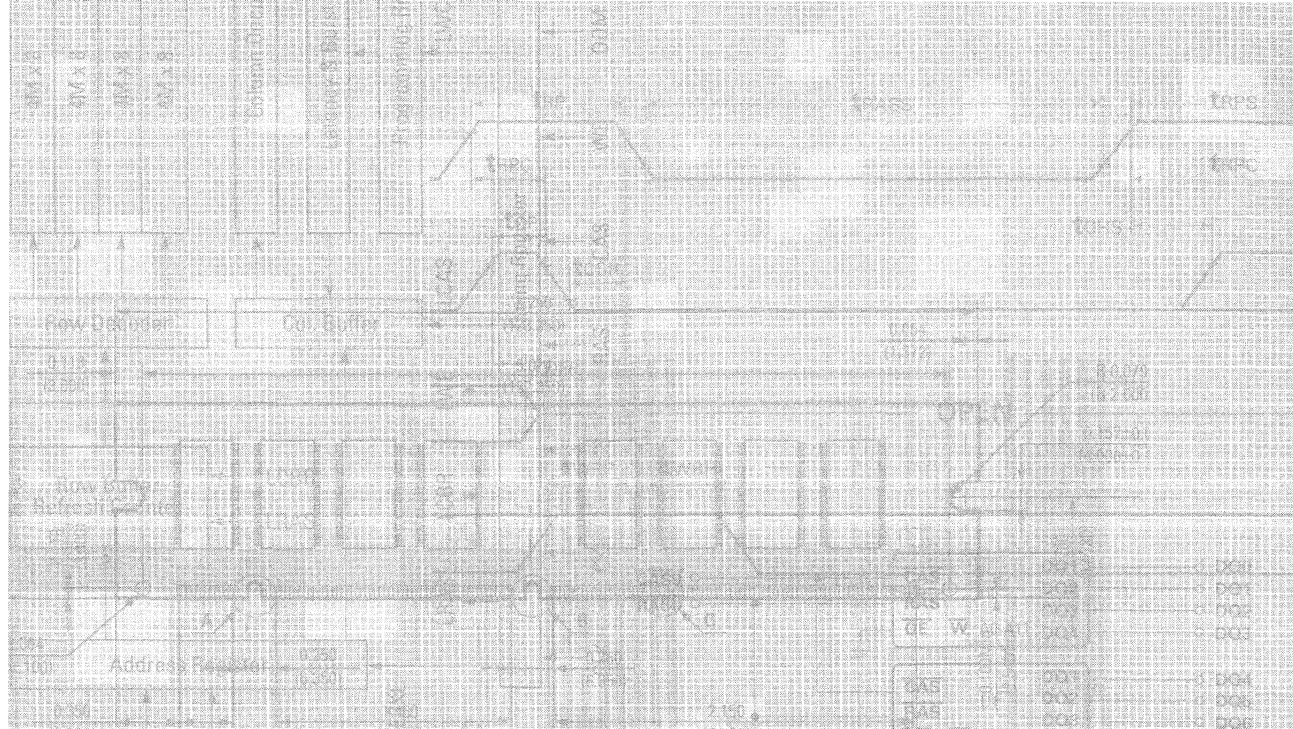
- Organization : 16MX64
- Composition : 8MX16 *8
- Used component part # : K4S281632B-TL75/TC75
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,250 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 64MB	10h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-75		-75		
35	Data signal input hold time	0.8ns		08h		
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	JEDEC 2		02h		
63	Checksum for bytes 0 ~ 62	-		95h		
64	Manufacturer JEDEC ID code	Samsung		CEh		
65~71	 Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM Configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	 Manufacturer part # (Data bits)	6		36h		
77	 Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	 Manufacturer part # (Module depth)	7		37h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2		32h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	B		42h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	1		31h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	L	C	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7		37h		
89	Manufacturer part # (Minimum cycle time)	5		35h		
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	1		31h		
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)		42h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	Reserved	-		64h		6
127	Reserved	Detailed PC100 Information		CDh		6
128+	Unused storage locations	Undefined		-		5

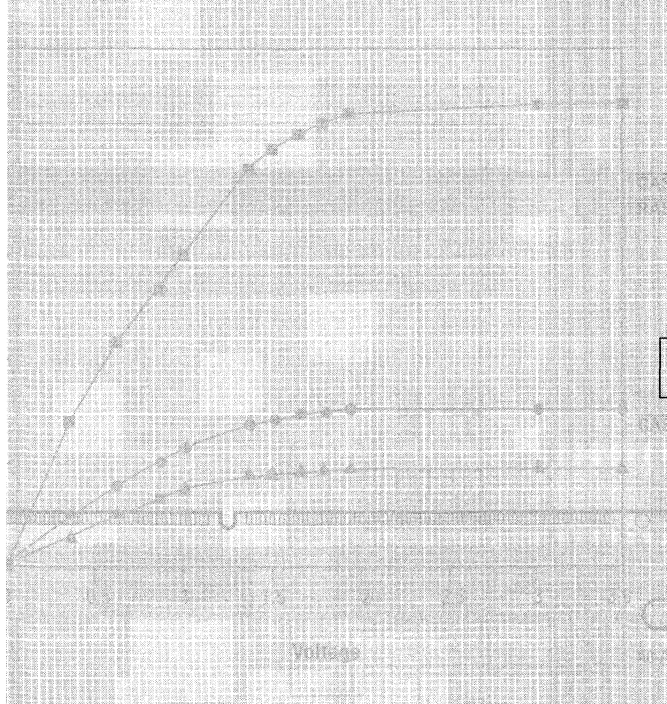
- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.
 6. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.



Module Specification

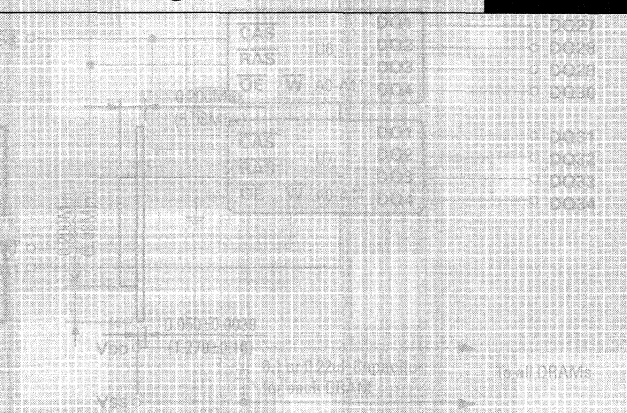
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66MHz and 100MHz PLT 120V



(Back view)

PC133 Registered DIMM



M390S1723AT1 SDRAM DIMM

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M390S1723AT1 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S1723AT1 consists of nine CMOS 16Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S1723AT1 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M390S1723AT1-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,500mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

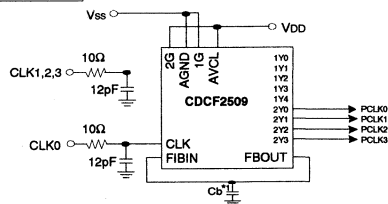
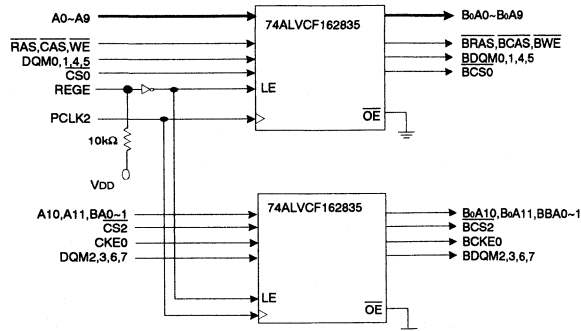
* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

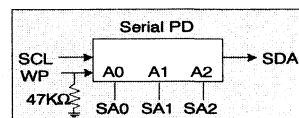
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PIN CONFIGURATION DESCRIPTION

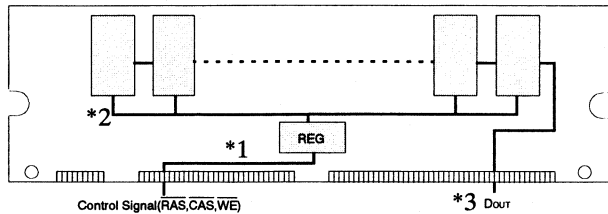
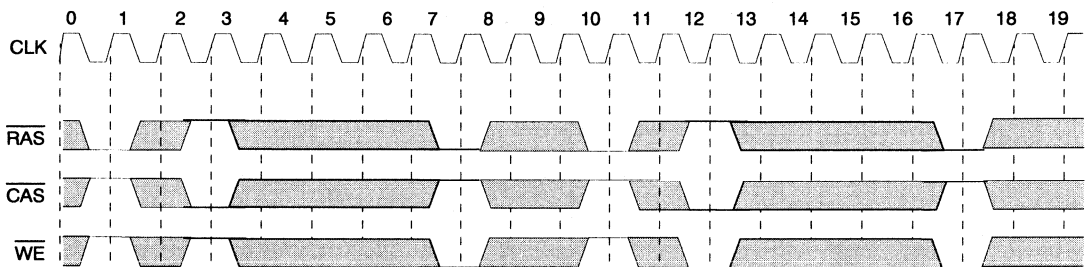
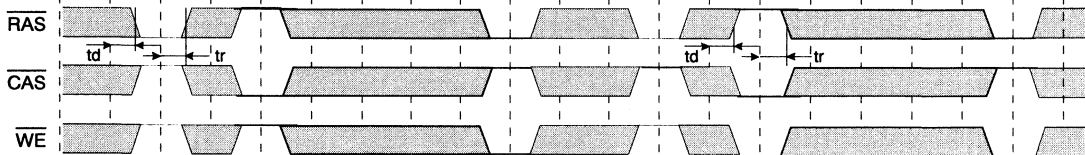
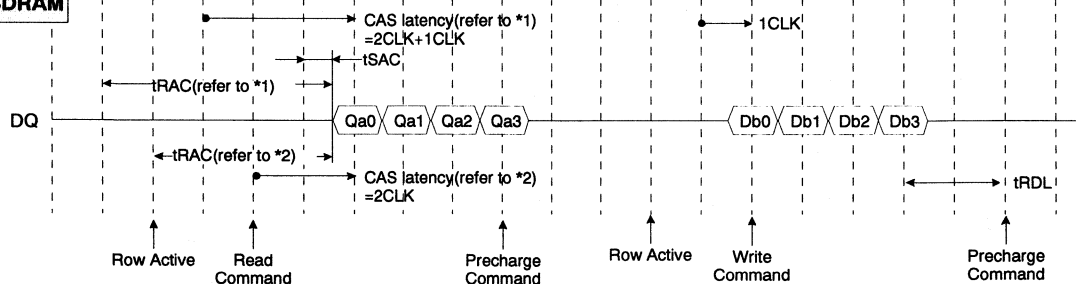
Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V _{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to V _{SS} through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V _{DD} /V _{SS}	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.



Note
1. The actual values of C_b will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

t_d, t_r = Delay of register (74ALVCF162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. Din is to be issued 1clock after write command in external timing because Din is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ VDDQ

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	CIN1	-	15	pF
Input capacitance (RAS, CAS, WE)	CIN2	-	15	pF
Input capacitance (CKE0)	CIN3	-	15	pF
Input capacitance (CLK0)	CIN4	-	23	pF
Input capacitance (CS0, CS2)	CIN5	-	15	pF
Input capacitance (DQM0 ~ DQM7)	CIN6	-	15	pF
Input capacitance (BA0 ~ BA1)	CIN7	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	COUT	-	16	pF
Data input/output capacitance (CB0 ~ CB7)	COUT1	-	16	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\min)$ $I_O = 0 \text{ mA}$	1,580	mA	1
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	359	mA	3
	ICC2PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	11		
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	530	mA	3
	ICC2NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	65		
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	395	mA	3
	ICC3PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	47		
Active standby current in non power-down mode	ICC3N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	620	mA	3
	ICC3NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	182	mA	3
Operating current (Burst mode)	ICC4	$I_O = 0\text{mA}$ Page burst 4Banks activated $t_{CCD} = 2CLK$	1,850	mA	1
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\min)$	2,480	mA	2
Self refresh current	ICC6	$CKE \leq 0.2V$	364	mA	3

Notes : 1. Measured with outputs open.

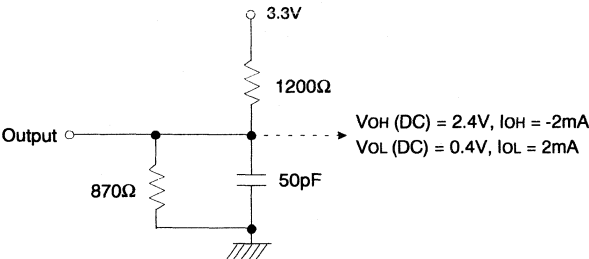
2. Refresh period is 64ms.

3. Measured with 1 PLL & 2 Drive ICs.

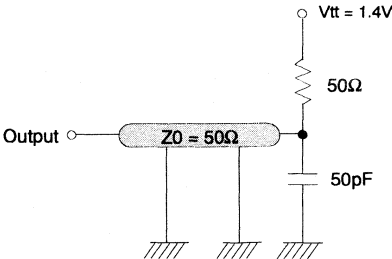
4. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	tRRD(min)	15	ns	1
RAS to CAS delay	tRCD(min)	20	ns	1
Row precharge time	tRP(min)	20	ns	1
Row active time	tRAS(min)	45	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	65	ns	1
Last data in to row precharge	tRDL(min)	2	CLK	2
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns		
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	tSAC	-	5.4	ns	1,2
Output data hold time	CAS latency=3	tOH	2.7	-	ns	1,2
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	1

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L							3		
		Exit	L	H	L	H	H	H	X	X	3		
					H	X	X	X			3		
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

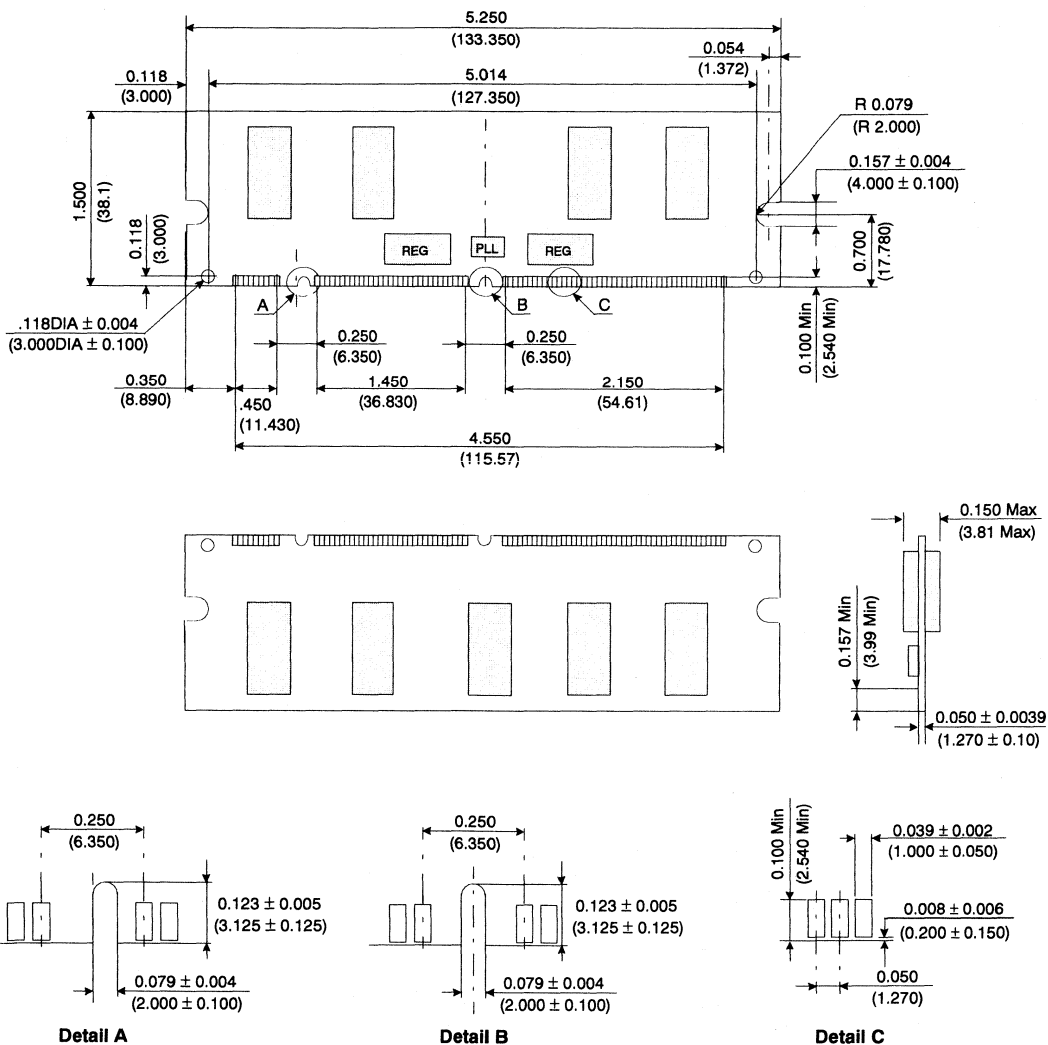
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832A-TC75

This module is based on JEDEC PC133 Specification

SERIAL PRESENCE DETECT

PC133 Registered DIMM

M390S1723AT1-C75

- Organization : 16MX72
- Composition : 16MX8 * 9ea
- Used component part # : K4S280832A-TC75
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC 2	02h	
63	Checksum for bytes 0 ~ 62	-	CEh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	9	39h	
77	 Manufacturer part # (Data bits)	0	30h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	1	31h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	1	31h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	100MHz	64h	
127	Reserved	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M390S3320AT1 SDRAM DIMM

32Mx72 SDRAM DIMM with PLL & Register based on 32Mx4, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M390S3320AT1 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S3320AT1 consists of eighteen CMOS 32Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S3320AT1 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

•Performance range

Part No.	Max Freq. (Speed)
M390S3320AT1-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,700mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	*CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

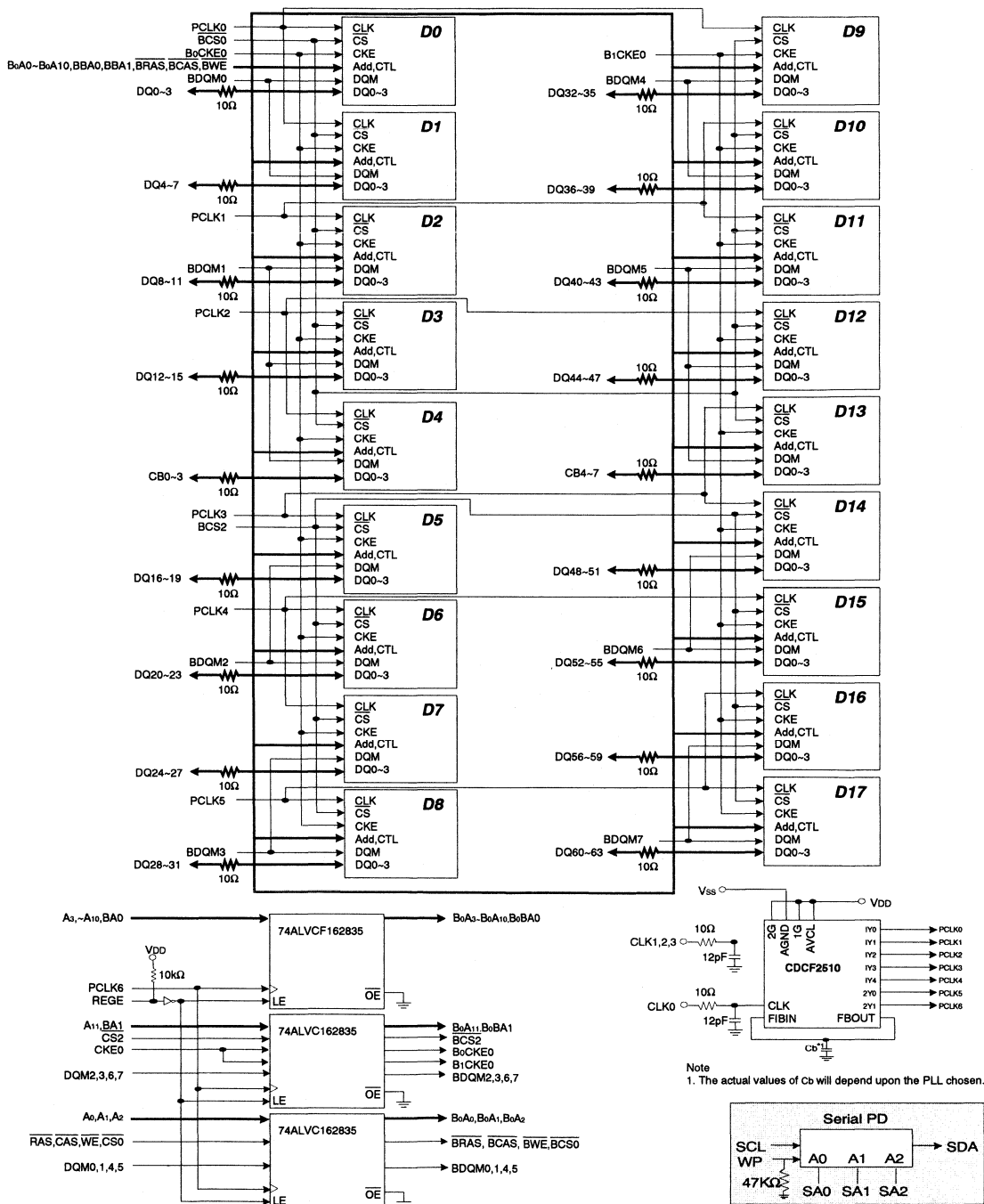
** These pins should be NC in the system which does not support SPD.

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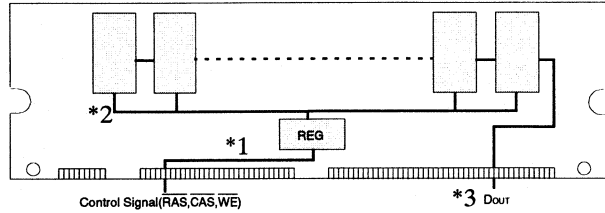
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{CS}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, $\overline{WE}$ active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write Protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

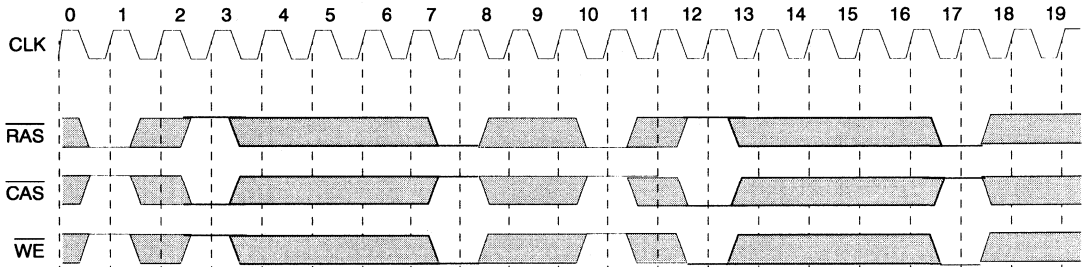
FUNCTIONAL BLOCK DIAGRAM



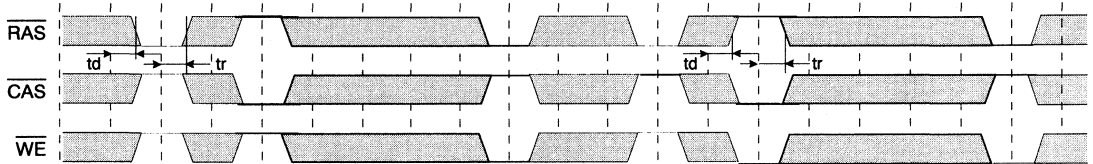
STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)



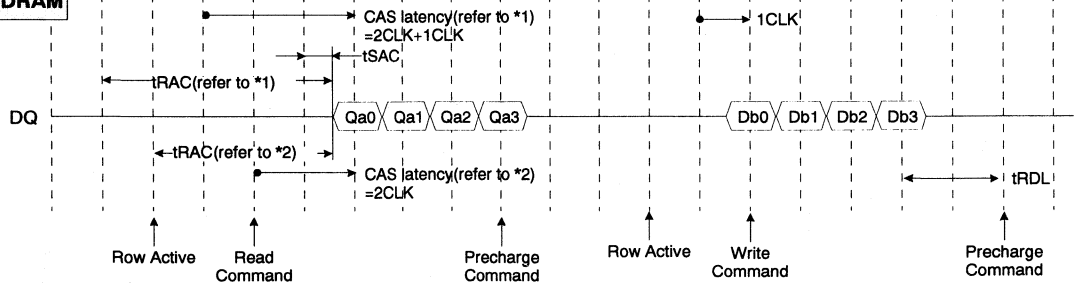
***1. Register Input**



***2. Register Output**



***3. SDRAM**



td, tr = Delay of register (74ALVCF162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ VDDQ.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A11)	C _{IN1}	-	15	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	15	pF
Input capacitance (CKE0)	C _{IN3}	-	15	pF
Input capacitance (CLK0)	C _{IN4}	-	20	pF
Input capacitance (CS0, CS2)	C _{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	16	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	16	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\text{min})$ $I_O = 0 \text{ mA}$	2,660	mA	1,3
Precharge standby current in power-down mode	ICC2P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	368	mA	3
	ICC2PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	20		
Precharge standby current in non power-down mode	ICC2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	710	mA	3
	ICC2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	128		
Active standby current in power-down mode	ICC3P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	440	mA	3
	ICC3PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	92		
Active Standby current in non power-down mode	ICC3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	990	mA	3
	ICC3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	362	mA	3
Operating current (Burst mode)	ICC4	$I_{OL} = 0\text{mA}$ Page burst 4 Banks activated $t_{CCD} = 2\text{CLK}$	3,020	mA	1,3
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\text{min})$	4,460	mA	2,3
Self refresh current	ICC6	$\text{CKE} \leq 0.2\text{V}$	377	mA	3

Notes : 1. Measured with outputs open.

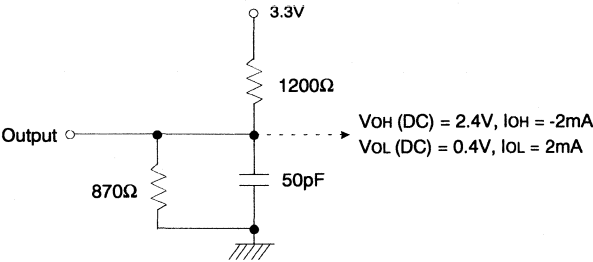
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

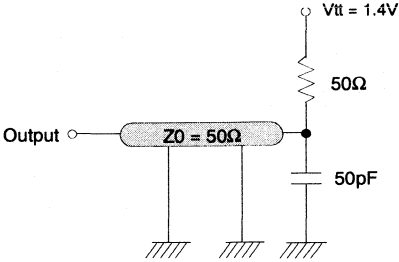
4. Unless otherwise noticed, Input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	tRRD(min)	15	ns	1
RAS to CAS delay	tRCD(min)	20	ns	1
Row precharge time	tRP(min)	20	ns	1
Row active time	tRAS(min)	45	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	65	ns	1
Last data in to row precharge	tRDL(min)	2	CLK	2
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns		
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	tsAC	-	5.4	ns	1,2
Output data hold time	CAS latency=3	tOH	2.7	-	ns	1,2
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	1

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3
	Self refresh	L		L	L	L	H	X	X		3	
		Exit	L	H	L	H	H	H	X	X		3
					H	X	X	X				3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9, A11)	4
	Auto precharge enable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9, A11)	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks								X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X		
					L	V	V	V				
		Exit	L	H	X	X	X	X	X			
Precharge power down mode		Entry	H	L	H	X	X	X	X	X		
					L	H	H	H				
		Exit	L	H	H	X	X	X	X			
					L	V	V	V				
DQM		H	X					V	X		7	
No operation command		H	X	H	X	X	X	X	X			
				L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

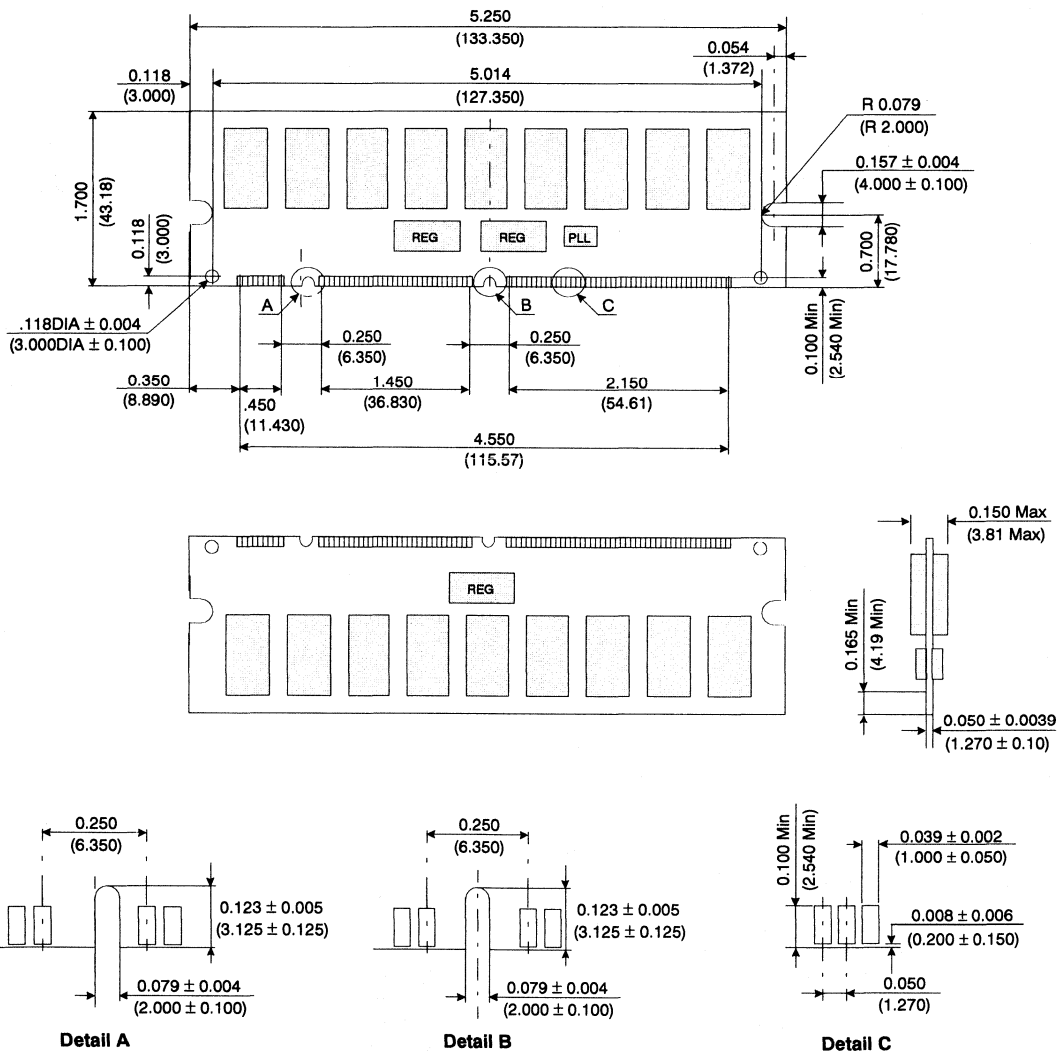
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC133 Registered DIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 32Mx4 SDRAM, TSOP
SDRAM Part No. : K4S280432A-TC75

This module is based on JEDEC PC133 Specification

SERIAL PRESENCE DETECT

PC133 Registered DIMM

M390S3320AT1-C75

- Organization : 32MX72
- Composition : 32MX4 * 18ea
- Used component part # : K4S280432A-TC75
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	11	0Bh	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x4	04h	
14	Error checking SDRAM width	x4	04h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, & 8 Page	0Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 256MB	40h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC 2	02h	
63	Checksum for bytes 0 ~ 62	-	67h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	9	39h	
77	 Manufacturer part # (Data bits)	0	30h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	 Manufacturer part # (Module depth)	3	33h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	0	30h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	1	31h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	1	31h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	100MHz	64h	
127	Reserved	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M390S1723BT1 SDRAM DIMM

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx8, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M390S1723BT1 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S1723BT1 consists of nine CMOS 16Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S1723BT1 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M390S1723BT1-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,500mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

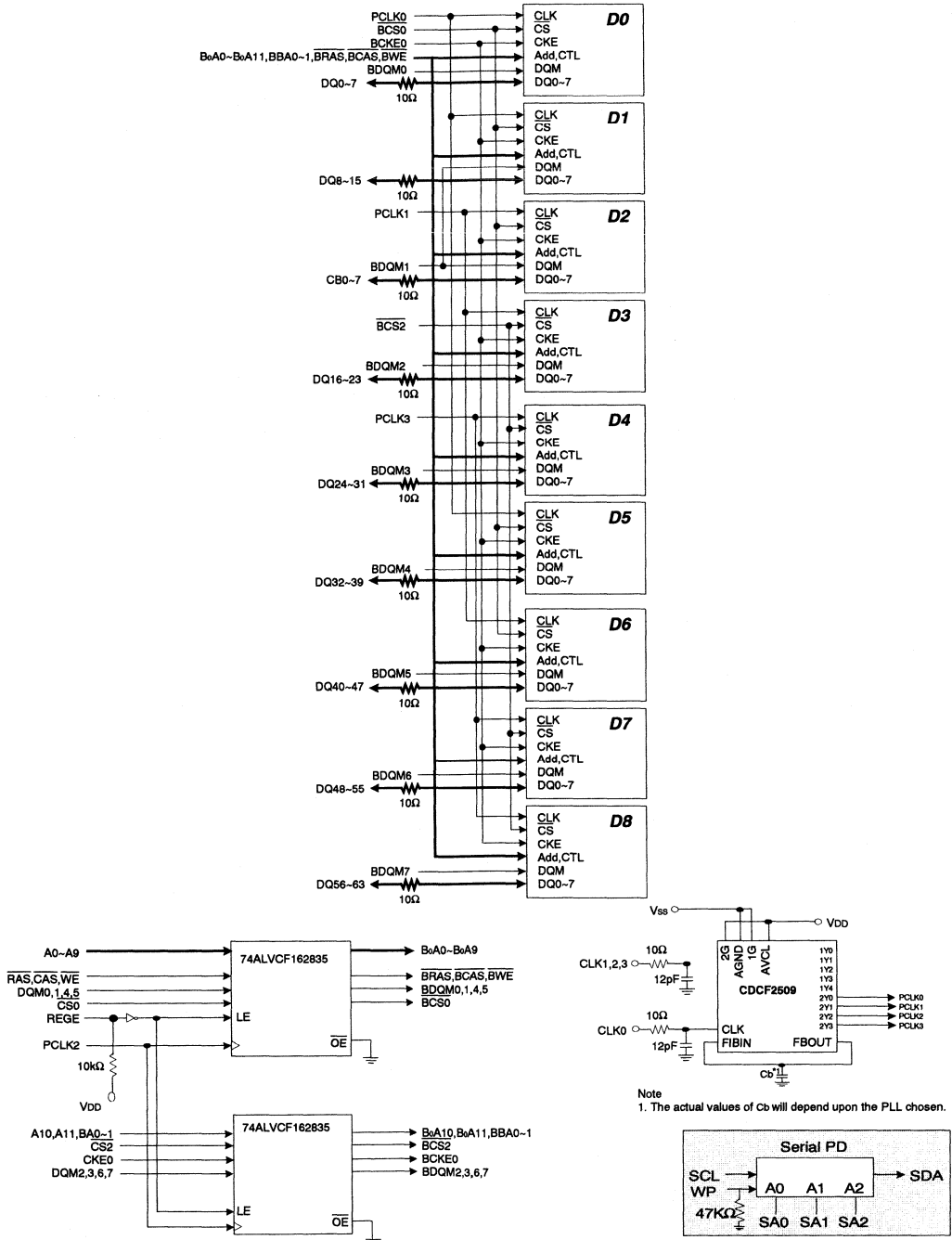
** These pins should be NC in the system which does not support SPD.

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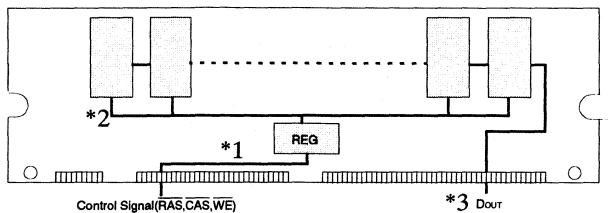
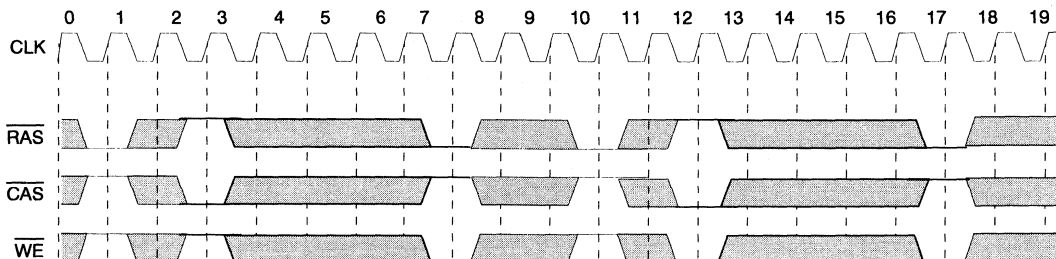
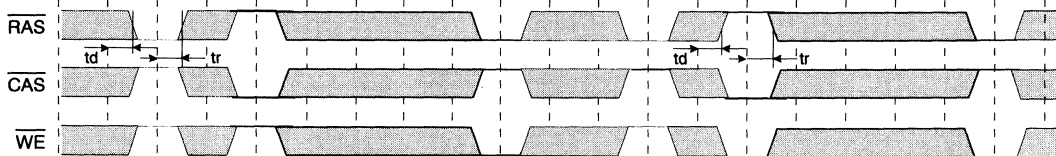
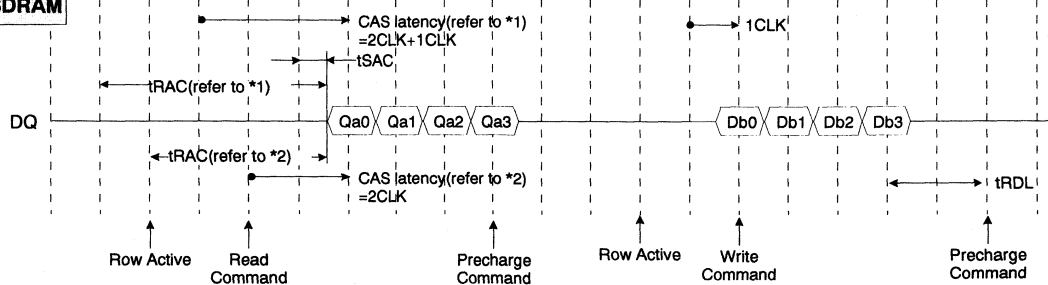
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	Register enable	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Check bit	Check bits for ECC.
WP	Write protection	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

t_d , t_r = Delay of register (74ALVCF162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. D_{in} is to be issued 1clock after write command in external timing because D_{in} is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁)	C _{IN1}	-	15	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	15	pF
Input capacitance (CKE0)	C _{IN3}	-	15	pF
Input capacitance (CLK0)	C _{IN4}	-	23	pF
Input capacitance (CS ₀ , CS ₂)	C _{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	16	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	16	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC(min)}$ $I_O = 0 \text{ mA}$	1,580	mA	1
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL(max)}$, $t_{CC} = 10\text{ns}$	359	mA	3
	ICC2PS	$CKE \& CLK \leq V_{IL(max)}$, $t_{CC} = \infty$	11		
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH(min)}$, $\overline{CS} \geq V_{IH(min)}$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	530	mA	3
	ICC2NS	$CKE \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$, $t_{CC} = \infty$ Input signals are stable	65		
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL(max)}$, $t_{CC} = 10\text{ns}$	395	mA	3
	ICC3PS	$CKE \& CLK \leq V_{IL(max)}$, $t_{CC} = \infty$	47		
Active standby current in non power-down mode	ICC3N	$CKE \geq V_{IH(min)}$, $\overline{CS} \geq V_{IH(min)}$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	620	mA	3
	ICC3NS	$CKE \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$, $t_{CC} = \infty$ Input signals are stable	182	mA	3
Operating current (Burst mode)	ICC4	$I_O = 0\text{mA}$ Page burst 4Banks activated $t_{CCD}=2CLK$	1,850	mA	1
Refresh current	ICC5	$t_{RC} \geq t_{RC(min)}$	2,480	mA	2
Self refresh current	ICC6	$CKE \leq 0.2V$	364	mA	3

Notes : 1. Measured with outputs open.

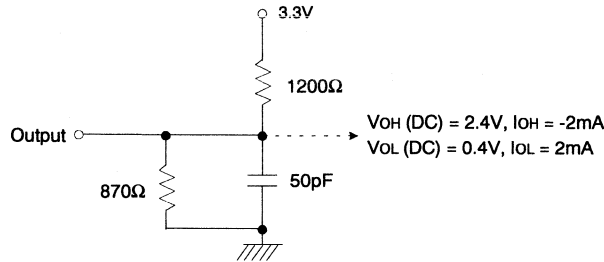
2. Refresh period is 64ms.

3. Measured with 1 PLL & 2 Drive ICs.

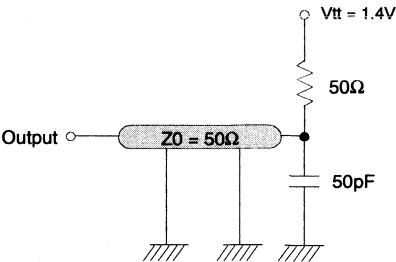
4. Unless otherwise noticed, Input swing level is CMOS($V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	tRRD(min)	15	ns	1
RAS to CAS delay	tRCD(min)	20	ns	1
Row precharge time	tRP(min)	20	ns	1
Row active time	tRAS(min)	45	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	65	ns	1
Last data in to row precharge	tRDL(min)	2	CLK	2
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns		
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	tsAC	-	5.4	ns	1,2
Output data hold time	CAS latency=3	tOH	2.7	-	ns	1,2
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	1

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note			
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2			
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3			
	Self refresh	Entry		L									3			
		Exit	L	H	L	H	H	H	X	X			3			
					H	X	X	X					3			
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address					
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4			
	Auto precharge enable										H		4,5			
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4			
	Auto precharge enable										H		4,5			
Burst stop			H	X	L	H	H	L	X	X			6			
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X				
	All banks									X	H					
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X						
					L	V	V	V								
		Exit	L	H	X	X	X	X	X							
Precharge power down mode		Entry	H	L	H	X	X	X	X	X						
					L	H	H	H								
		Exit	L	H	H	X	X	X	X							
					L	V	V	V								
DQM			H	X					V	X		7				
No operation command			H	X	H	X	X	X	X	X						
					L	H	H	H								

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

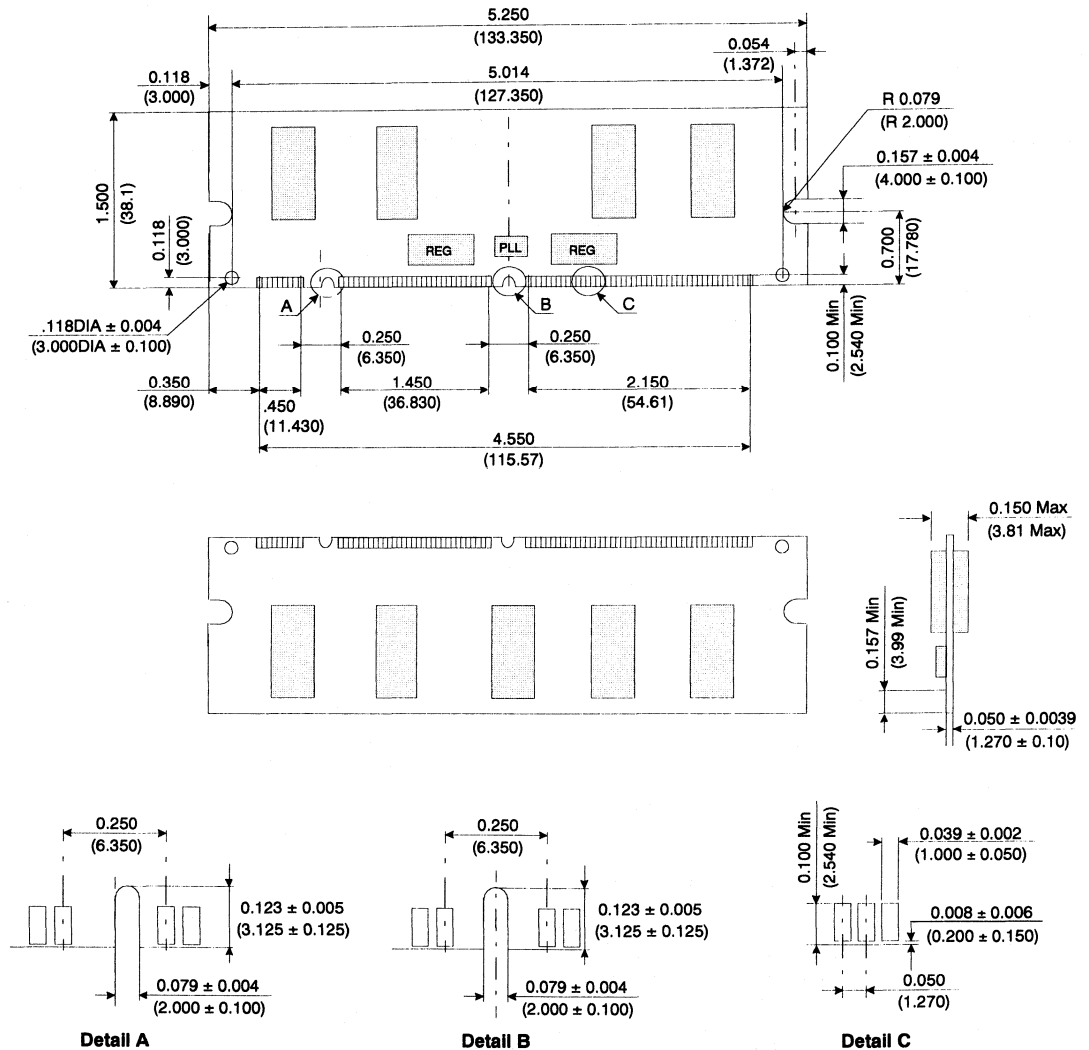
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832B-TC75

This module is based on JEDEC PC133 Specification

M390S1723BT1-C75

•Organization : 16MX72

•Composition : 16MX8 * 9ea

•Used component part # : K4S280832B-TC75

•# of banks in module : 1 Row

•# of banks in component : 4 banks

•Feature : 1,500 mil height & double sided component

•Refresh : 4K/64ms

•Contents :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraon type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC 2	02h	
63	Checksum for bytes 0 ~ 62	-	CEh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	9	39h	
77	 Manufacturer part # (Data bits)	0	30h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	1	31h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	1	31h	
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	100MHz	64h	
127	Reserved	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M390S3320BT1 SDRAM DIMM

32Mx72 SDRAM DIMM with PLL & Register based on 32Mx4, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M390S3320BT1 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S3320BT1 consists of eighteen CMOS 32Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S3320BT1 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE
•Performance range

Part No.	Max Freq. (Speed)
M390S3320BT1-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

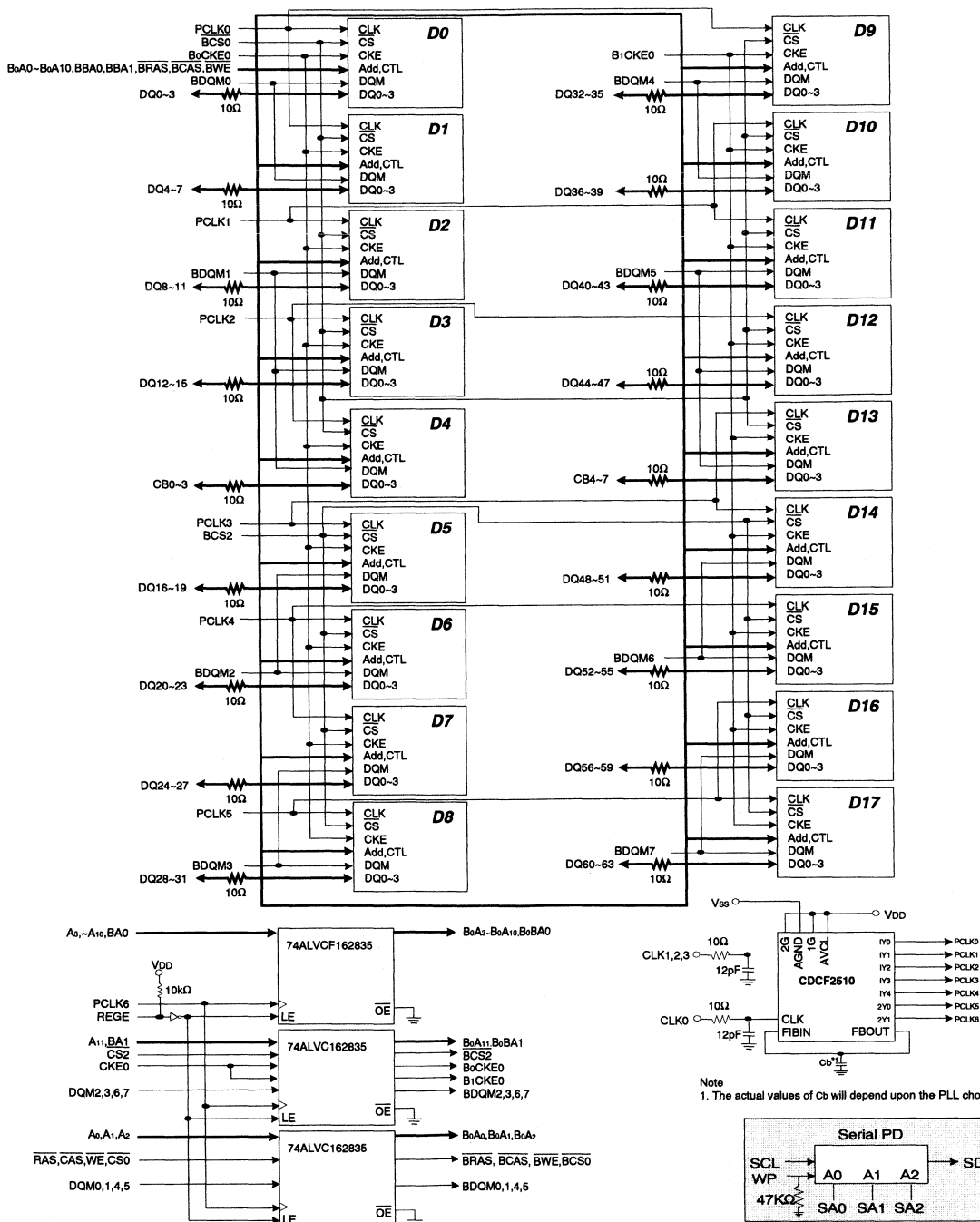
** These pins should be NC in the system which does not support SPD.

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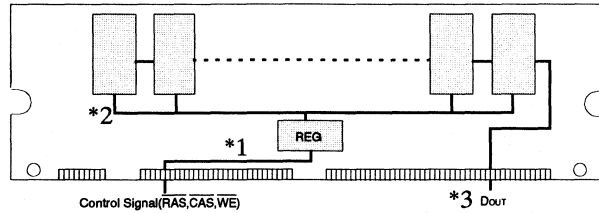
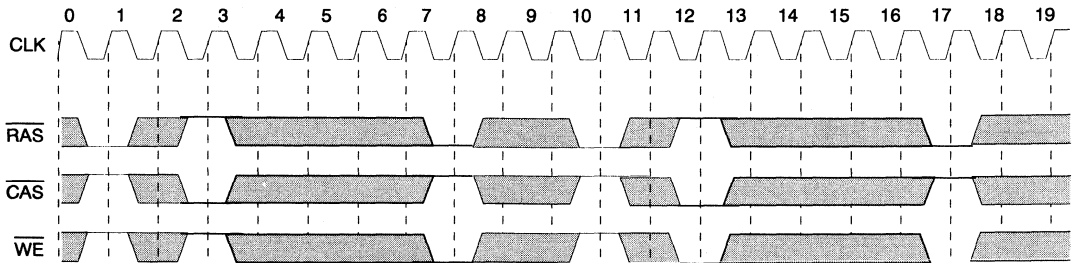
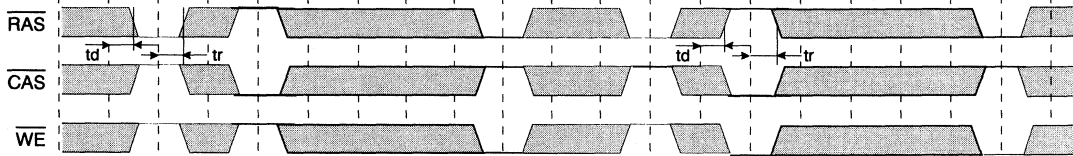
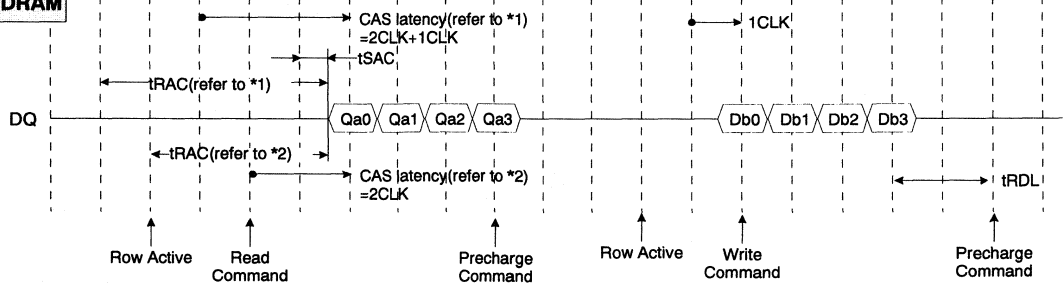
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V _{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write Protection</i>	WP pin is connected to V _{SS} through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
V _{DD} /V _{SS}	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

td, tr = Delay of register (74ALVCF162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. Din is to be issued 1clock after write command in external timing because Din is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₁)	C _{IN1}	-	15	pF
Input capacitance (R _{AS} , C _{AS} , W _E)	C _{IN2}	-	15	pF
Input capacitance (C _{KE0})	C _{IN3}	-	15	pF
Input capacitance (C _{LK0})	C _{IN4}	-	20	pF
Input capacitance (C _{S0} , C _{S2})	C _{IN5}	-	15	pF
Input capacitance (D _{QM0} ~ D _{QM7})	C _{IN6}	-	15	pF
Input capacitance (B _{A0} ~ B _{A1})	C _{IN7}	-	15	pF
Data input/output capacitance (D _{Q0} ~ D _{Q63})	C _{OUT}	-	16	pF
Data input/output capacitance (C _{B0} ~ C _{B7})	C _{OUT1}	-	16	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\min)$ $I_O = 0 \text{ mA}$	2,660	mA	1,3
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	368	mA	3
	ICC2PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	20		
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	710	mA	3
	ICC2NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	128		
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	440	mA	3
	ICC3PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	92		
Active Standby current in non power-down mode	ICC3N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	990	mA	3
	ICC3NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	362	mA	3
Operating current (Burst mode)	ICC4	$I_{OL} = 0\text{mA}$ Page burst 4 Banks activated $t_{CCD} = 2CLK$	3,020	mA	1,3
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\min)$	4,460	mA	2,3
Self refresh current	ICC6	$CKE \leq 0.2V$	377	mA	3

Notes : 1. Measured with outputs open.

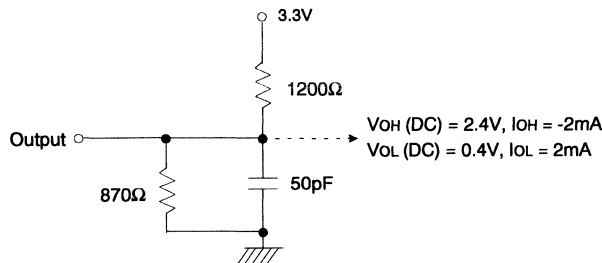
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

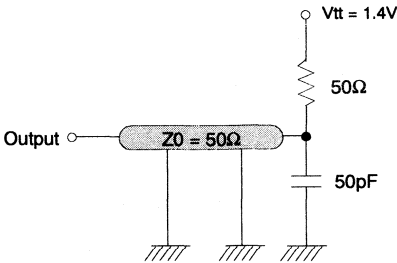
4. Unless otherwise noticed, Input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	tRRD(min)	15	ns	1
RAS to CAS delay	tRCD(min)	20	ns	1
Row precharge time	tRP(min)	20	ns	1
Row active time	tRAS(min)	45	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	65	ns	1
Last data in to row precharge	tRDL(min)	2	CLK	2
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns		
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	tsac	-	5.4	ns	1,2
Output data hold time	CAS latency=3	toH	2.7	-	ns	1,2
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tss	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	1

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9, A11)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9, A11)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

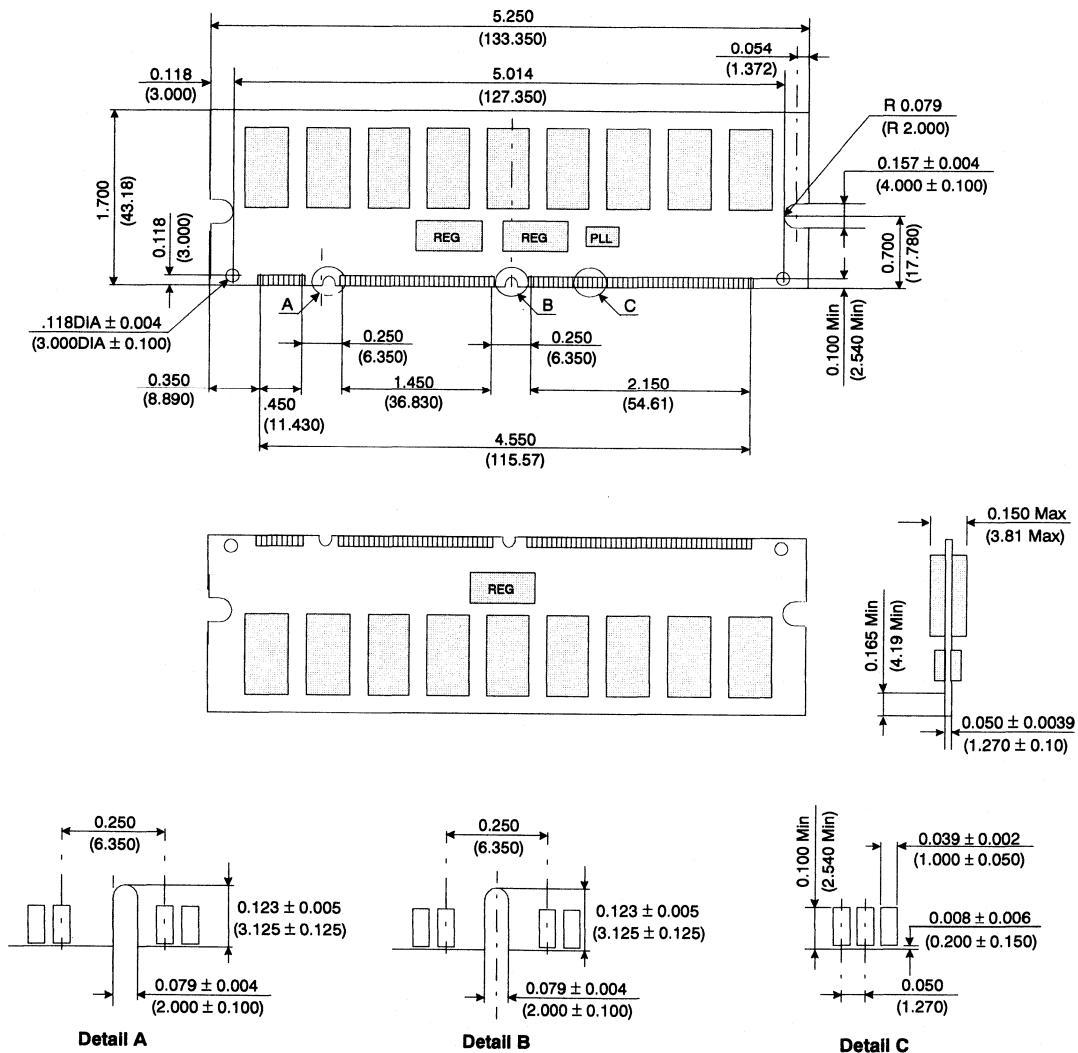
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

M390S3320BT1 **PC133 Registered DIMM**

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 32Mx4 SDRAM, TSOP
SDRAM Part No. : K4S280432B-TC75

This module is based on JEDEC PC133 Specification

M390S3320BT1-C75

- Organization : 32MX72
- Composition : 32MX4 * 18ea
- Used component part # : K4S280432B-TC75
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 4K/64ms
- Contents :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	11	0Bh	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x4	04h	
14	Error checking SDRAM width	x4	04h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, & 8 Page	0Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 256MB	40h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC 2	02h	
63	Checksum for bytes 0 ~ 62	-	67h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	9	39h	
77	 Manufacturer part # (Data bits)	0	30h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	 Manufacturer part # (Module depth)	3	33h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	0	30h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	1	31h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	1	31h	
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	100MHz	64h	
127	Reserved	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The row select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsung's own purpose.

M390S3253AT1 SDRAM DIMM

32Mx72 SDRAM DIMM with PLL & Register based on 32Mx8, 4Banks 8K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M390S3253AT1 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S3253AT1 consists of nine CMOS 32Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S3253AT1 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M390S3253AT1-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,500mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

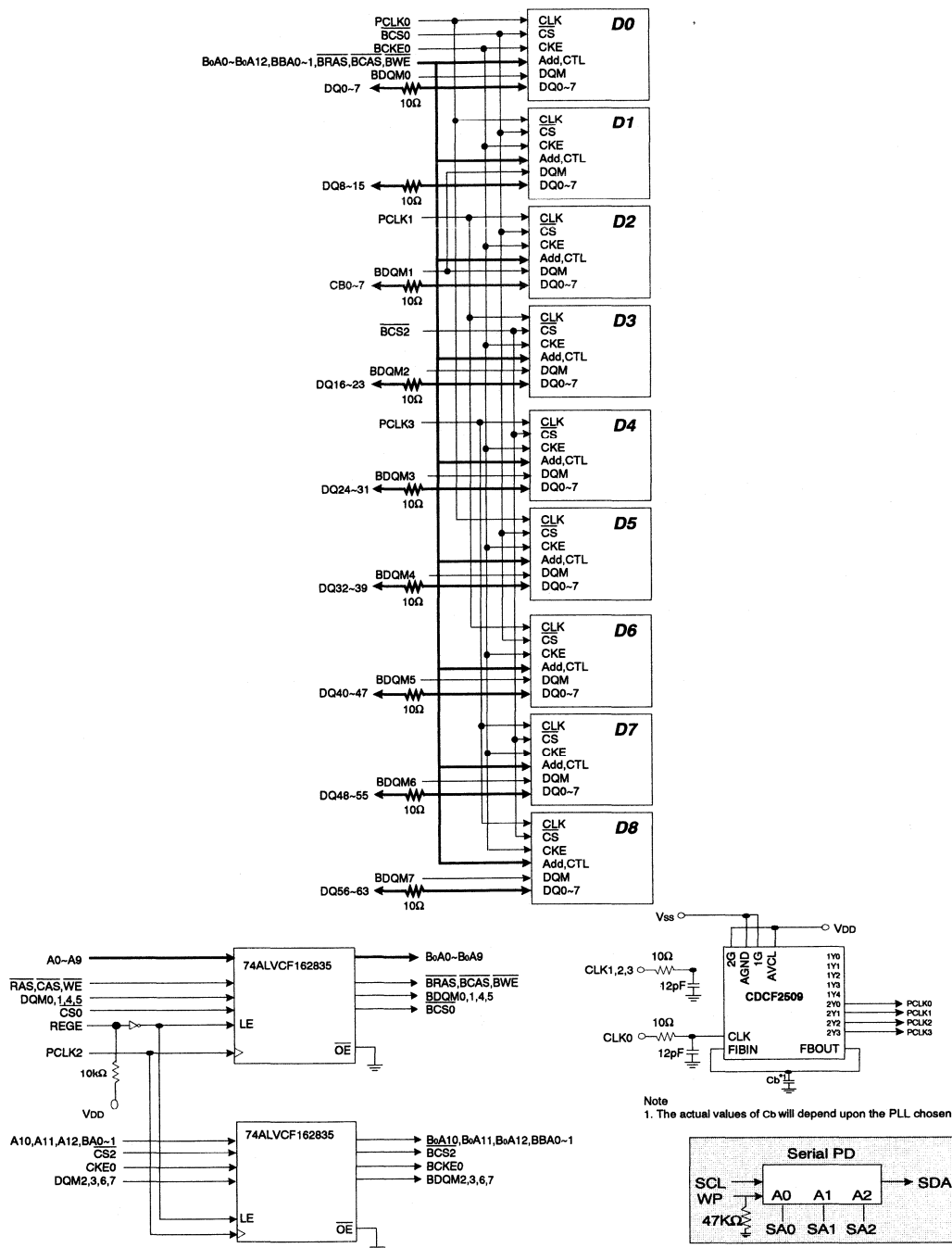
** These pins should be NC in the system which does not support SPD.

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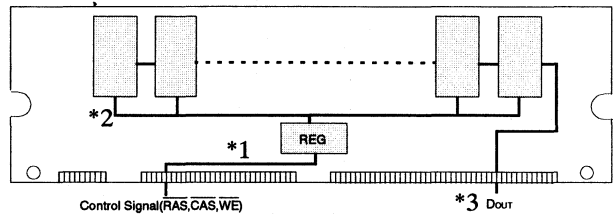
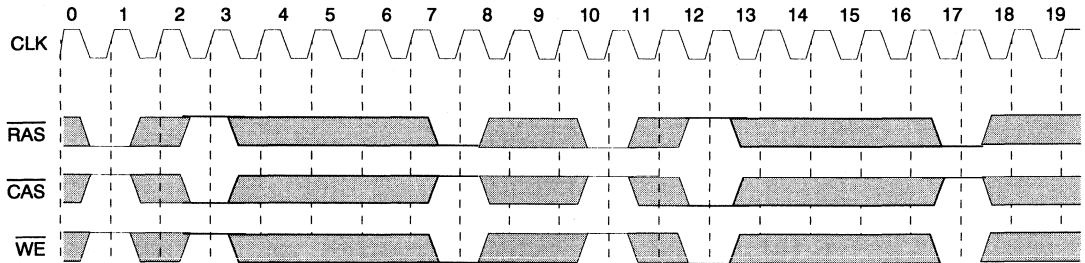
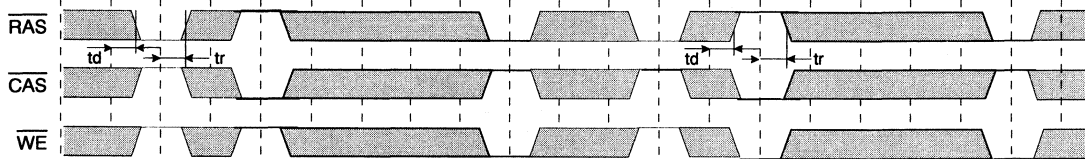
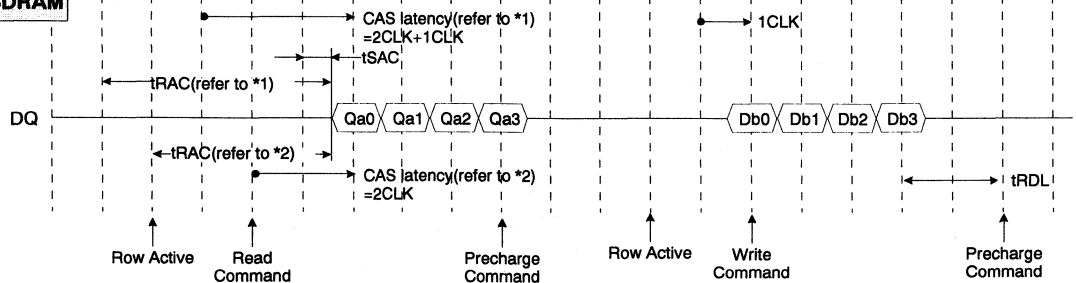
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

t_d, t_r = Delay of register (74ALVCF162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12)	C _{IN1}	-	15	pF
Input capacitance (RAS, CAS, WE)	C _{IN2}	-	15	pF
Input capacitance (CKE0)	C _{IN3}	-	15	pF
Input capacitance (CLK0)	C _{IN4}	-	23	pF
Input capacitance (CS0, CS2)	C _{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	16	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	16	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\min)$ $I_O = 0$ mA	1,630	mA	1
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	368	mA	3
	ICC2PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	20		
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	494	mA	3
	ICC2NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	128		
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	404	mA	3
	ICC3PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	56		
Active standby current in non power-down mode	ICC3N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	620	mA	3
	ICC3NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	227	mA	3
Operating current (Burst mode)	ICC4	$I_O = 0\text{mA}$ Page burst 4Banks activated $t_{CCD} = 2CLK$	1,610	mA	1
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\min)$	2,240	mA	2
Self refresh current	ICC6	$CKE \leq 0.2V$	395	mA	3

Notes : 1. Measured with outputs open.

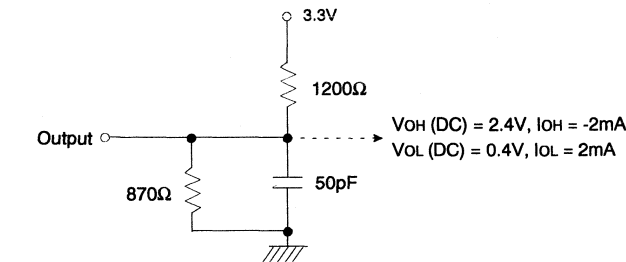
2. Refresh period is 64ms.

3. Measured with 1 PLL & 2 Drive ICs.

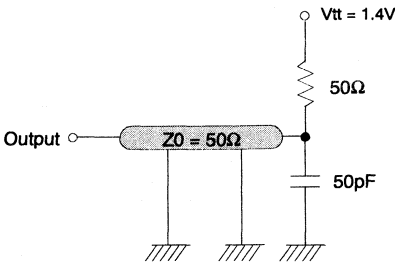
4. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	tRRD(min)	15	ns	1
RAS to CAS delay	tRCD(min)	20	ns	1
Row precharge time	tRP(min)	20	ns	1
Row active time	tRAS(min)	45	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	65	ns	1
Last data in to row precharge	tRDL(min)	2	CLK	2
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns		
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	tSAC	-	5.4	ns	1,2
Output data hold time	CAS latency=3	tOH	2.7	-	ns	1,2
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	1

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11,A12 A9 ~ A0	Note
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3
	Self refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X	X		3
					H	X	X	X				3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks								X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X		
					L	V	V	V				
		Exit	L	H	X	X	X	X	X			
Precharge power down mode		Entry	H	L	H	X	X	X	X	X		
					L	H	H	H				
		Exit	L	H	H	X	X	X	X			
					L	V	V	V				
DQM		H	X					V	X		7	
No operation command		H	X	H	X	X	X	X	X			
				L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

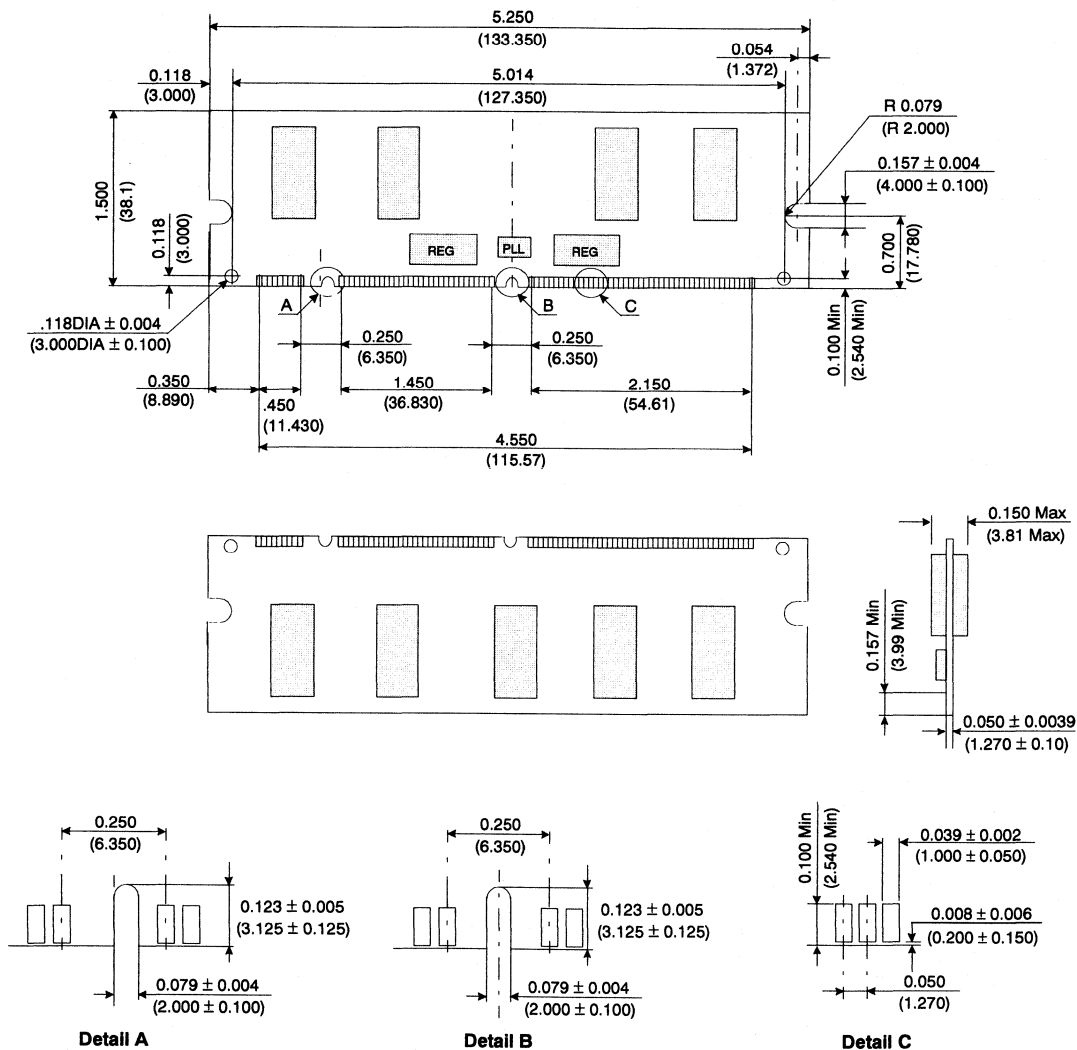
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC133 Registered DIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
SDRAM Part No. : K4S560832A-TC75

This module is based on JEDEC PC133 Specification

SERIAL PRESENCE DETECT

PC133 Registered DIMM

M390S3253AT1-C75

- Organization : 32MX72
- Composition : 32MX8 * 9ea
- Used component part # : K4S560832A-TC75
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,500 mil height & double sided component
- Refresh : 8K/64ms
- Contents :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	7.8us, support self refresh	82h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 256MB	40h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC 2	02h	
63	Checksum for bytes 0 ~ 62	-	F1h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	9	39h	
77	 Manufacturer part # (Data bits)	0	30h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	 Manufacturer part # (Module depth)	2	32h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5	35h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	1	31h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	1	31h	
92	 Manufacturer revision code (For component)	A-dle (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	100MHz	64h	
127	Reserved	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M390S6450AT1 SDRAM DIMM

64Mx72 SDRAM DIMM with PLL & Register based on 64Mx4, 4Banks, 8K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M390S6450AT1 is a 64M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S6450AT1 consists of eighteen CMOS 64Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S6450AT1 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M390S6450AT1-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

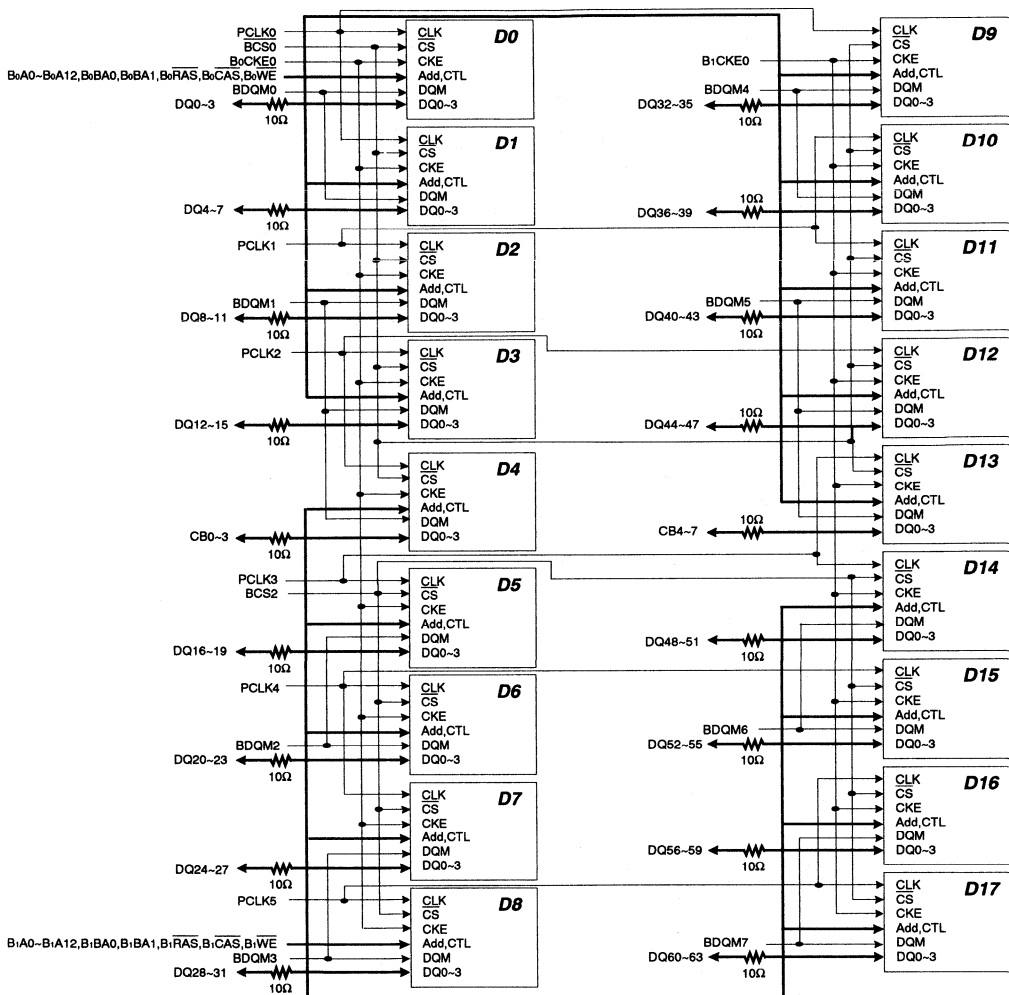
** These pins should be NC in the system which does not support SPD.

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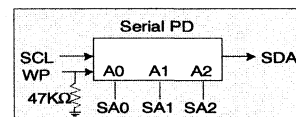
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	Register enable	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Check bit	Check bits for ECC.
WP	Write protection	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.

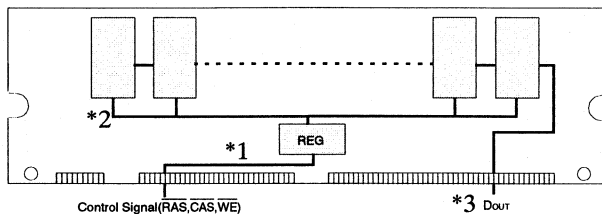
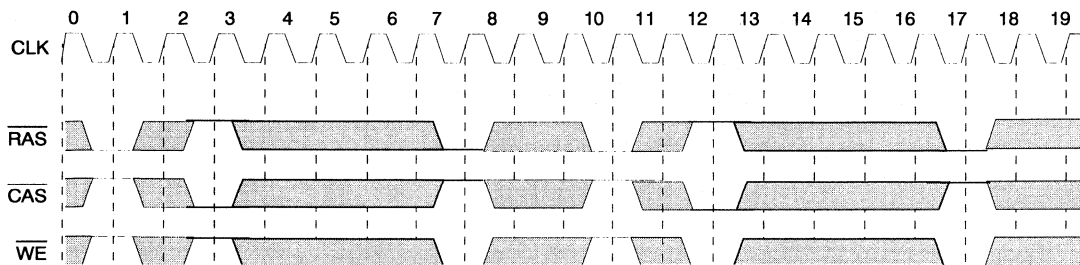
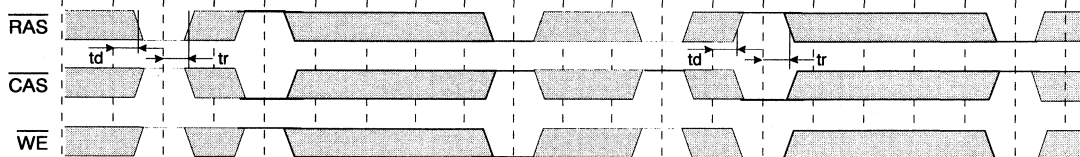
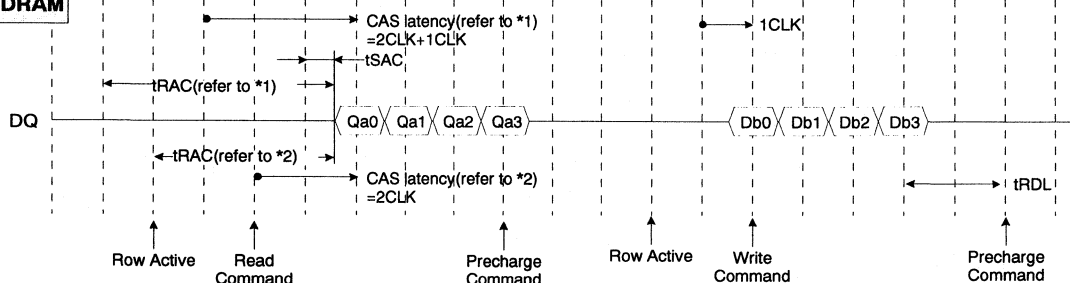
FUNCTIONAL BLOCK DIAGRAM



Note
1. The actual values of Cb will depend upon the PLL chosen.



STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

t_d , t_r = Delay of register (74ALVCF162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	μA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12)	C _{IN1}	-	15	pF
Input capacitance (<u>RAS</u> , <u>CAS</u> , <u>WE</u>)	C _{IN2}	-	15	pF
Input capacitance (CKE0)	C _{IN3}	-	15	pF
Input capacitance (CLK0)	C _{IN4}	-	20	pF
Input capacitance (<u>CS0</u> , <u>CS2</u>)	C _{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	16	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	16	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\min)$ $I_O = 0 \text{ mA}$	2,660	mA	1,3
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	386	mA	3
	ICC2PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	38		
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	638	mA	3
	ICC2NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	254		
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	458	mA	3
	ICC3PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	110		
Active Standby current in non power-down mode	ICC3N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	890	mA	3
	ICC3NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	452	mA	3
Operating current (Burst mode)	ICC4	$I_{OL} = 0\text{mA}$ Page burst 4 Banks activated $t_{CCD} = 2CLK$	3,020	mA	1,3
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\min)$	4,280	mA	2,3
Self refresh current	ICC6	$CKE \leq 0.2V$	440	mA	3

Notes : 1. Measured with outputs open.

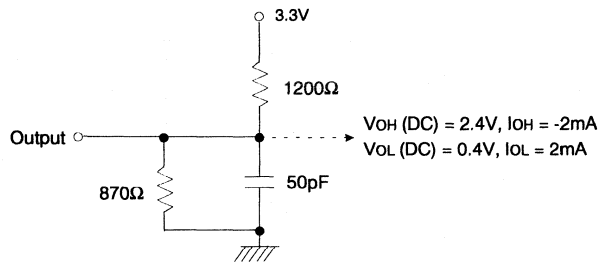
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

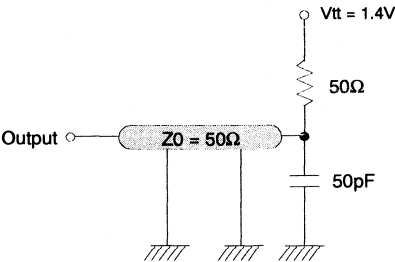
4. Unless otherwise noticed, Input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	tRRD(min)	15	ns	1
RAS to CAS delay	tRCD(min)	20	ns	1
Row precharge time	tRP(min)	20	ns	1
Row active time	tRAS(min)	45	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	65	ns	1
Last data in to row precharge	tRDL(min)	2	CLK	2
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns		
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	tsAC	-	5.4	ns	1,2
Output data hold time	CAS latency=3	tOH	2.7	-	ns	1,2
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tss	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	1

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A12, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9,A11)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9,A11)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

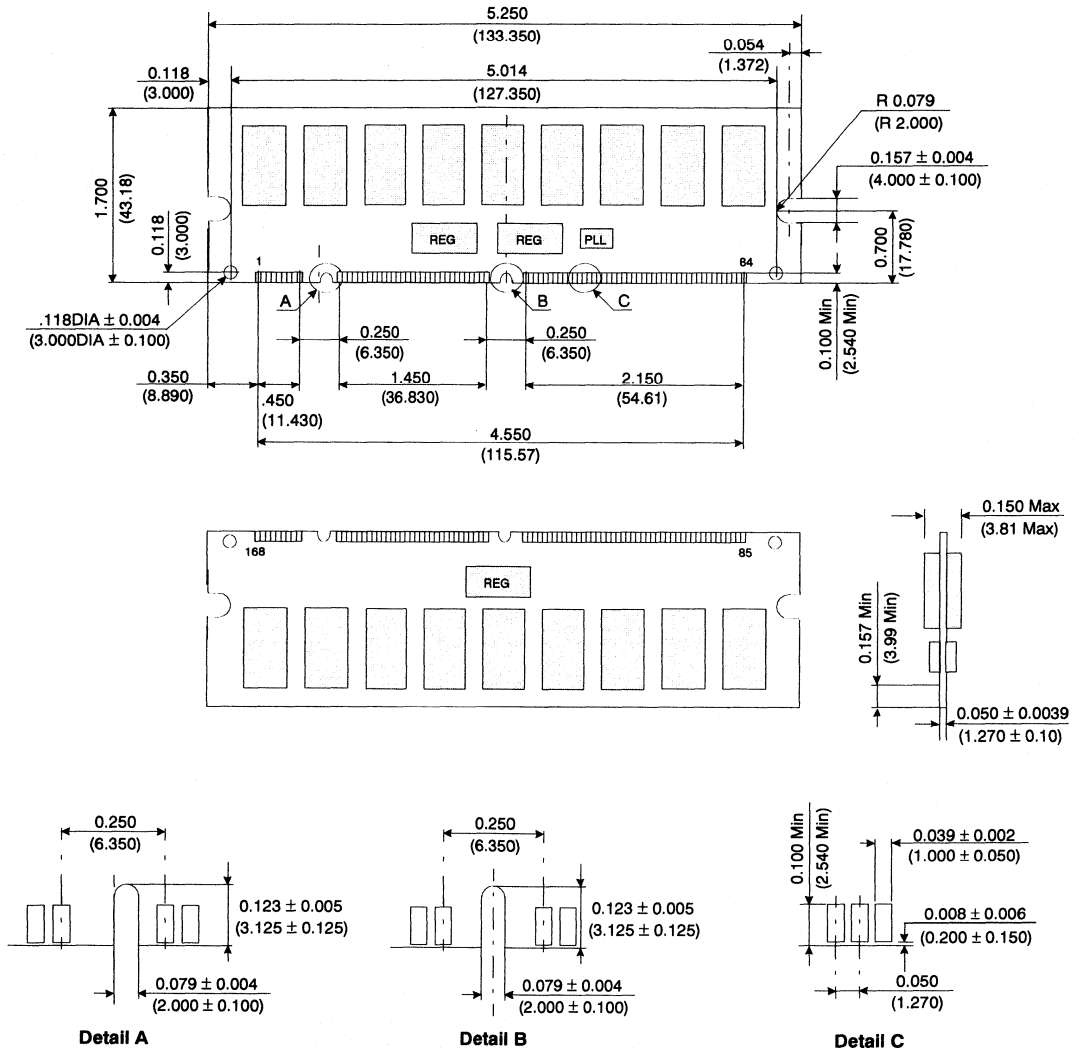
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 64Mx4 SDRAM, TSOP
SDRAM Part No. : K4S560432A-TC75

This module is based on JEDEC PC133 Specification

M390S6450AT1-C75

- Organization : 64MX72
- Composition : 64MX4 * 18ea
- Used component part # : K4S560432A-TC75
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 8K/64ms
- Contents :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	11	0Bh	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	7.8us, support self refresh	82h	
13	Primary SDRAM width	x4	04h	
14	Error checking SDRAM width	x4	04h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 512MB	80h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC 2	02h	
63	Checksum for bytes 0 ~ 62	-	2Ah	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	9	39h	
77	 Manufacturer part # (Data bits)	0	30h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	6	36h	
80	 Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5	35h	
82	Manufacturer part # (Composition component)	0	30h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	1	31h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	1	31h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	100MHz	64h	
127	Reserved	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

M390S2858AT1 SDRAM DIMM

128Mx72 SDRAM DIMM with PLL & Register based on Stacked 128Mx4, 4Banks 8K Ref., 3.3V SDRAMs with SPD

GENERAL DESCRIPTION

The Samsung M390S2858AT1 is a 128M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S2858AT1 consists of eighteen CMOS Stacked 128Mx4 bit Synchronous DRAMs in two TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S2858AT1 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M390S2858AT1-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,700mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

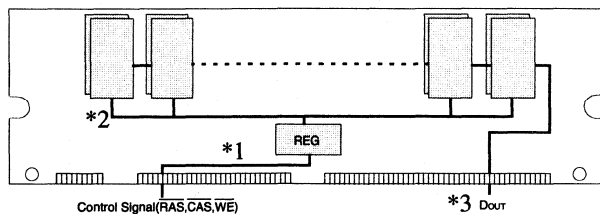
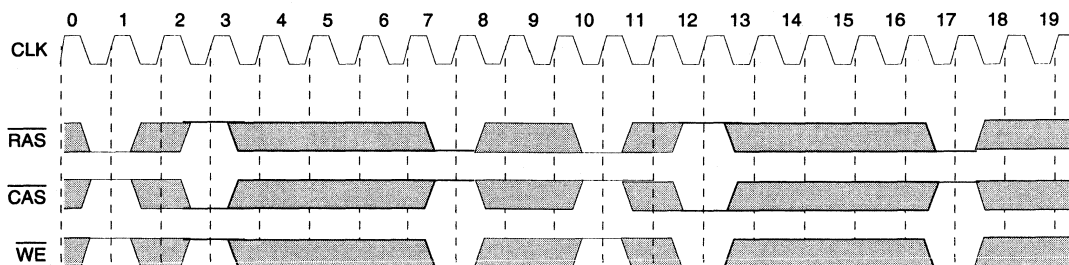
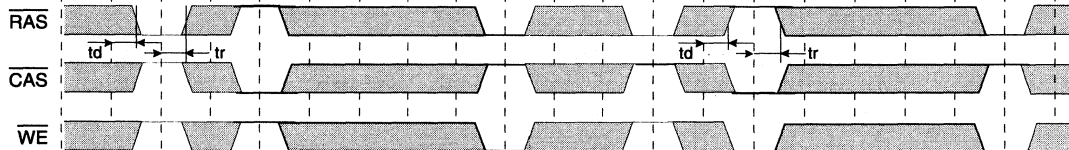
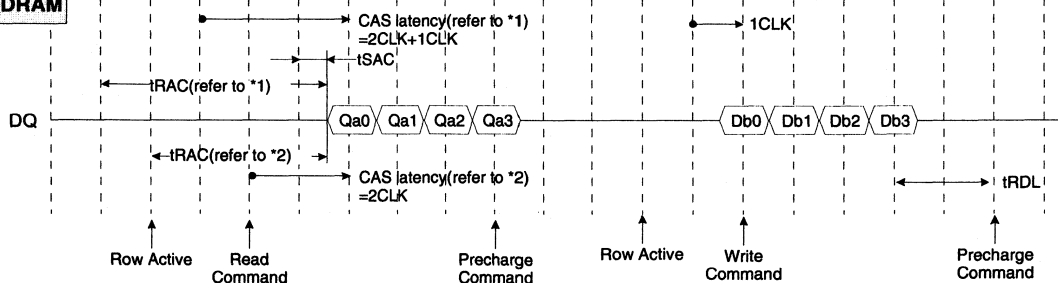
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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{CS}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9, CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to Vdd through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47KΩ Resistor. When WP is "high", EEPROM programming will be inhibited and the entire memory will be write-protected.
Vdd/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

[illegible]

STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)

***1. Register Input*****2. Register Output*****3. SDRAM**

td, tr = Delay of register (74ALVCF162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. Din is to be issued 1clock after write command in external timing because Din is issued directly to module.

□ : Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	36	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	μA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12)	C _{IN1}	-	15	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	-	15	pF
Input capacitance (CKE0)	C _{IN3}	-	15	pF
Input capacitance (CLK0)	C _{IN4}	-	20	pF
Input capacitance ($\overline{\text{CS0}}$, $\overline{\text{CS2}}$)	C _{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C _{IN7}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	22	pF
Data input/output capacitance (CB0 ~ CB7)	C _{OUT1}	-	22	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\min)$ $I_O = 0$ mA	3,200	mA	1,3
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	422	mA	3
	ICC2PS	$CKE \& CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	38		
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	926	mA	3
	ICC2NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	506		
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	566	mA	3
	ICC3PS	$CKE \& CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	218		
Active Standby current in non power-down mode	ICC3N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	1,430	mA	3
	ICC3NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	902	mA	3
Operating current (Burst mode)	ICC4	$I_{OL} = 0\text{mA}$ Page burst 4 Banks activated $t_{CCD} = 2CLK$	3,560	mA	1,3
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\min)$	4,820	mA	2,3
Self refresh current	ICC6	$CKE \leq 0.2V$	530	mA	3

Notes : 1. Measured with outputs open.

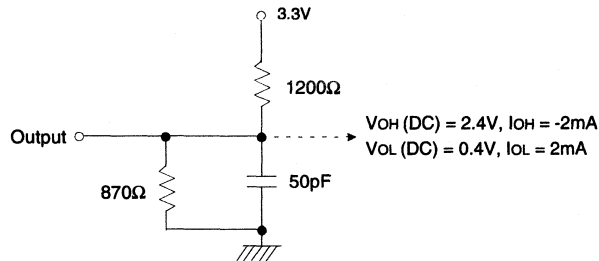
2. Refresh period is 64ms.

3. Measured with 1 PLL & 3 Drive ICs.

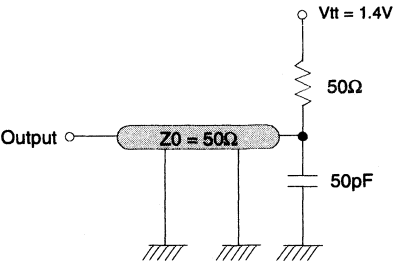
4. Unless otherwise noticed, Input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	tRRD(min)	15	ns	1
RAS to CAS delay	tRCD(min)	20	ns	1
Row precharge time	tRP(min)	20	ns	1
Row active time	tRAS(min)	45	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	65	ns	1
Last data in to row precharge	tRDL(min)	2	CLK	2
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns		
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :
- 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 - 2. Minimum delay is required to complete write.
 - 3. All parts allow every cycle column address change.
 - 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	tsAC	-	5.4	ns	1,2
Output data hold time	CAS latency=3	toH	2.7	-	ns	1,2
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	1

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A12,A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X		3	
			H	X	X	X	3						
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H	4,5		
Write & Column Address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0~A9, A11)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Exit	L	H	X	X	X	X	X	X			
					X	X	X	X					
		Entry	H	L	H	X	X	X	X				
					L	H	H	H					
DQM		Exit	L	H	H	X	X	X	X	X			
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

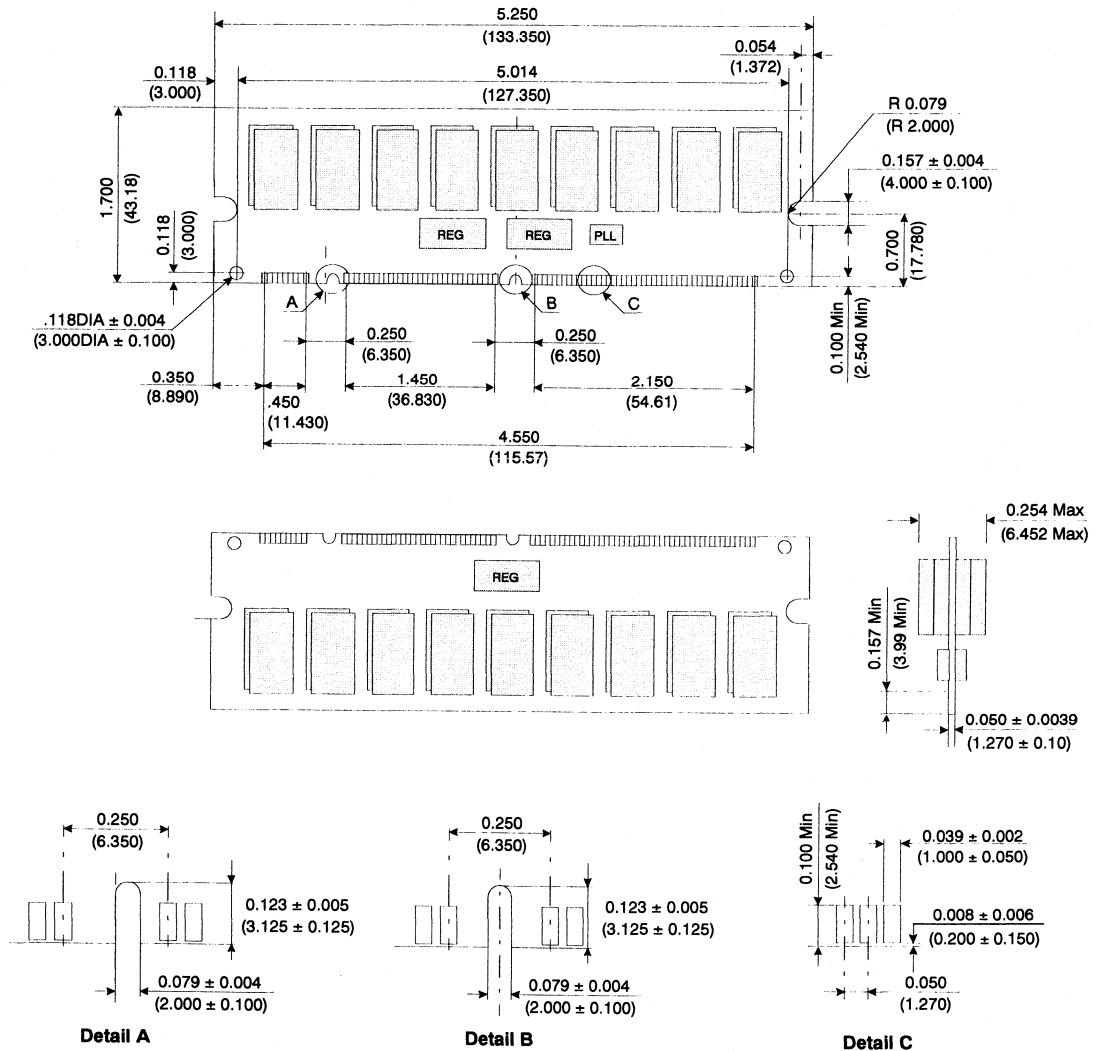
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)

Tolerances : ± 0.005 (.13) unless otherwise specified

The used device is stacked 128Mx4 SDRAM
 SDRAM Part No. : K4S510632A-TC75

This module is based on JEDEC PC133 Specification

SERIAL PRESENCE DETECT

PC133 Registered DIMM

M390S2858AT1-C75

- Organization : 128MX72
- Composition : 128MX4 * 18ea
- Used component part # : K4S510632A-TC75
- # of banks in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 8K/64ms
- Contents :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	11	0Bh	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	7.8us, support self refresh	82h	
13	Primary SDRAM width	x4	04h	
14	Error checking SDRAM width	x4	04h	
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 512MB	80h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC 2	02h	
63	Checksum for bytes 0 ~ 62	-	2Bh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	9	39h	
77	 Manufacturer part # (Data bits)	0	30h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	2	32h	
80	 Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5	35h	
82	Manufacturer part # (Composition component)	8	38h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	1	31h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	1	31h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	100MHz	64h	
127	Reserved	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	Undefined	-	5

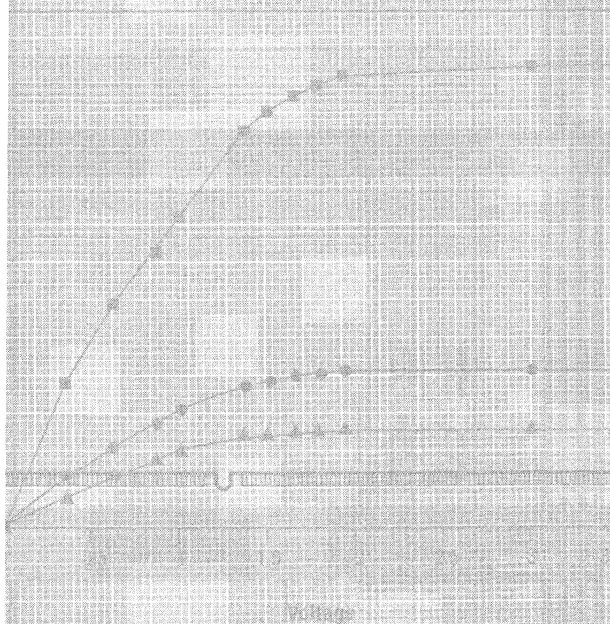
- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.

Module Specification

3

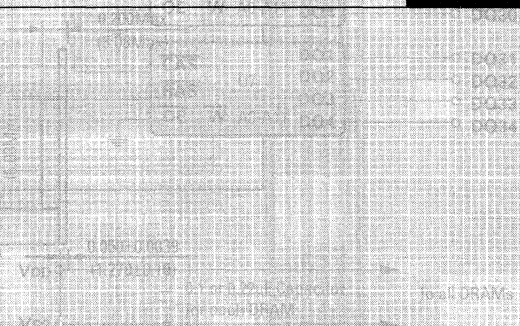
66MHz and 100MHz FULL RAS

(front view)



(Back view)

PC133 Unbuffered DIMM



M366S1723ATS SDRAM DIMM

16Mx64 SDRAM DIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1723ATS is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1723ATS consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S1723ATS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S1723ATS-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

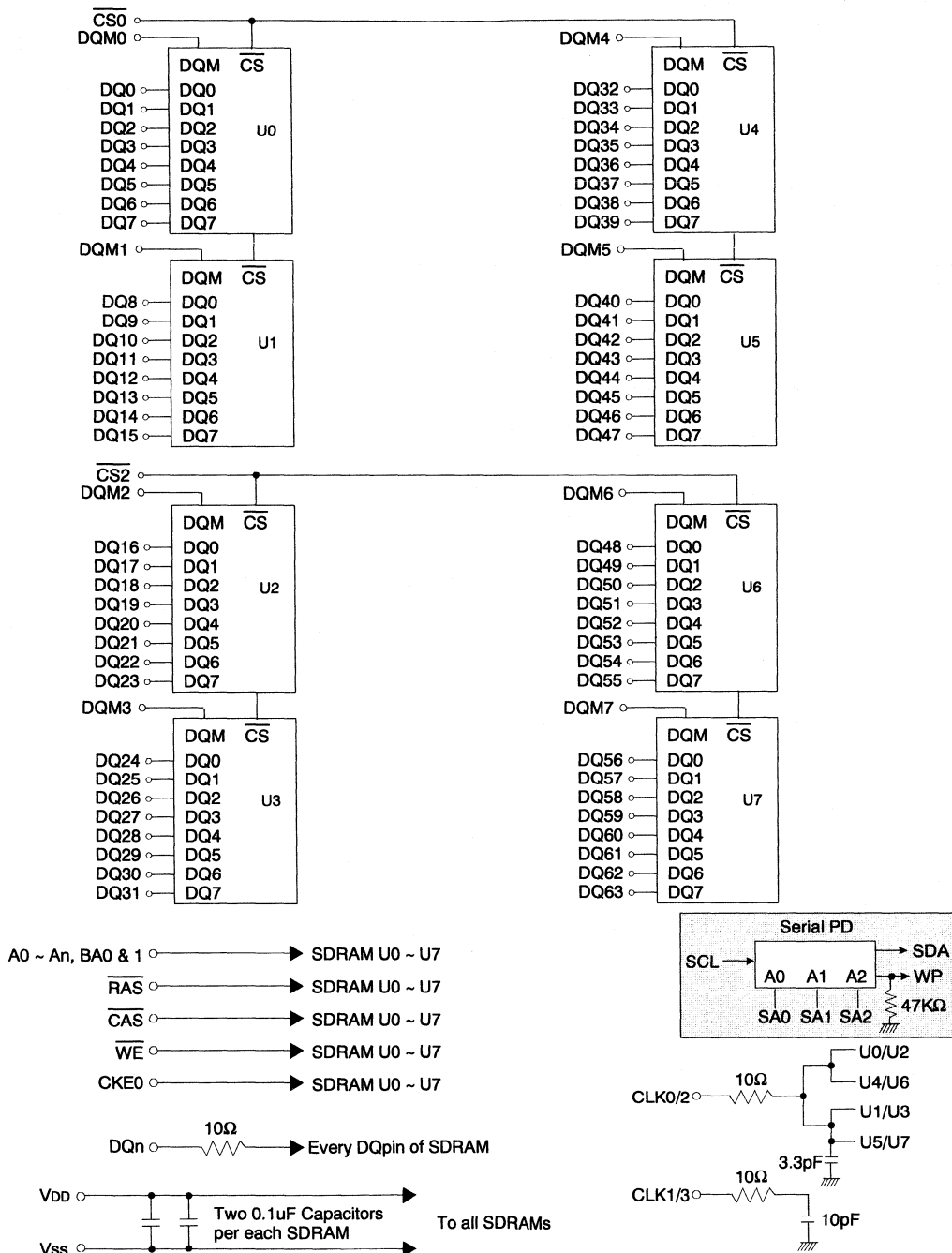
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{CS}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	30	45	pF
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	C _{IN}	30	45	pF
CKE (CKE0)	C _{CKE}	30	45	pF
Clock (CLK0, CLK2)	C _{CLK}	22	30	pF
CS (CS0, CS2)	C _{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	6	8	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	6	8	pF

DC CHARACTERISTICS(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\text{min})$ $I_O = 0 \text{ mA}$	960	mA	1
Precharge standby current in power-down mode	ICC2P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	8	mA	
	ICC2PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	8		
Precharge standby current in non power-down mode	ICC2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	160	mA	
	ICC2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	56		
Active standby current in power-down mode	ICC3P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	40	mA	
	ICC3PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	40		
Active standby current in non power-down mode (One bank active)	ICC3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	240	mA	
	ICC3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	160	mA	
Operating current (Burst mode)	ICC4	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	1,200	mA	1
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\text{min})$	1,760	mA	2
Self refresh current	ICC6	$\text{CKE} \leq 0.2\text{V}$	12	mA	

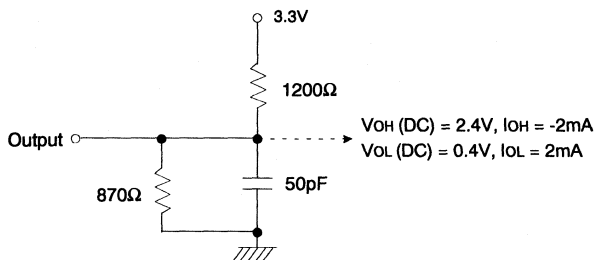
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

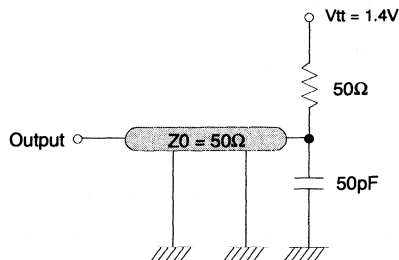
3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\text{min})$	15	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	$t_{RCD}(\text{min})$	20	ns	1
Row precharge time	$t_{RP}(\text{min})$	20	ns	1
Row active time	$t_{RAS}(\text{min})$	45	ns	1
	$t_{RAS}(\text{max})$	100	us	
Row cycle time	$t_{RC}(\text{min})$	65	ns	1
Last data in to row precharge	$t_{RDL}(\text{min})$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\text{min})$	2 CLK + 20 ns		
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\text{min})$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\text{min})$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tCC	7.5	1000	ns	1
CLK to valid	tsAC		5.4	ns	1,2
Output data	tOH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tSS	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tsLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	L		3									
		Exit	L	H	L	H	H	X	X		3		
											H	X	X
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

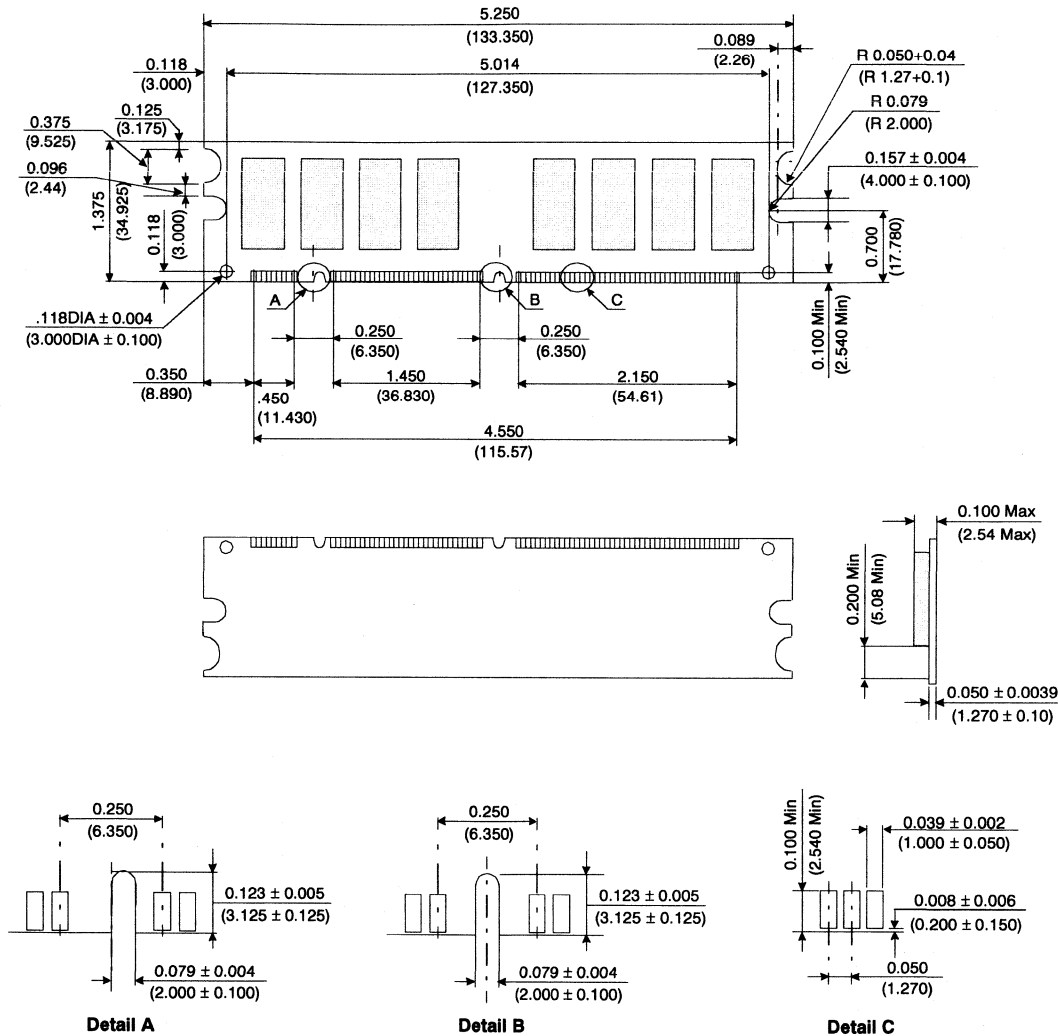
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC133 Unbuffered DIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832A-TC75

M366S1723ATS-C75

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832A-TC75
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	16ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 row of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT

PC133 Unbuffered DIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	9Dh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	S	53h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	S	53h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserverd	-	64h	6
127	Reserved	Detailed PC100 Information	ADh	6
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.
 6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M374S1723ATS SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S1723ATS is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S1723ATS consists of nine CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S1723ATS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S1723ATS-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	*CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	*SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	*SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

- * These pins are not used in this module.
 ** These pins should be NC in the system which does not support SPD.

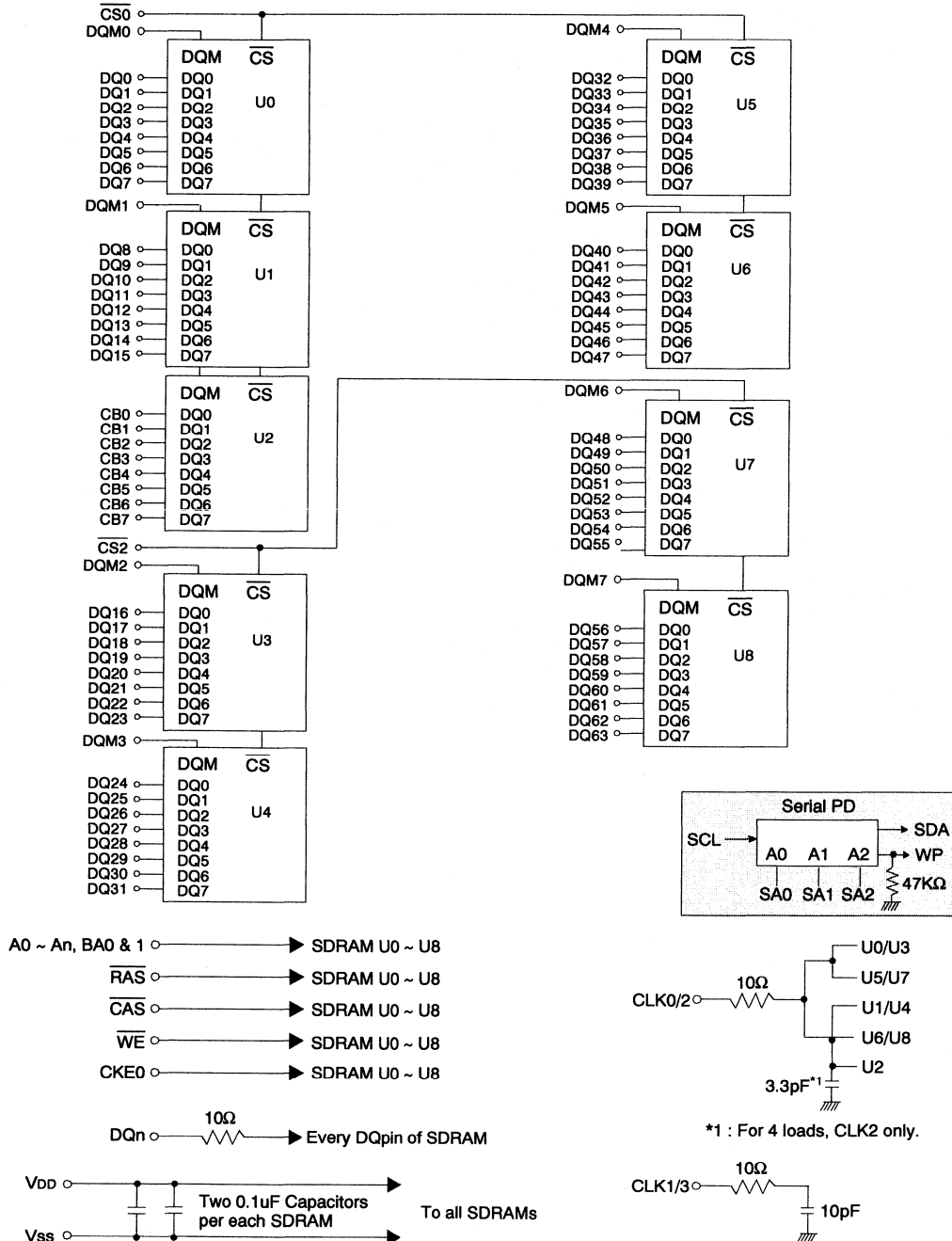
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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{LI}	-10	-	10	μA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	35	60	pF
RAS, CAS, WE	C _{IN}	35	60	pF
CKE (CKE0)	C _{CKE}	35	45	pF
Clock (CLK0, CLK2)	C _{CLK}	25	30	pF
CS (CS0, CS2)	C _{CS}	20	30	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	9	15	pF
DQ (DQ0 ~ DQ63)	C _{OUT1}	6	8	pF
CB (CB0 ~ CB7)	C _{OUT2}	6	8	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note ey15 04
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $\text{trc} \geq \text{trc}(\text{min})$ $I_o = 0 \text{ mA}$	1080	mA	1
Precharge standby current in power-down mode	ICC2P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	9	mA	
	ICC2PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	9		
Precharge standby current in non power-down mode	ICC2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	180	mA	
	ICC2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	63		
Active standby current in power-down mode	ICC3P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	45	mA	
	ICC3PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	45		
Active standby current in non power-down mode (One bank active)	ICC3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	270	mA	
	ICC3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	180	mA	
Operating current (Burst mode)	ICC4	$I_o = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	1,350	mA	1
Refresh current	ICC5	$\text{trc} \geq \text{trc}(\text{min})$	1,980	mA	2
Self refresh current	ICC6	$\text{CKE} \leq 0.2\text{V}$	9	mA	

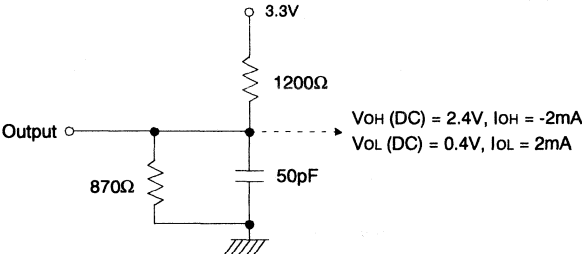
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

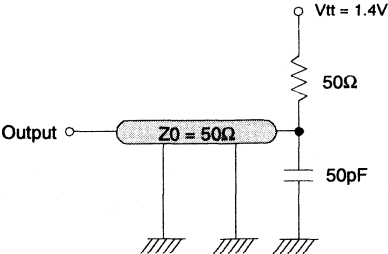
3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (V _{Ih} /V _{Il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	t _{RRD} (min)	15	ns	1
RAS to CAS delay	t _{RCD} (min)	20	ns	1
Row precharge time	t _{RP} (min)	20	ns	1
Row active time	t _{RAS} (min)	45	ns	1
	t _{RAS} (max)	100	us	
Row cycle time	t _{RC} (min)	65	ns	1
Last data in to row precharge	t _{RDL} (min)	2	CLK	2
Last data in to Active delay	t _{DAL} (min)	2 CLK + 20 ns		
Last data in to new col. address delay	t _{CDL} (min)	1	CLK	2
Last data in to burst stop	t _{BDL} (min)	1	CLK	2
Col. address to col. address delay	t _{CCD} (min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	- 75		Unit	Note
		Min	Max		
CLK cycle time	tCC	7.5	1000	ns	1
CLK to valid	tSAC		5.4	ns	1, 2
Output data	tOH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tSS	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tSLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	H	X	X			3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable									H	4,5		
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC133 Unbuffered DIMM

Units : Inches (Millimeters)



M374S1723ATS-C75

- Organization : 16Mx72
- Composition : 16Mx8 *9
- Used component part # : K4S280832B-TC75
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT

PC133 Unbuffered DIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	AFh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	7	37h	
77	 Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	S	53h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	S	53h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserverd	-	64h	6
127	Reserved	Detailed PC100 Information	ADh	6
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.
 6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M366S3323AT0 SDRAM DIMM

32Mx64 SDRAM DIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S3323AT0 is a 32M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S3323AT0 consists of sixteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S3323AT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S3323AT0-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

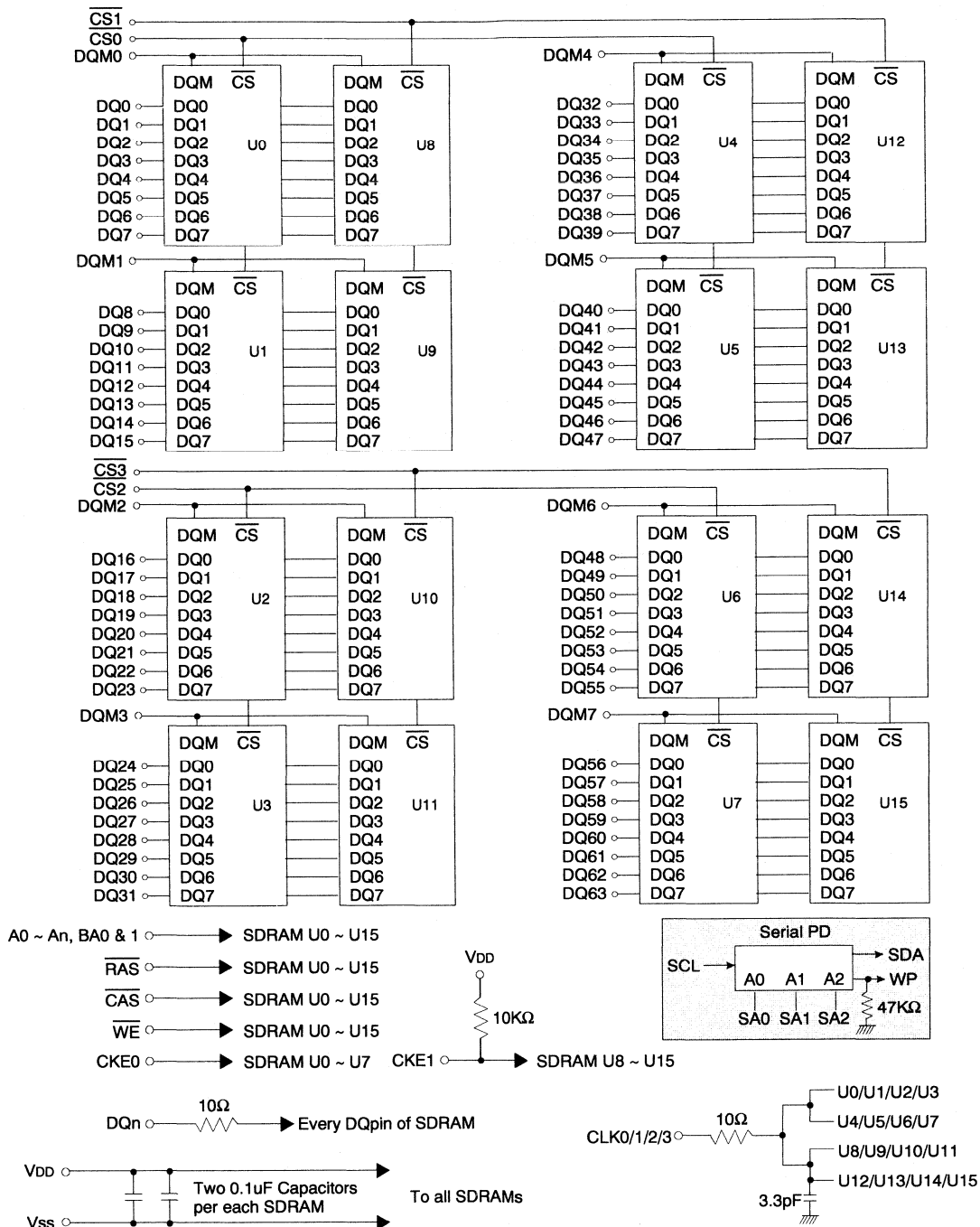
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
WP	Write protection	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	16	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	70	95	pF
RAS, CAS, WE	C _{IN}	70	95	pF
CKE (CKE0 ~ CKE1)	C _{CKE}	45	55	pF
Clock (CLK0 ~ CLK3)	C _{CLK}	35	40	pF
CS (CS0, CS2)	C _{CS}	25	30	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	15	20	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	10	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (one Bank Active)	Icc1	Burst length = 1 $\text{trc} \geq \text{trc}(\text{min})$ $I_o = 0 \text{ mA}$	1,200	mA	1
Precharge standby current in power-down mode	Icc2P	$\text{CKE} \leq V_{IL}(\text{max})$, $\text{tcc} = 10\text{ns}$	16	mA	
	Icc2PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$	16		
Precharge standby current in non power-down mode	Icc2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $\text{tcc} = 10\text{ns}$ Input signals are changed one time during 20ns	320	mA	
	Icc2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable	112		
Active standby current in power-down mode	Icc3P	$\text{CKE} \leq V_{IL}(\text{max})$, $\text{tcc} = 10\text{ns}$	80	mA	
	Icc3PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$	80		
Active standby current in non power-down mode (One bank active)	Icc3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $\text{tcc} = 10\text{ns}$ Input signals are changed one time during 20ns	480	mA	
	Icc3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable	320	mA	
Operating current (Burst mode)	Icc4	$I_o = 0 \text{ mA}$ Page burst 4Banks activated $\text{tCCD} = 2\text{CLKs}$	1,440	mA	1
Refresh current	Icc5	$\text{trc} \geq \text{trc}(\text{min})$	2,000	mA	2
Self refresh current	Icc6	$\text{CKE} \leq 0.2\text{V}$	24	mA	

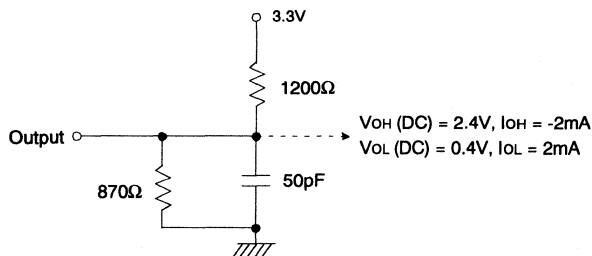
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

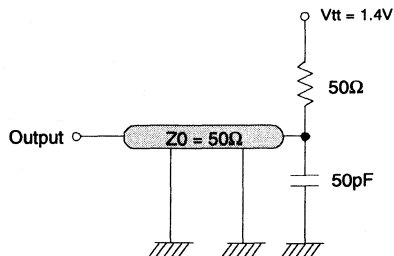
3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\min)$	15	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	ns	1
Row active time	$t_{RAS}(\min)$	45	ns	1
	$t_{RAS}(\max)$	100	us	
Row cycle time	$t_{RC}(\min)$	65	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20 ns		
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tcc	7.5	1000	ns	1
CLK to valid	tsAC		5.4	ns	1,2
Output data	toH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tss	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tsLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	X	X		3		
											H	X	X
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

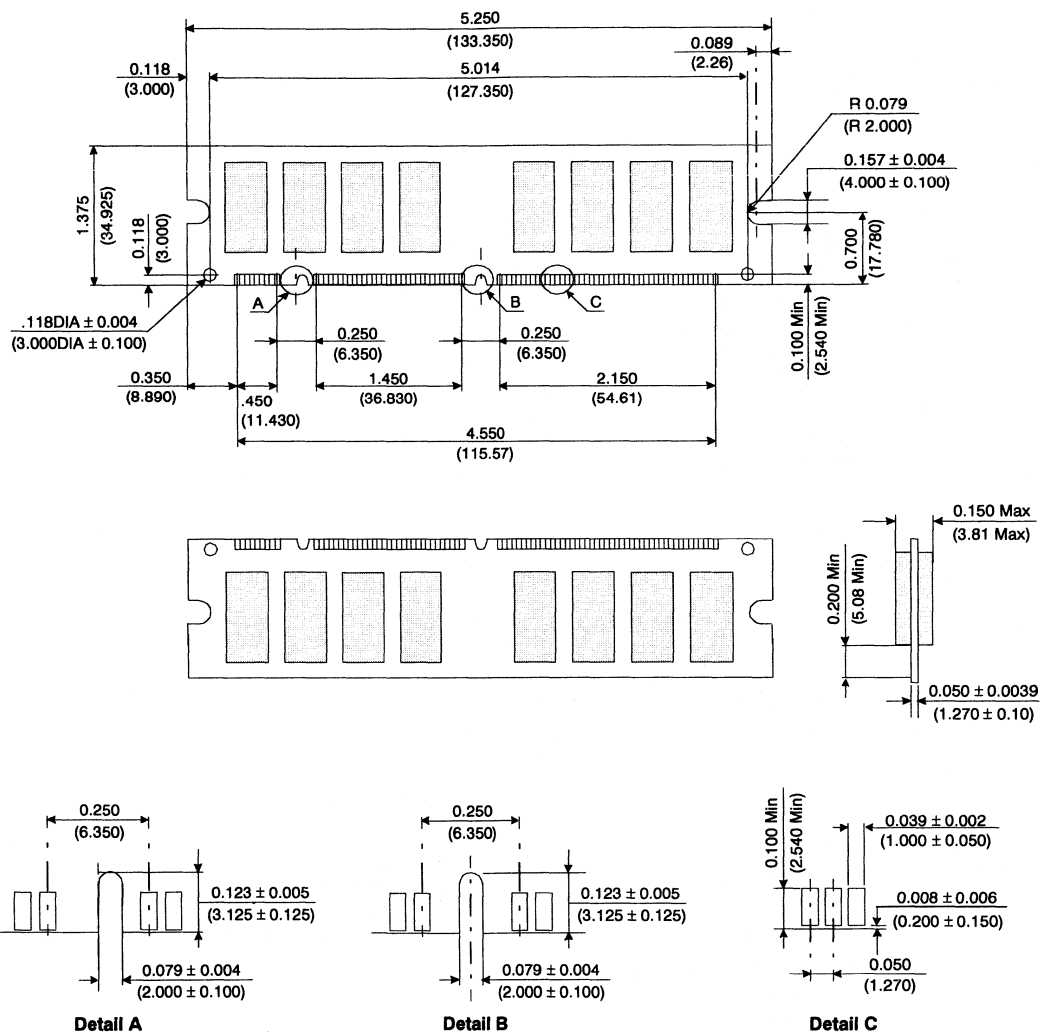
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832A-TC75

M366S3323AT0-C75

- Organization : 32Mx64
- Composition : 16Mx8 *16
- Used component part # : K4S280832A-TC75
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module ROWS on this assembly	2 rows	02h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock@CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock@CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	2 rows of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT

PC133 Unbuffered DIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	9Eh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	 Manufacturer part # (Module depth)	3	33h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	FDh	6
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.
 6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M374S3323AT0 SDRAM DIMM

32Mx72 SDRAM DIMM with ECC based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S3323AT0 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S3323AT0 consists of eighteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S3323AT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S3323AT0-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	*SA0
26	Vdd	54	Vss	82	*SDA	110	Vdd	138	Vss	166	*SA1
27	WE	55	DQ16	83	*SCL	111	CAS	139	DQ48	167	*SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

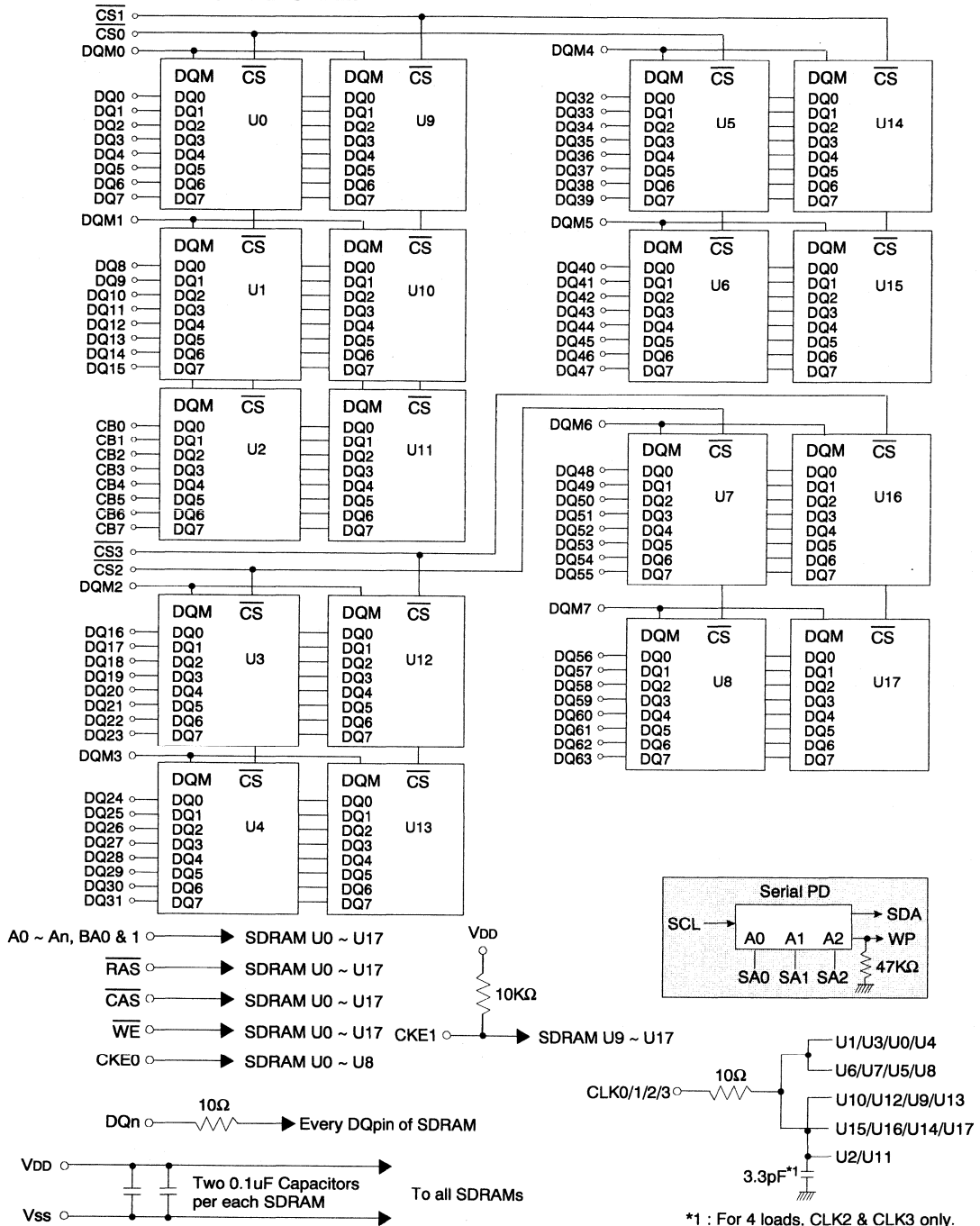
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ VDDQ.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	CADD	75	100	pF
RAS, CAS, WE	CIN	75	100	pF
CKE (CKE0)	CCKE	50	60	pF
Clock (CLK0, CLK2)	CCLK	35	40	pF
CS (CS0, CS2)	Ccs	30	35	pF
DQM (DQM0 ~ DQM7)	CDQM	20	25	pF
DQ (DQ0 ~ DQ63)	COU1	10	15	pF
CB (CB0 ~ CB7)	COU2	10	15	pF

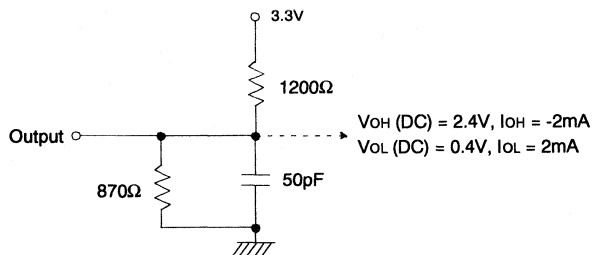
DC CHARACTERISTICS(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	Icc1	Burst length = 1 $t_{RC} \geq t_{RC}(\text{min})$ $I_O = 0 \text{ mA}$	1,350	mA	1
Precharge standby current in power-down mode	Icc2P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	18	mA	
	Icc2PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	18		
Precharge standby current in non power-down mode	Icc2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	360	mA	
	Icc2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	126		
Active standby current in power-down mode	Icc3P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	90	mA	
	Icc3PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	90		
Active standby current in non power-down mode (One bank active)	Icc3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	540	mA	
	Icc3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	360	mA	
Operating current (Burst mode)	Icc4	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	1,620	mA	1
Refresh current	Icc5	$t_{RC} \geq t_{RC}(\text{min})$	2,250	mA	2
Self refresh current	Icc6	$\text{CKE} \leq 0.2\text{V}$	27	mA	

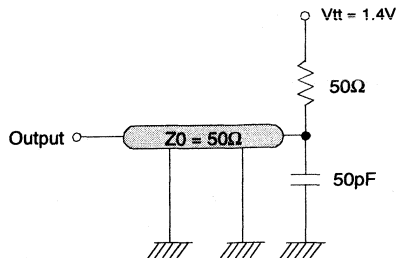
- Notes :**
1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\text{min})$	15	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	$t_{RCD}(\text{min})$	20	ns	1
Row precharge time	$t_{RP}(\text{min})$	20	ns	1
Row active time	$t_{RAS}(\text{min})$	45	ns	1
	$t_{RAS}(\text{max})$	100	us	
Row cycle time	$t_{RC}(\text{min})$	65	ns	1
Last data in to row precharge	$t_{RDL}(\text{min})$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\text{min})$	2 CLK + 20 ns		
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\text{min})$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\text{min})$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tcc	7.5	1000	ns	1
CLK to valid	tsAC		5.4	ns	1,2
Output data	toH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tss	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tsLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note										
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2										
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3										
	Self refresh	Entry		L									H	L	H	H	X	X	X	X	3		
		Exit	L		H	L	H	H	X	X	X	X									X	X	3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address												
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4										
	Auto precharge enable										H		4,5										
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4										
	Auto precharge enable										H		4,5										
Burst stop			H	X	L	H	H	L	X	X			6										
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X											
	All banks									X	H												
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X													
					L	V	V	V															
Precharge power down mode		Entry	H	L	H	X	X	X	X	X													
					L	H	H	H															
		Exit	L	H	H	X	X	X	X														
					L	V	V	V															
DQM			H	X					V	X			7										
No operation command			H	X	H	X	X	X	X	X													
					L	H	H	H															

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

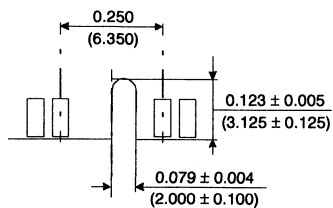
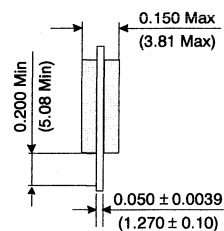
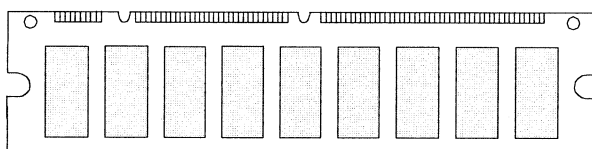
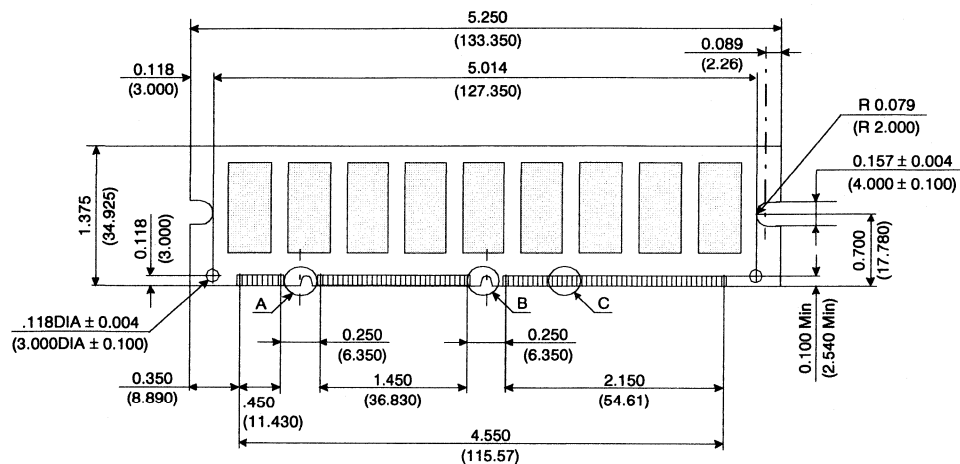
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

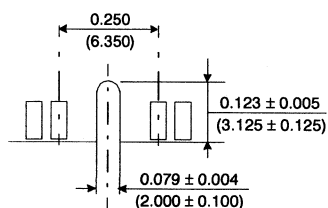
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

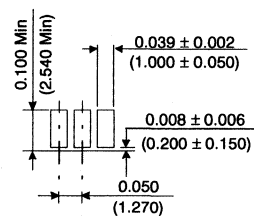
Units : Inches (Millimeters)



Detail A



Detail B



Detail C

Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832A-TC75

M374S3323AT0-C75

- Organization : 32Mx72
- Composition : 16Mx8 *18
- Used component part # : K4S280832A-TC75
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module rows on this assembly	2 rows	02h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock@CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock@CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	2 rows of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT

PC133 Unbuffered DIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	B0h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	7	37h	
77	 Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	 Manufacturer part # (Module depth)	3	33h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	FDh	6
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsungs own purpose.
 6. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

M366S1723BTS SDRAM DIMM

16Mx64 SDRAM DIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S1723BTS is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S1723BTS consists of eight CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S1723BTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S1723BTS-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm 0.3V$ power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*VREF	90	Vdd	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	*CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	Vdd	77	DQ31	105	*CB4	133	Vdd	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

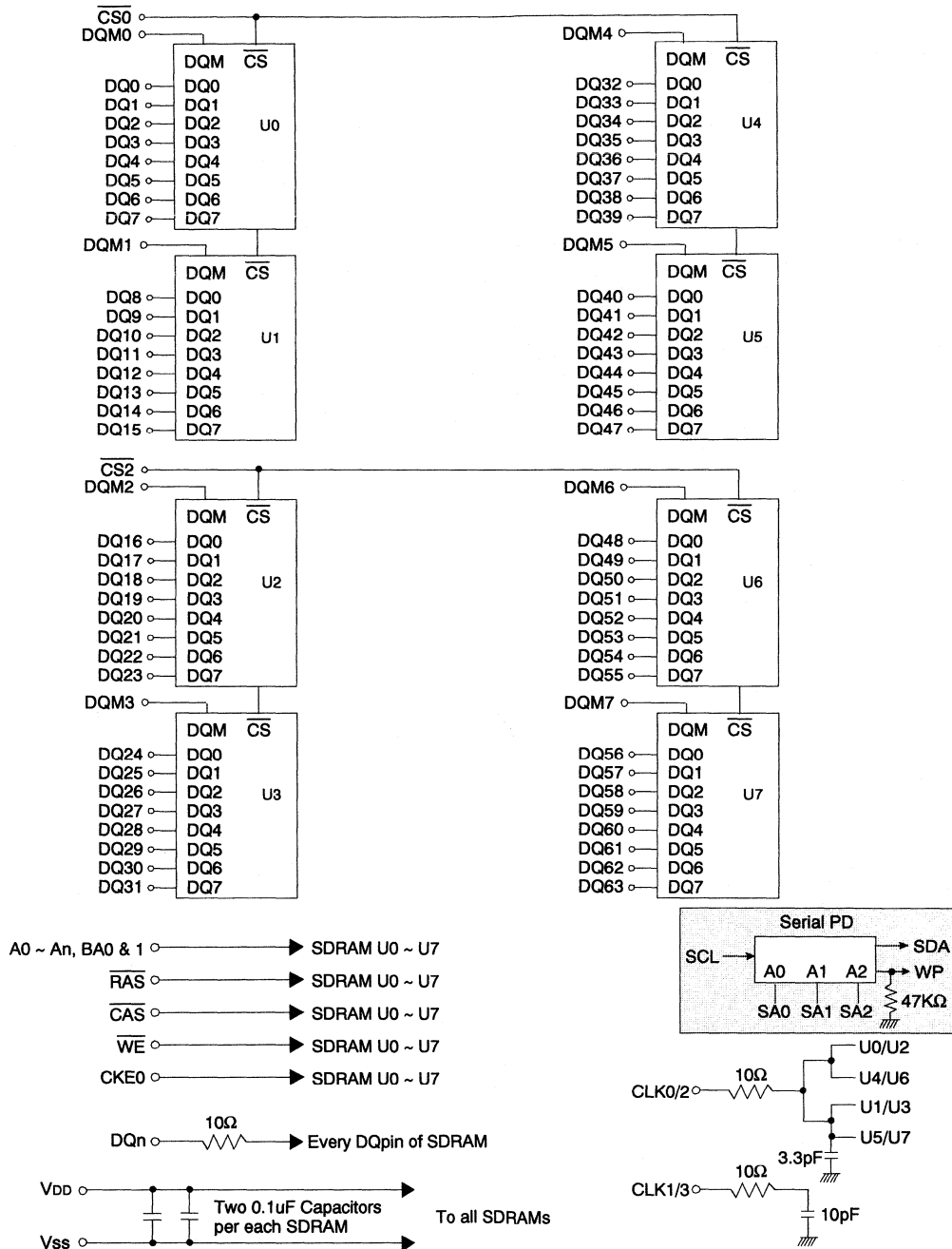
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	30	45	pF
RAS, CAS, WE	C _{IN}	30	45	pF
CKE (CKE0)	C _{CKE}	30	45	pF
Clock (CLK0, CLK2)	C _{CLK}	22	30	pF
CS (CS0, CS2)	C _{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	6	8	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	6	8	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $trc \geq trc(min)$ $I_o = 0$ mA	960	mA	1
Precharge standby current in power-down mode	I_{CC2P}	$CKE \leq V_{IL}(max)$, $t_{CC} = 10ns$	8	mA	
	I_{CC2PS}	$CKE \& CLK \leq V_{IL}(max)$, $t_{CC} = \infty$	8		
Precharge standby current in non power-down mode	I_{CC2N}	$CKE \geq V_{IH}(min)$, $\overline{CS} \geq V_{IH}(min)$, $t_{CC} = 10ns$ Input signals are changed one time during 20ns	160	mA	
	I_{CC2NS}	$CKE \geq V_{IH}(min)$, $CLK \leq V_{IL}(max)$, $t_{CC} = \infty$ Input signals are stable	56		
Active standby current in power-down mode	I_{CC3P}	$CKE \leq V_{IL}(max)$, $t_{CC} = 10ns$	40	mA	
	I_{CC3PS}	$CKE \& CLK \leq V_{IL}(max)$, $t_{CC} = \infty$	40		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	$CKE \geq V_{IH}(min)$, $\overline{CS} \geq V_{IH}(min)$, $t_{CC} = 10ns$ Input signals are changed one time during 20ns	240	mA	
	I_{CC3NS}	$CKE \geq V_{IH}(min)$, $CLK \leq V_{IL}(max)$, $t_{CC} = \infty$ Input signals are stable	160	mA	
Operating current (Burst mode)	I_{CC4}	$I_o = 0$ mA Page burst 4Banks activated $t_{CCD} = 2CLKs$	1,200	mA	1
Refresh current	I_{CC5}	$trc \geq trc(min)$	1,760	mA	2
Self refresh current	I_{CC6}	$CKE \leq 0.2V$	12	mA	

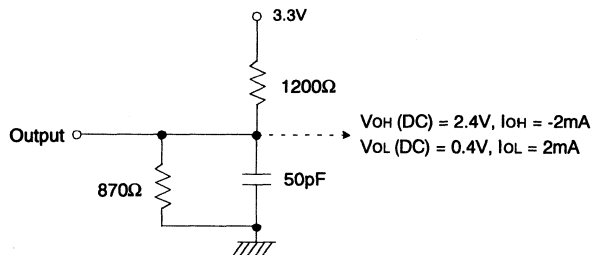
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

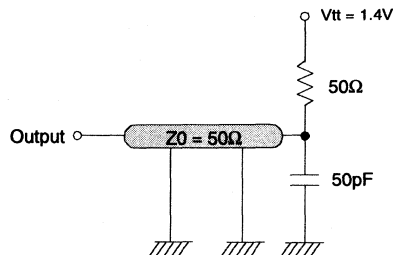
3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\text{min})$	15	ns	1
RAS to CAS delay	$t_{RCD}(\text{min})$	20	ns	1
Row precharge time	$t_{RP}(\text{min})$	20	ns	1
Row active time	$t_{RAS}(\text{min})$	45	ns	1
	$t_{RAS}(\text{max})$	100	us	
Row cycle time	$t_{RC}(\text{min})$	65	ns	1
Last data in to row precharge	$t_{RDL}(\text{min})$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\text{min})$	2 CLK + 20 ns		
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\text{min})$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\text{min})$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tcc	7.5	1000	ns	1
CLK to valid	tsAC		5.4	ns	1,2
Output data	tOH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tss	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tsLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3	
	Self refresh		Entry	L	H	H	H	X	X			3	
		Exit	L	H	X	X	X					3	
				H	X	X	X						
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable									H		4,5	
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable									H		4,5	
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X		
	All banks								X	H			
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC133 Unbuffered DIMM

Units : Inches (Millimeters)



917

M366S1723BTS-C75

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832B-TC75
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module ROWs on this assembly	1 row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	16ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 row of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT

PC133 Unbuffered DIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	9Dh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, #of banks In Comp. & Interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	S	53h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	S	53h	
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	ADh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The row select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsung's own purpose.

6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M374S1723BTS SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S1723BTS is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S1723BTS consists of nine CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S1723BTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S1723BTS-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

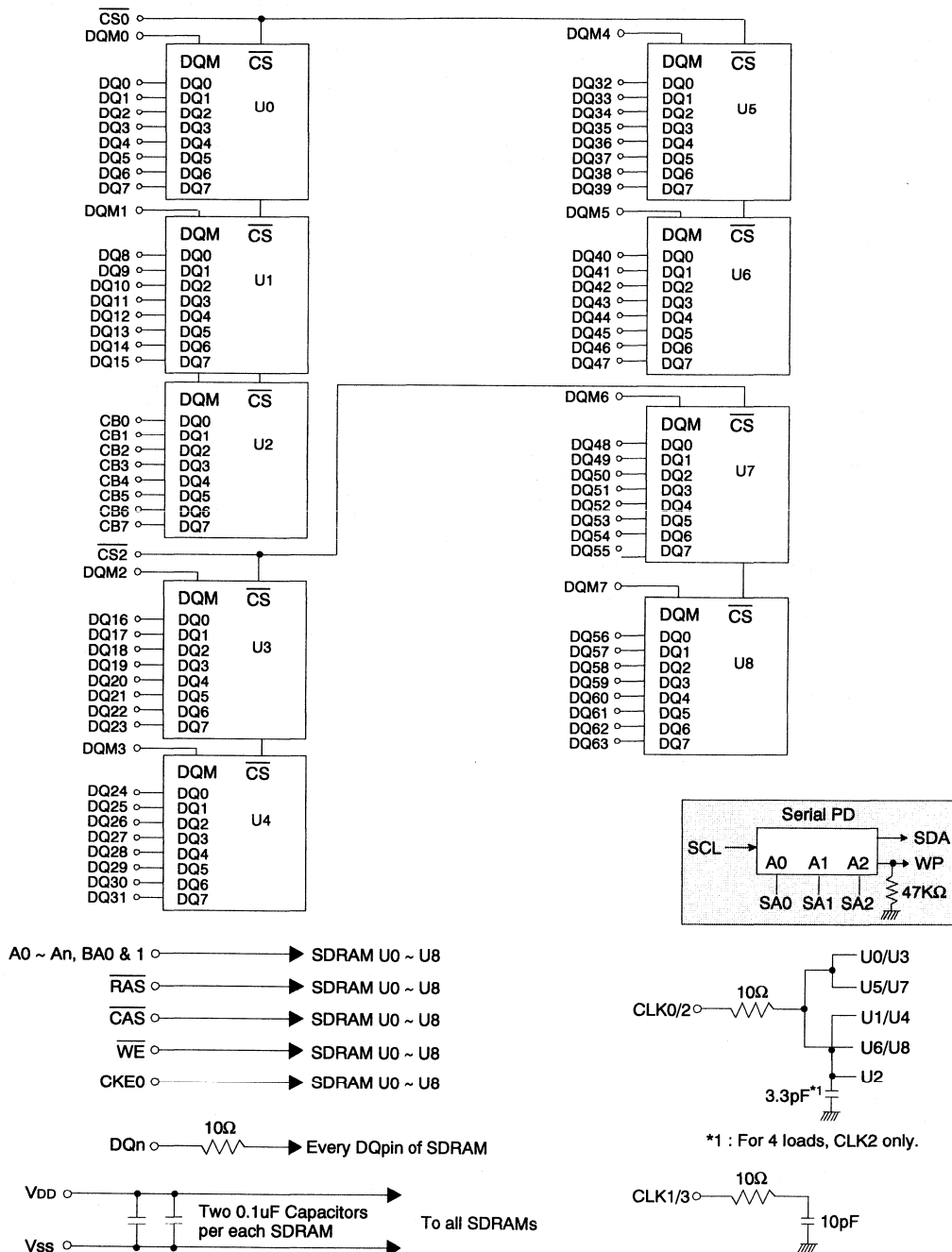
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	35	60	pF
RAS, CAS, WE	C _{IN}	35	60	pF
CKE (CKE0)	C _{CKE}	35	45	pF
Clock (CLK0, CLK2)	C _{CLK}	25	30	pF
CS (CS0, CS2)	C _{CS}	20	30	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	9	15	pF
DQ (DQ0 ~ DQ63)	C _{OUT1}	6	8	pF
CB (CB0 ~ CB7)	C _{OUT2}	6	8	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note ey15 04
			-75		
Operating current (One bank active)	I _{CC1}	Burst length = 1 trc ≥ trc(min) Io = 0 mA	1080	mA	1
Precharge standby current in power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), tcc = 10ns	9	mA	
	I _{CC2PS}	CKE & CLK ≤ V _{IL} (max), tcc = ∞	9		
Precharge standby current in non power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(\min)$, tcc = 10ns Input signals are changed one time during 20ns	180	mA	
	I _{CC2NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), tcc = ∞ Input signals are stable	63		
Active standby current in power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), tcc = 10ns	45	mA	
	I _{CC3PS}	CKE & CLK ≤ V _{IL} (max), tcc = ∞	45		
Active standby current in non power-down mode (One bank active)	I _{CC3N}	CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(\min)$, tcc = 10ns Input signals are changed one time during 20ns	270	mA	
	I _{CC3NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), tcc = ∞ Input signals are stable	180	mA	
Operating current (Burst mode)	I _{CC4}	Io = 0 mA Page burst 4Banks activated tccd = 2CLKs	1,350	mA	1
Refresh current	I _{CC5}	trc ≥ trc(min)	1,980	mA	2
Self refresh current	I _{CC6}	CKE ≤ 0.2V	9	mA	

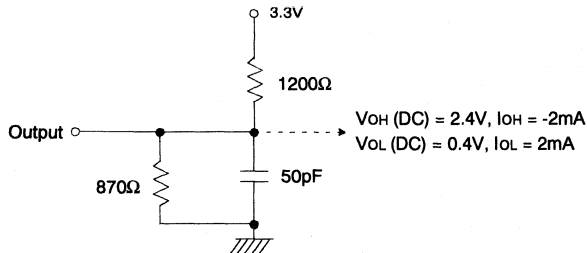
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

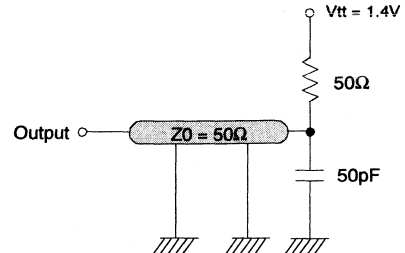
3. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\text{min})$	15	ns	1
RAS to CAS delay	$t_{RCD}(\text{min})$	20	ns	1
Row precharge time	$t_{RP}(\text{min})$	20	ns	1
Row active time	$t_{RAS}(\text{min})$	45	ns	1
	$t_{RAS}(\text{max})$	100	us	
Row cycle time	$t_{RC}(\text{min})$	65	ns	1
Last data in to row precharge	$t_{RDL}(\text{min})$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\text{min})$	2 CLK + 20 ns		
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\text{min})$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\text{min})$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	- 75		Unit	Note
		Min	Max		
CLK cycle time	tCC	7.5	1000	ns	1
CLK to valid	tSAC		5.4	ns	1, 2
Output data	tOH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tSS	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tSLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	X	X			3	
												H	X
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is Ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

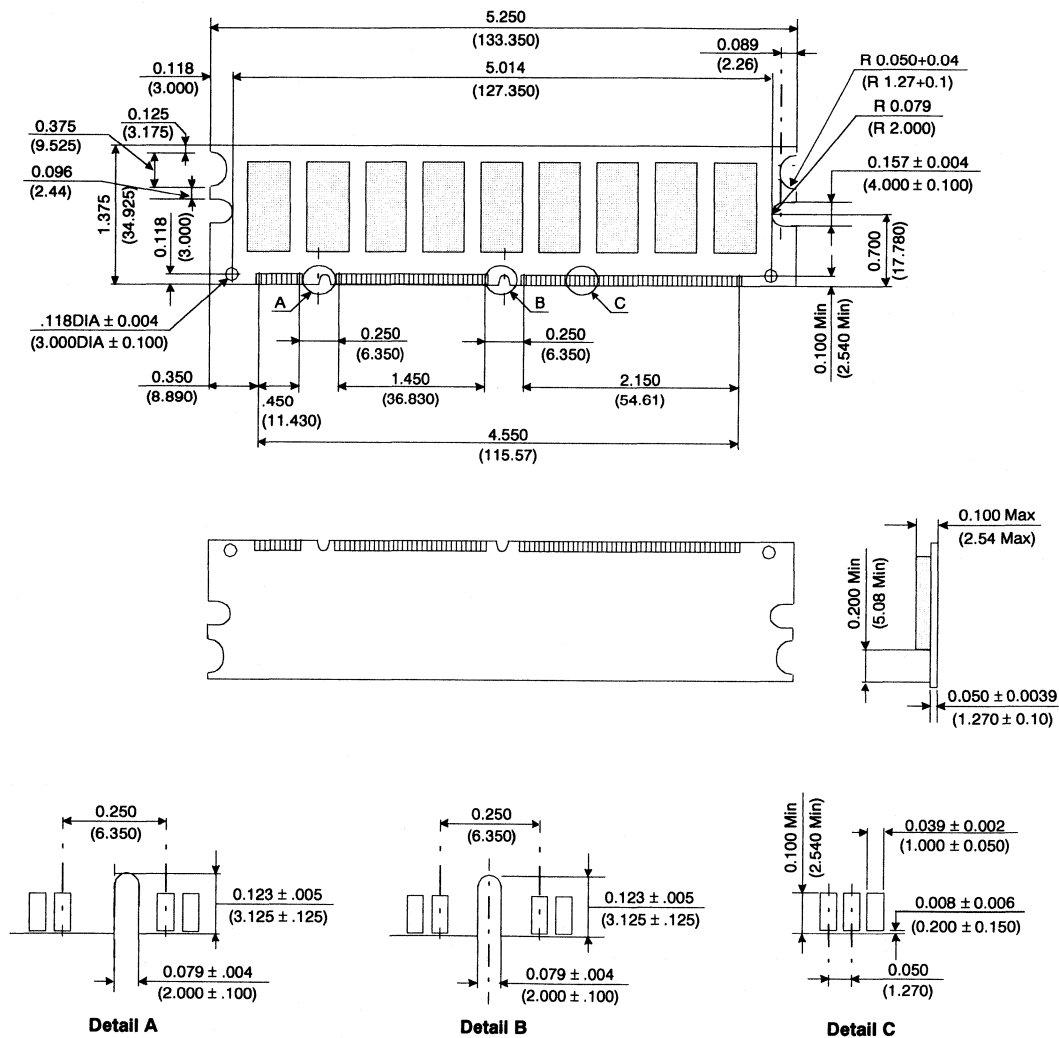
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832B-TC75

M374S1723BTS-C75

- Organization : 16Mx72
- Composition : 16Mx8 *9
- Used component part # : K4S280832B-TC75
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	AFh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	7	37h	
77	 Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	 Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	S	53h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	S	53h	
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserverd	-	64h	6
127	Reserved	Detailed PC100 Information	ADh	6
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsungs own purpose.
 6. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

M366S3323BT0 SDRAM DIMM

32Mx64 SDRAM DIMM based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S3323BT0 is a 32M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S3323BT0 consists of sixteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S3323BT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S3323BT0-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

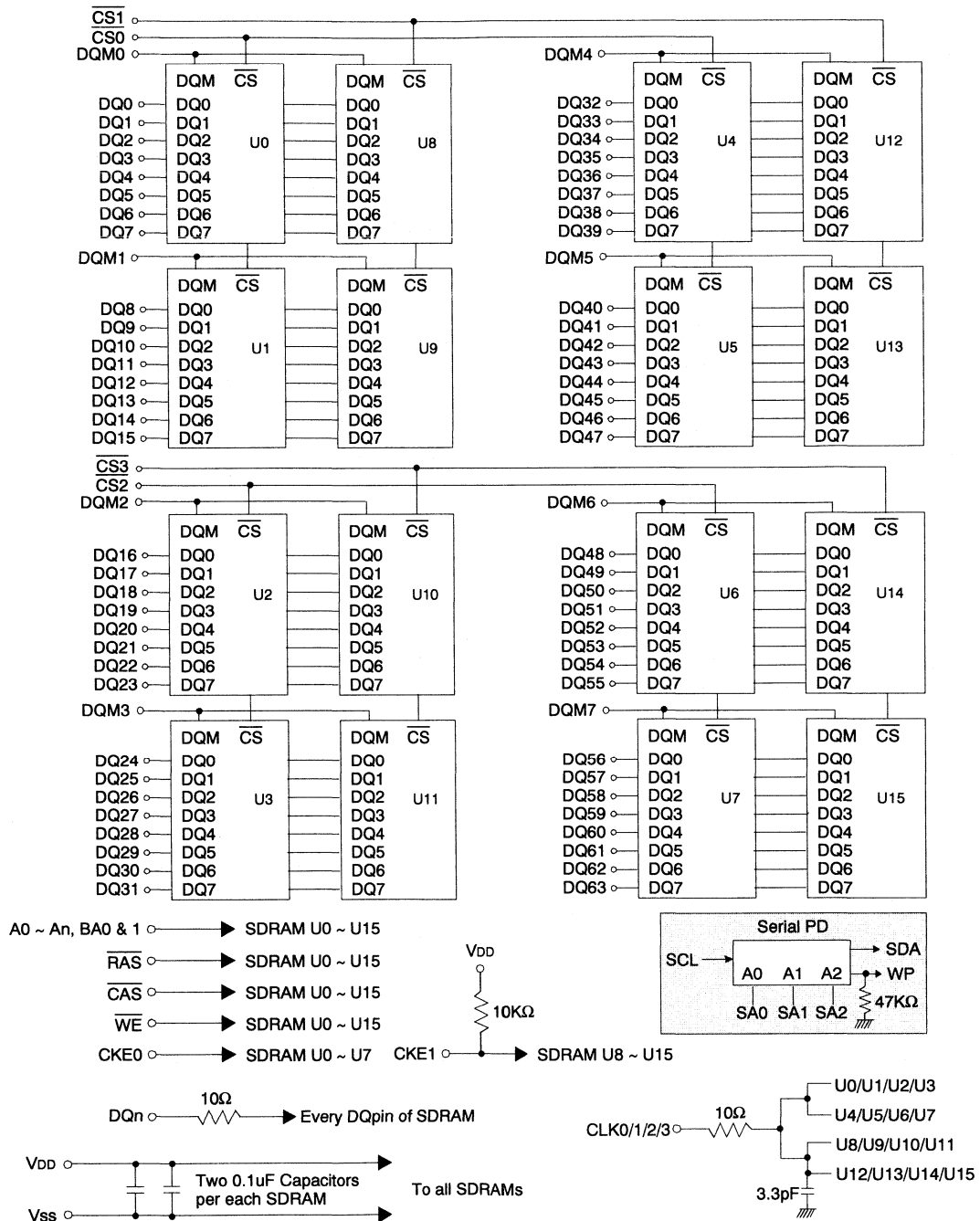
- * These pins are not used in this module.
- ** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	16	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	70	95	pF
RAS, CAS, WE	C _{IN}	70	95	pF
CKE (CKE0 ~ CKE1)	C _{CKE}	45	55	pF
Clock (CLK0 ~ CLK3)	C _{CLK}	35	40	pF
CS (CS0, CS2)	C _{CS}	25	30	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	15	20	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	10	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (one Bank Active)	I _{CC1}	Burst length = 1 $\text{trc} \geq \text{trc}(\text{min})$ $I_o = 0 \text{ mA}$	1,200	mA	1
Precharge standby current in power-down mode	I _{CC2P}	$\text{CKE} \leq V_{IL}(\text{max})$, $\text{tcc} = 10\text{ns}$	16	mA	
	I _{CC2PS}	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$	16		
Precharge standby current in non power-down mode	I _{CC2N}	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $\text{tcc} = 10\text{ns}$ Input signals are changed one time during 20ns	320	mA	
	I _{CC2NS}	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable	112		
Active standby current in power-down mode	I _{CC3P}	$\text{CKE} \leq V_{IL}(\text{max})$, $\text{tcc} = 10\text{ns}$	80	mA	
	I _{CC3PS}	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$	80		
Active standby current in non power-down mode (One bank active)	I _{CC3N}	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $\text{tcc} = 10\text{ns}$ Input signals are changed one time during 20ns	480	mA	
	I _{CC3NS}	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable	320	mA	
Operating current (Burst mode)	I _{CC4}	$I_o = 0 \text{ mA}$ Page burst 4Banks activated $\text{tCCD} = 2\text{CLKs}$	1,440	mA	1
Refresh current	I _{CC5}	$\text{trc} \geq \text{trc}(\text{min})$	2,000	mA	2
Self refresh current	I _{CC6}	$\text{CKE} \leq 0.2V$	24	mA	

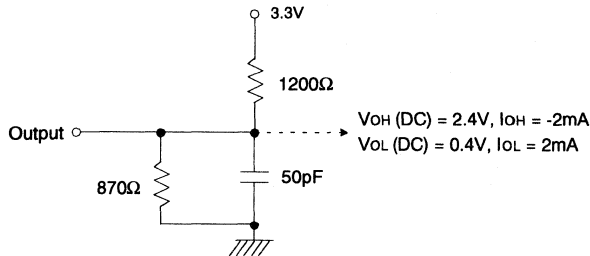
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

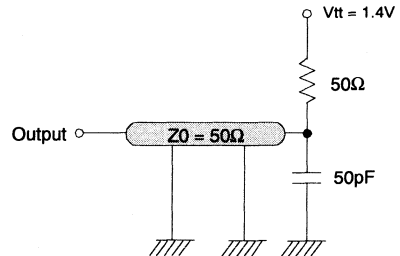
3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\min)$	15	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	ns	1
Row active time	$t_{RAS}(\min)$	45	ns	1
	$t_{RAS}(\max)$	100	us	
Row cycle time	$t_{RC}(\min)$	65	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20 ns		
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tcc	7.5	1000	ns	1
CLK to valid	tsAC		5.4	ns	1,2
Output data	toH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tss	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tsLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA _{0,1}	A ₁₀ /AP	A ₁₁ , A ₉ ~ A ₀	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L	L	L	L	H	X	X		3	
		Exit	L	H	L	H	H	H	X	X		3	
					H	X	X	X				3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A ₀ ~ A ₉)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A ₀ ~ A ₉)	4
	Auto precharge enable										H		4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

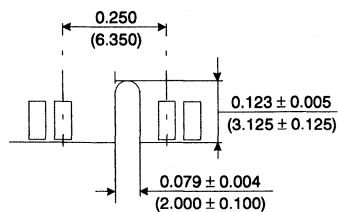
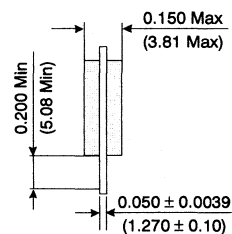
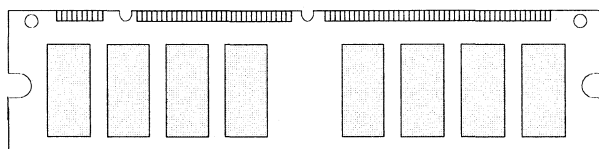
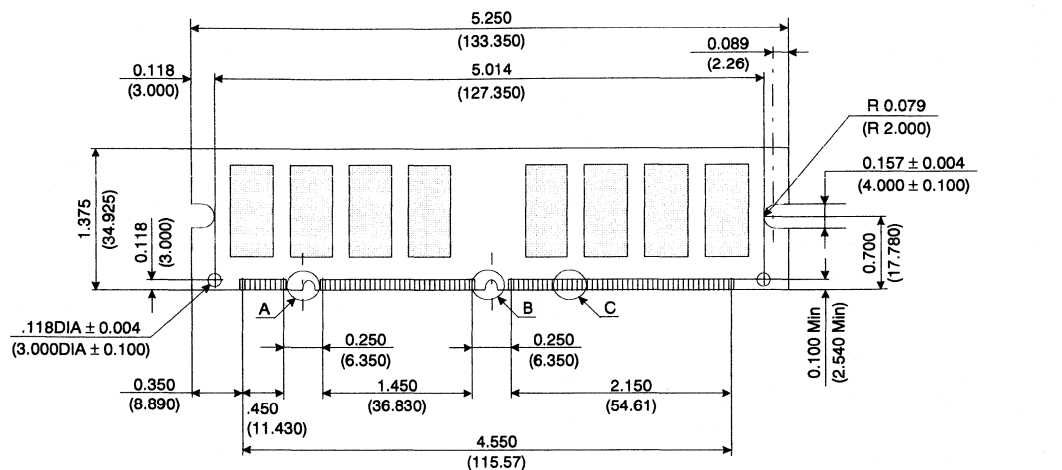
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

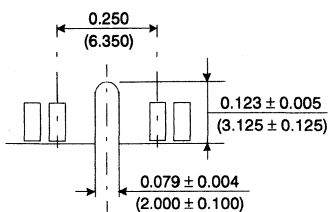
PC133 Unbuffered DIMM

PACKAGE DIMENSIONS

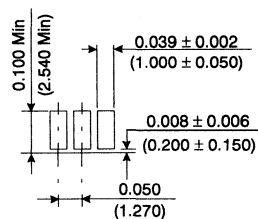
Units : Inches (Millimeters)



Detail A



Detail B



Detail C

Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832B-TC75

M366S3323BT0-C75

- Organization : 32Mx64
- Composition : 16Mx8 *16
- Used component part # : K4S280832B-TC75
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module rows on this assembly	2 rows	02h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock@CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock@CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	2 rows of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	9Eh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	 Manufacturer part # (Module depth)	3	33h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	FDh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The row select address is excluded in counting the total # of addresses.

2. This value is based on the component specification.

3. These bytes are programmed by code of Date Week & Date Year with BCD format.

4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.

5. These bytes are Undefined and can be used for Samsung's own purpose.

6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M374S3323BT0 SDRAM DIMM

32Mx72 SDRAM DIMM with ECC based on 16Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S3323BT0 is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S3323BT0 consists of eighteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S3323BT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S3323BT0-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

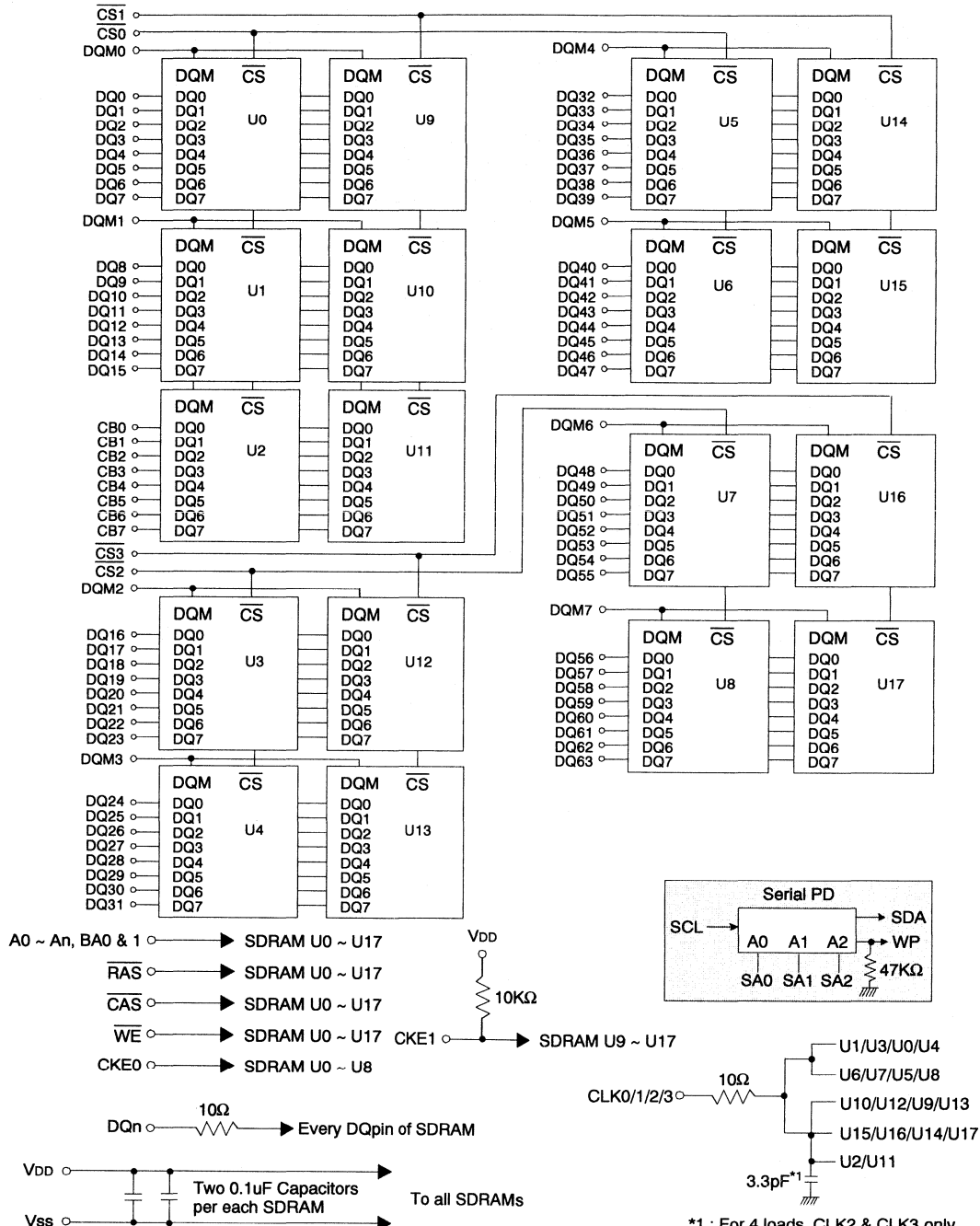
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	16	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	μA	3

Note : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C _{ADD}	70	95	pF
RAS, CAS, WE	C _{IN}	70	95	pF
CKE (CKE0 ~ CKE1)	C _{CKE}	45	55	pF
Clock (CLK0 ~ CLK3)	C _{CLK}	35	40	pF
CS (CS0, CS2)	C _{CS}	25	30	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	15	20	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	10	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $\text{trc} \geq \text{trc}(\text{min})$ $I_O = 0 \text{ mA}$	1,350	mA	1
Precharge standby current in power-down mode	ICC2P	$\text{CKE} \leq V_{IL}(\text{max})$, $\text{tcc} = 10\text{ns}$	18	mA	
	ICC2PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$	18		
Precharge standby current in non power-down mode	ICC2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $\text{tcc} = 10\text{ns}$ Input signals are changed one time during 20ns	360	mA	
	ICC2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable	126		
Active standby current in power-down mode	ICC3P	$\text{CKE} \leq V_{IL}(\text{max})$, $\text{tcc} = 10\text{ns}$	90	mA	
	ICC3PS	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$	90		
Active standby current in non power-down mode (One bank active)	ICC3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $\text{tcc} = 10\text{ns}$ Input signals are changed one time during 20ns	540	mA	
	ICC3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $\text{tcc} = \infty$ Input signals are stable	360	mA	
Operating current (Burst mode)	ICC4	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $\text{tCCD} = 2\text{CLKs}$	1,620	mA	1
Refresh current	ICC5	$\text{trc} \geq \text{trc}(\text{min})$	2,250	mA	2
Self refresh current	ICC6	$\text{CKE} \leq 0.2\text{V}$	27	mA	

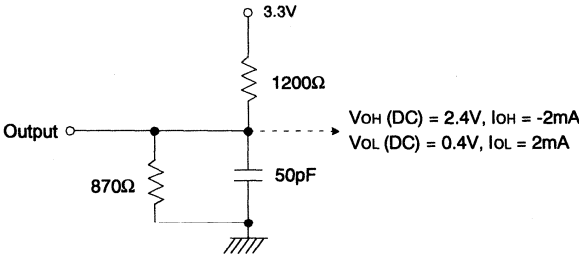
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

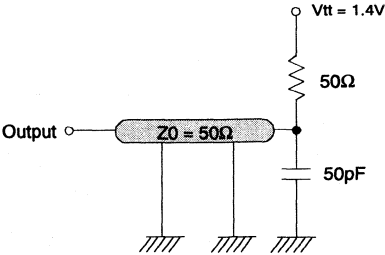
3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			-75		
Row active to row active delay		tRRD(min)	15	ns	1
RAS to CAS delay		tRCD(min)	20	ns	1
Row precharge time		tRP(min)	20	ns	1
Row active time		tRAS(min)	45	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	65	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2
Last data in to Active delay		tDAL(min)	2 CLK + 20 ns		
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	-		-		

- Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tcc	7.5	1000	ns	1
CLK to valid	tsac		5.4	ns	1,2
Output data	toH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tss	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tsLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2 - 0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2 - 1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

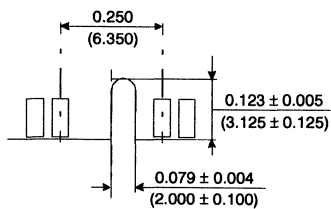
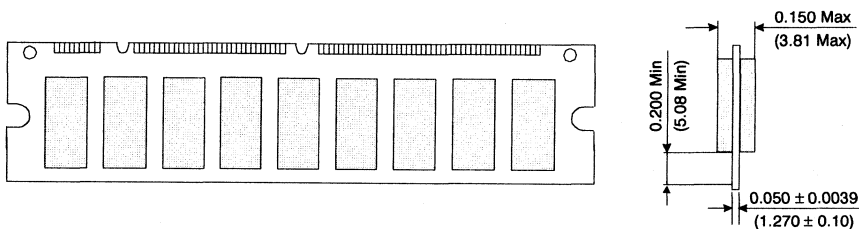
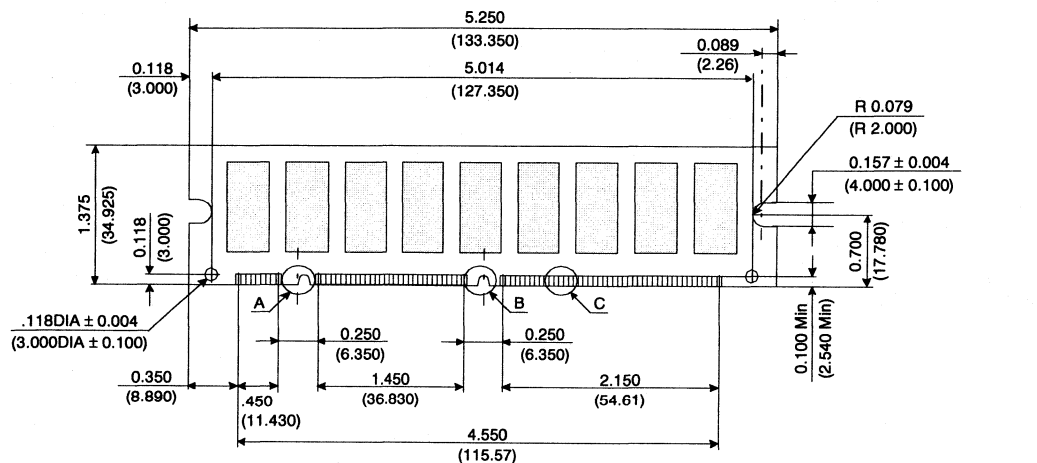
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

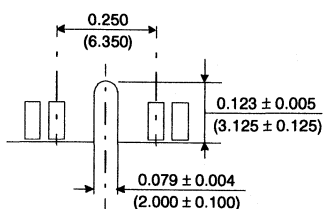
PC133 Unbuffered DIMM

PACKAGE DIMENSIONS

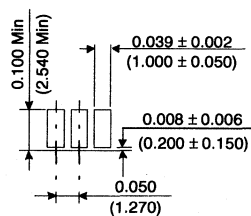
Units : Inches (Millimeters)



Detail A



Detail B



Detail C

Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 16Mx8 SDRAM, TSOP
SDRAM Part No. : K4S280832B-TC75

M374S3323BT0-C75

- Organization : 32Mx72
- Composition : 16Mx8 *18
- Used component part # : K4S280832B-TC75
- # of rows in module : 2 rows
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 4K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module ROWS on this assembly	2 rows	02h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock@CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock@CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	2 rows of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT

PC133 Unbuffered DIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	B0h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	7	37h	
77	 Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	 Manufacturer part # (Module depth)	3	33h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	 Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	FDh	6
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.
 6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M366S3253ATS SDRAM DIMM

32Mx64 SDRAM DIMM based on 32Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S3253ATS is a 32M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S3253ATS consists of eight CMOS 32M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S3253ATS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S3253ATS-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	*SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	*SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

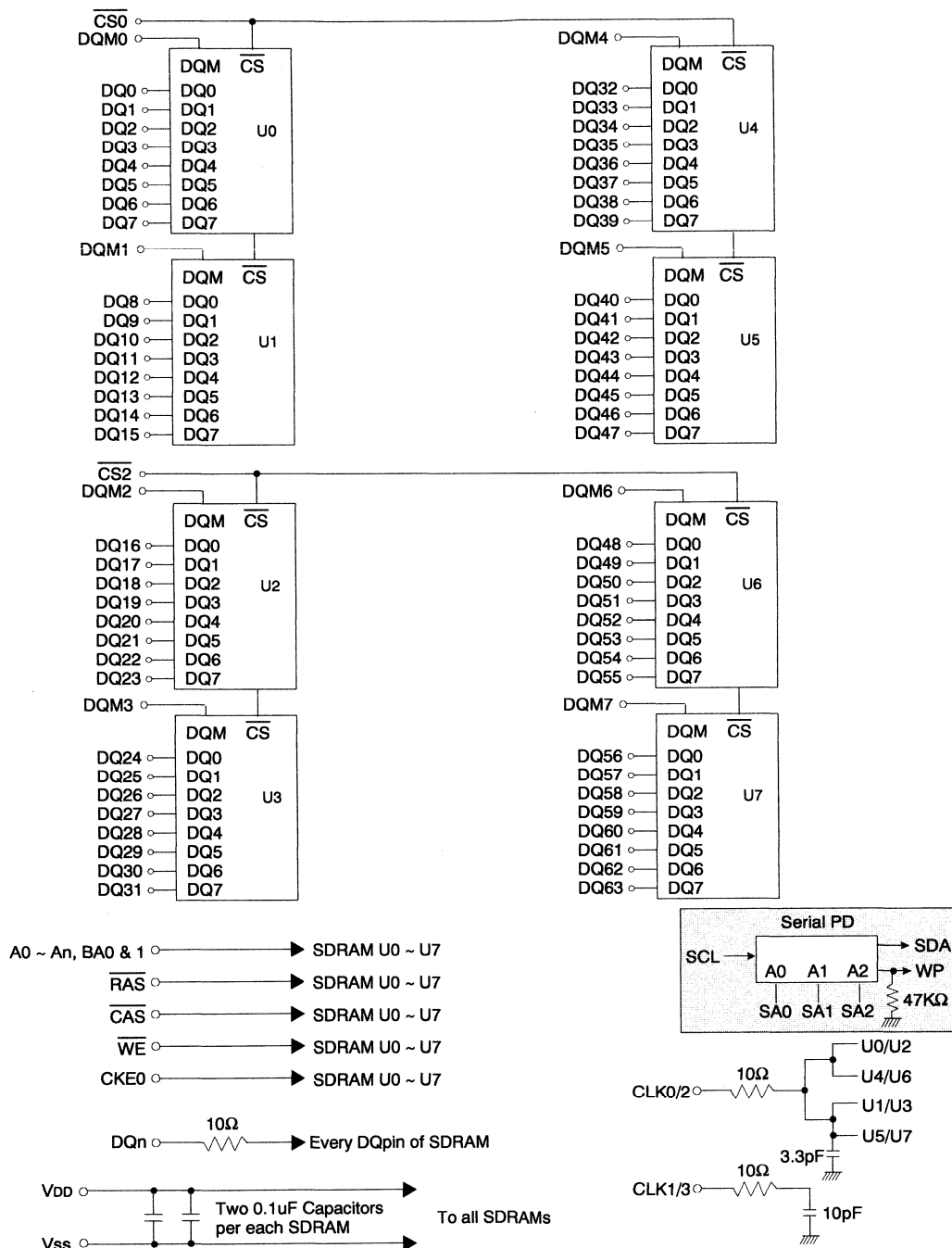
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
Vdd/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	C _{ADD}	30	40	pF
RAS, CAS, WE	C _{IN}	30	40	pF
CKE (CKE0)	C _{CKE}	30	40	pF
Clock (CLK0, CLK2)	C _{CLK}	25	30	pF
CS (CS0, CS2)	C _{CS}	16	25	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	8	10	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	6	8	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $\text{trc} \geq \text{trc}(\text{min})$ $I_O = 0 \text{ mA}$	960	mA	1
Precharge standby current in power-down mode	ICC2P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	16	mA	
	ICC2PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	16		
Precharge standby current in non power-down mode	ICC2N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	128	mA	
	ICC2NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	112		
Active standby current in power-down mode	ICC3P	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	48	mA	
	ICC3PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	48		
Active standby current in non power-down mode (One bank active)	ICC3N	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	240	mA	
	ICC3NS	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	200	mA	
Operating current (Burst mode)	ICC4	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	1,120	mA	1
Refresh current	ICC5	$\text{trc} \geq \text{trc}(\text{min})$	1,680	mA	2
Self refresh current	ICC6	$\text{CKE} \leq 0.2\text{V}$	40	mA	

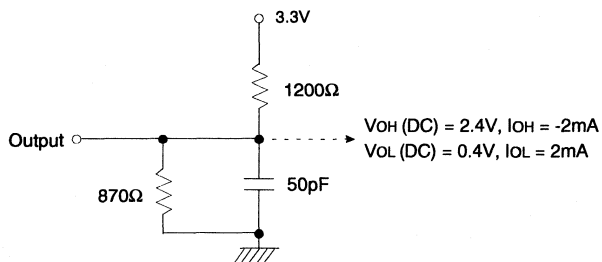
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

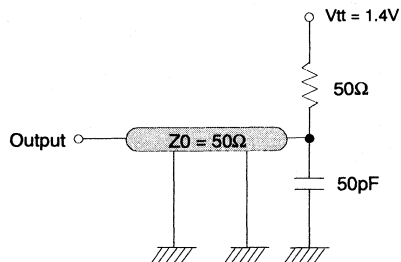
3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\min)$	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	$t_{RCD}(\min)$	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	ns	1
Row active time	$t_{RAS}(\min)$	45	ns	1
	$t_{RAS}(\max)$	100	us	
Row cycle time	$t_{RC}(\min)$	65	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20 ns		
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tCC	7.5	1000	ns	1
CLK to valid	tSAC		5.4	ns	1,2
Output data	tOH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tSS	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tSLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A12, A11, A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3	
	Entry		L									3	
	Self refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable									H		4,5	
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4	
	Auto precharge enable									H		4,5	
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X		
	All banks								X	H			
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

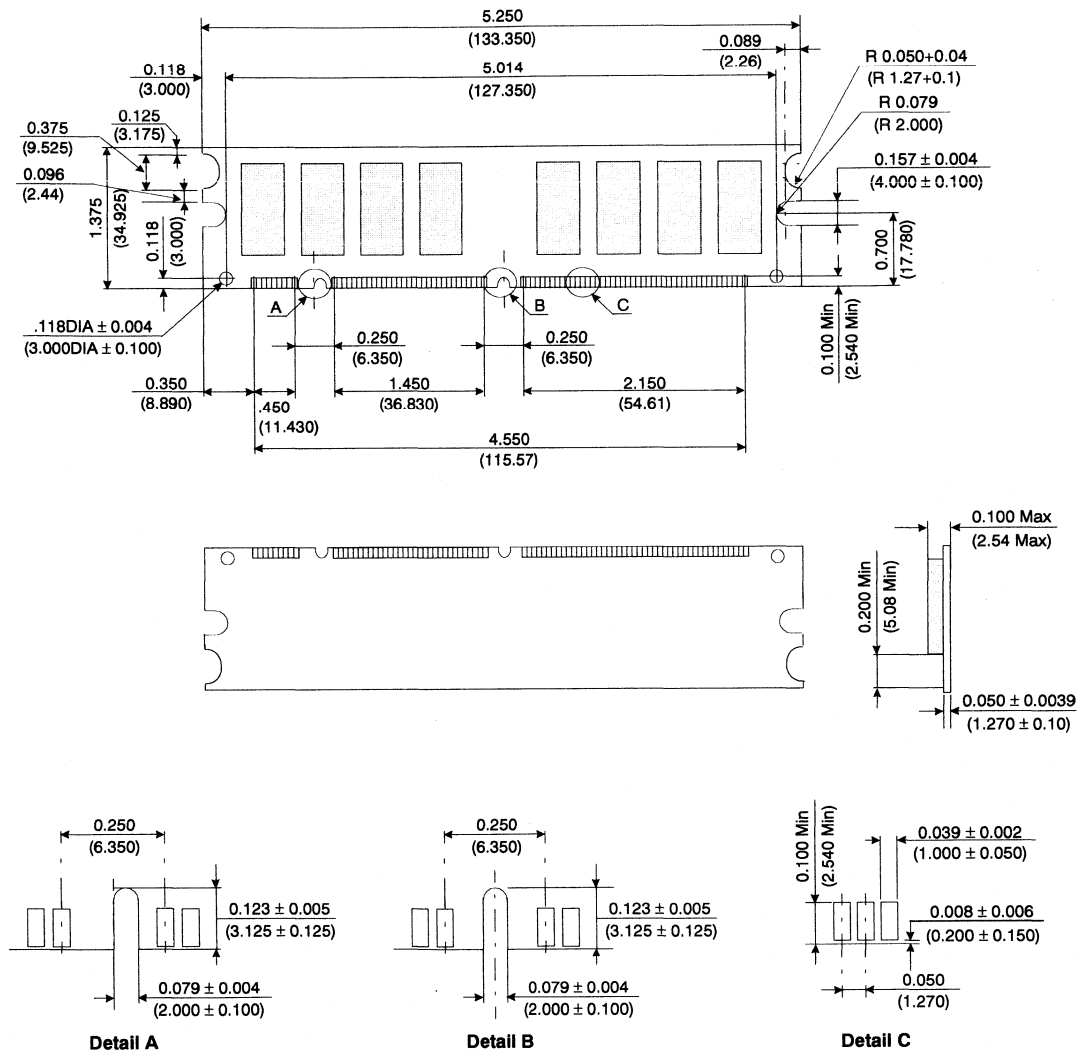
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)

Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
 SDRAM Part No. : K4S560832A-TC75

M366S3253ATS-C75

- Organization : 32Mx64
- Composition : 32Mx8 *8
- Used component part # : K4S560832A-TC75
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 8K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 row	01h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	7.8us, support self refresh	82h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	16ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 row of 256MB	40h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT

PC133 Unbuffered DIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	C0h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	 Manufacturer part # (Module depth)	2	32h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	5	35h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	S	53h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	S	53h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserverd	-	64h	6
127	Reserved	Detailed PC100 Information	ADh	6
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsungs own purpose.
 6. These values apply to PC100 application only,per Intel PC66/100 SPD standards.

M374S3253ATS

PC133 Unbuffered DIMM

M374S3253ATS SDRAM DIMM

32Mx72 SDRAM DIMM with ECC based on 32Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S3253ATS is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S3253ATS consists of nine CMOS 32M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S3253ATS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S3253ATS-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), single sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0, CLK2	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

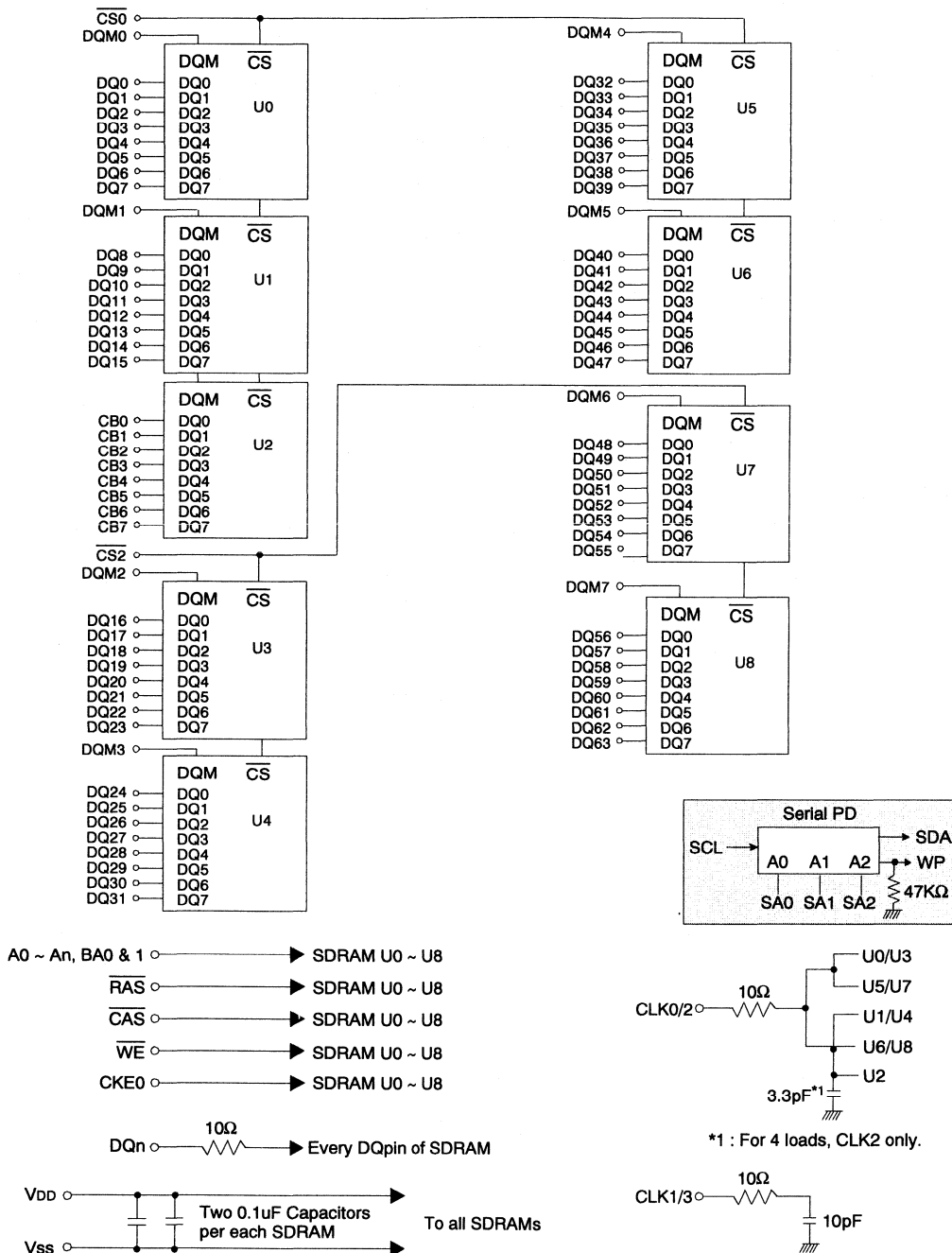
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
WE	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
Vdd/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	9	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	CADD	35	45	pF
RAS, CAS, WE	CIN	35	45	pF
CKE (CKE0)	CKE	35	45	pF
Clock (CLK0, CLK2)	CCLK	30	35	pF
CS (CS0, CS2)	CCS	20	30	pF
DQM (DQM0 ~ DQM7)	CDQM	10	15	pF
DQ (DQ0 ~ DQ63)	COUT1	6	8	pF
CB (CB0 ~ CB7)	COUT2	6	8	pF

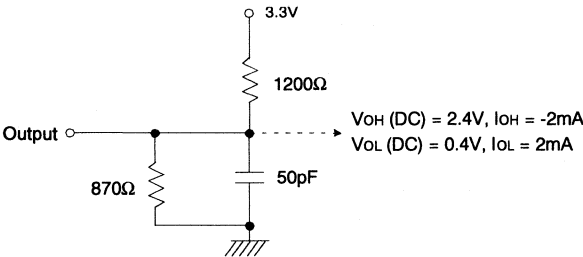
DC CHARACTERISTICS(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}(\text{min})$ $I_O = 0$ mA	1,080	mA	1
Precharge standby current in power-down mode	I_{CC2P}	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	18	mA	
	I_{CC2PS}	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	18		
Precharge standby current in non power-down mode	I_{CC2N}	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	144	mA	
	I_{CC2NS}	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	126		
Active standby current in power-down mode	I_{CC3P}	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	54	mA	
	I_{CC3PS}	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	54		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	270	mA	
	I_{CC3NS}	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	225	mA	
Operating current (Burst mode)	I_{CC4}	$I_O = 0$ mA Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	1,260	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}(\text{min})$	1,890	mA	2
Self refresh current	I_{CC6}	$\text{CKE} \leq 0.2\text{V}$	45	mA	

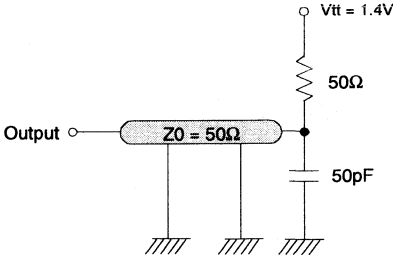
- Notes :**
1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\min)$	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	$t_{RCD}(\min)$	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	ns	1
Row active time	$t_{RAS}(\min)$	45	ns	1
	$t_{RAS}(\max)$	100	us	
Row cycle time	$t_{RC}(\min)$	65	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20 ns		
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tcc	7.5	1000	ns	1
CLK to valid	tsAC		5.4	ns	1, 2
Output data	toH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tss	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tsLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.3. Assumed input rise and fall time (tr & tf) = 1ns.If tr & tf is longer than 1ns, transient time compensation should be considered,i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A12, A11, A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

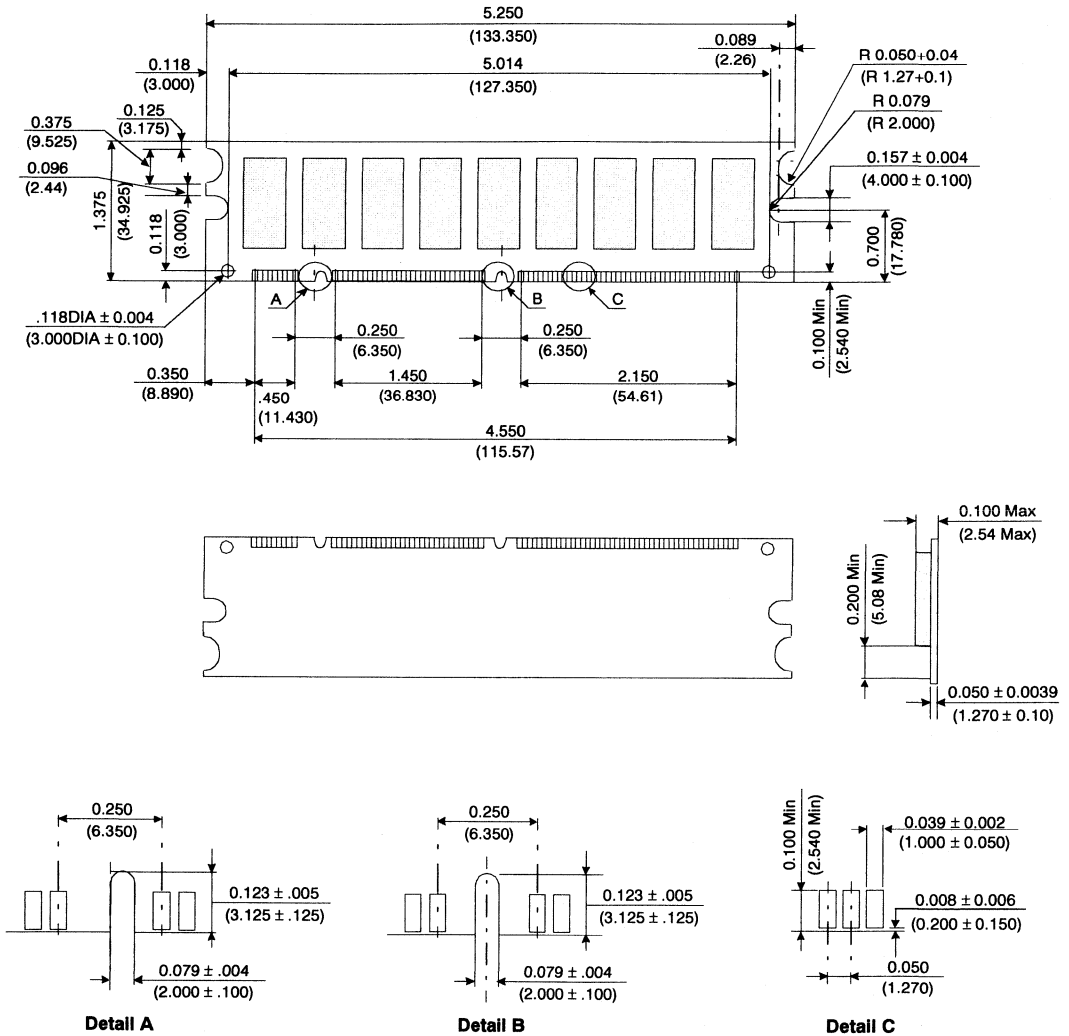
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± .005(.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
SDRAM Part No. : K4S560832A-TC75

SERIAL PRESENCE DETECT

PC133 Unbuffered DIMM

M374S3253ATS-C75

- Organization : 32Mx72
- Composition : 32Mx8 *9
- Used component part # : K4S560832A-TC75
- # of rows in module : 2 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & single sided component
- Refresh : 8K/64ms
- Contents ;

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 row	01h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	7.8us, support self refresh	82h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	16ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 row of 256MB	40h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT

PC133 Unbuffered DIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	D2h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	7	37h	
77	 Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	 Manufacturer part # (Module depth)	2	32h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	5	35h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	S	53h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	S	53h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserverd	-	64h	6
127	Reserved	Detailed PC100 Information	ADh	6
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.
 6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M366S6453AT0 SDRAM DIMM

64Mx64 SDRAM DIMM based on 32Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M366S6453AT0 is a 64M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S6453AT0 consists of sixteen CMOS 32M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S6453AT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M366S6453AT0-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V $\pm$ 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

* These pins are not used in this module.

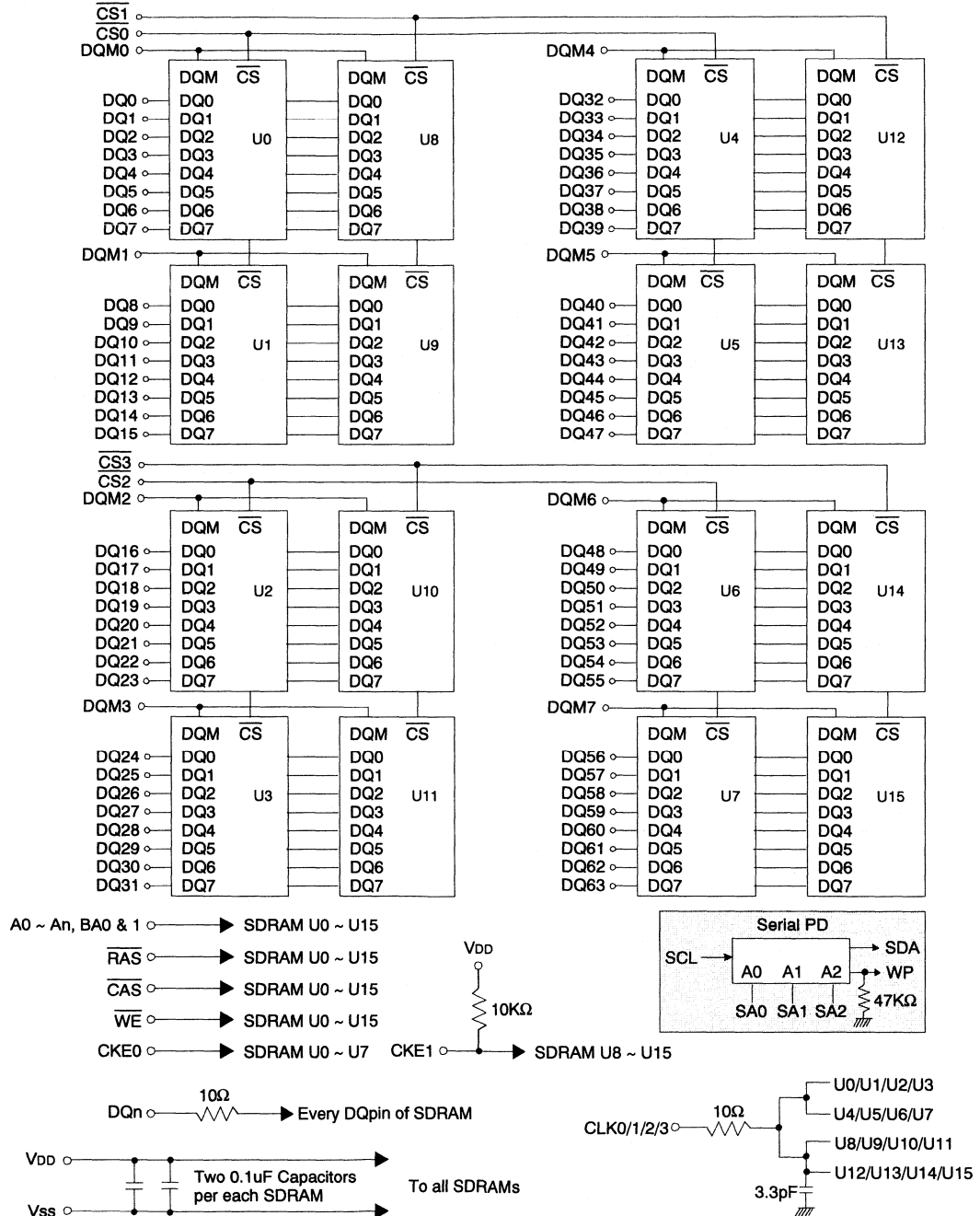
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/Vss	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	16	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	C _{ADD}	80	100	pF
RAS, CAS, WE	C _{IN}	80	100	pF
CKE (CKE0 ~ CKE1)	C _{CKE}	50	60	pF
Clock (CLK0 ~ CLK3)	C _{CLK}	40	45	pF
CS (CS0, CS2)	C _{CS}	25	35	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	15	20	pF
DQ (DQ0 ~ DQ63)	C _{OUT}	10	15	pF

DC CHARACTERISTICS(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	I _{CC1}	Burst length = 1 $\text{trc} \geq \text{trc}(\text{min})$ $I_O = 0 \text{ mA}$	1,200	mA	1
Precharge standby current in power-down mode	I _{CC2P}	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	32	mA	
	I _{CC2PS}	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	32		
Precharge standby current in non power-down mode	I _{CC2N}	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	256	mA	
	I _{CC2NS}	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	224		
Active standby current in power-down mode	I _{CC3P}	$\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$	96	mA	
	I _{CC3PS}	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$	96		
Active standby current in non power-down mode (One bank active)	I _{CC3N}	$\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	480	mA	
	I _{CC3NS}	$\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable	400	mA	
Operating current (Burst mode)	I _{CC4}	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2\text{CLKs}$	1,360	mA	1
Refresh current	I _{CC5}	$\text{trc} \geq \text{trc}(\text{min})$	1,920	mA	2
Self refresh current	I _{CC6}	$\text{CKE} \leq 0.2V$	80	mA	

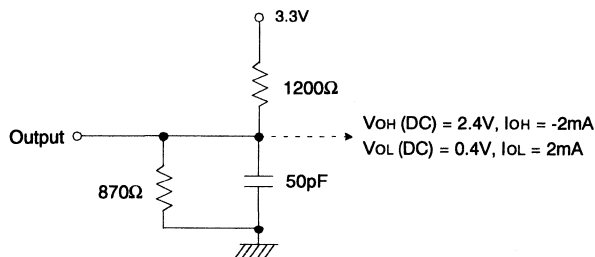
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

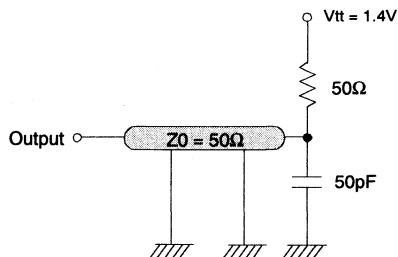
3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\min)$	15	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	ns	1
Row active time	$t_{RAS}(\min)$	45	ns	1
	$t_{RAS}(\max)$	100	us	
Row cycle time	$t_{RC}(\min)$	65	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20 ns		
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tcc	7.5	1000	ns	1
CLK to valid	tsAC		5.4	ns	1,2
Output data	toH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tss	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tsLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1ns$.
If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A12, A11 A9 ~ A0	Note	
Register	Mode register set		H	X	L	L	L	L	X	OP code		1,2	
Refresh	Auto refresh		H	H	L	L	L	H	X	X		3	
	Self refresh	Entry		L								3	
		Exit	L	H	L	H	H	X	X		3		
											H	X	X
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X		6	
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand codeA₀ ~ A₁₂ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A₁₀/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

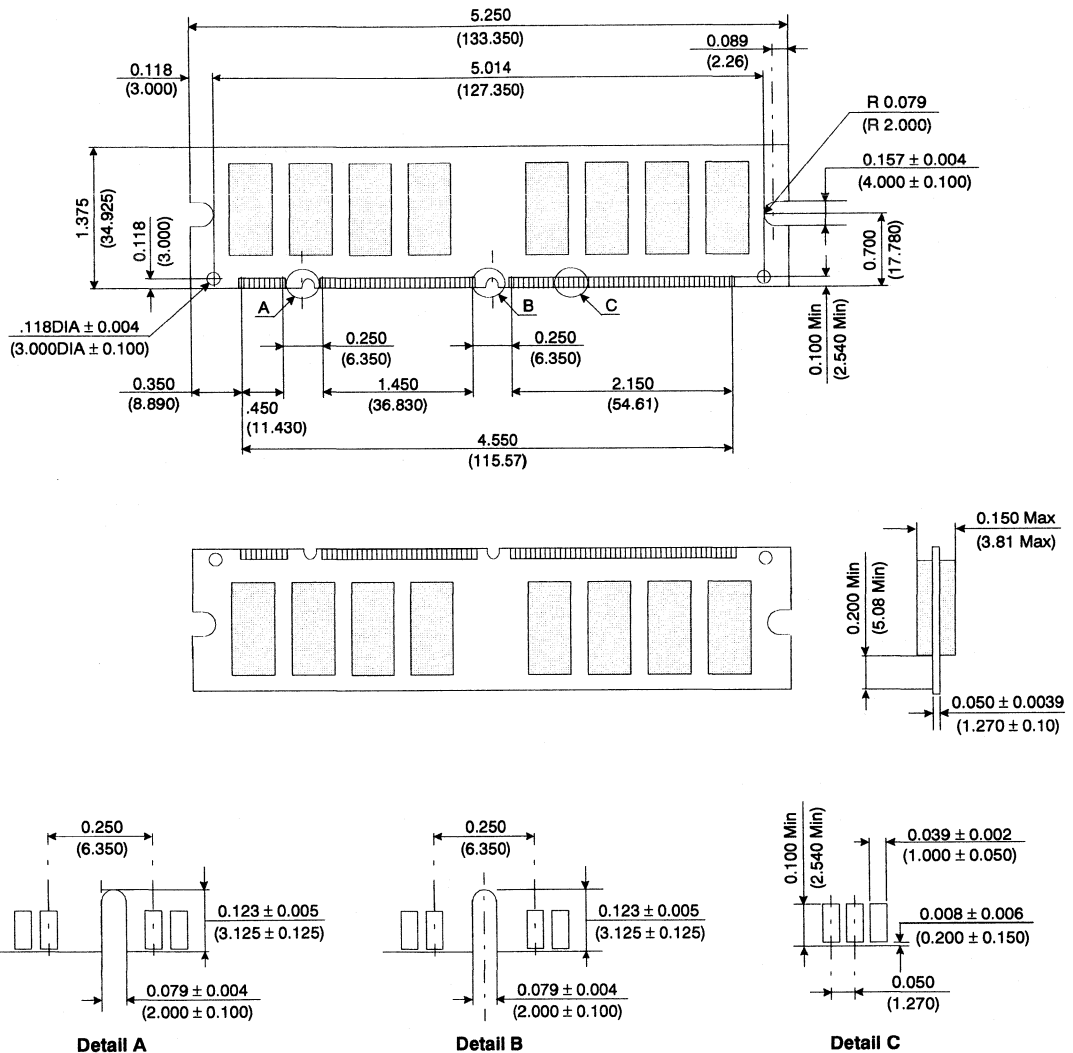
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm .005(.13)$ unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
SDRAM Part No. :K4S560832A-TC75

M366S6453AT0-C75

- Organization : 64Mx64
- Composition : 32Mx8 *16
- Used component part # : K4S560832A-TC75
- # of rows in module : 2 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 8K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	2row	02h	
6	Data width of this assembly	64 bits	40h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	7.8us, support self refresh	82h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	16ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 rows of 256MB	40h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT

PC133 Unbuffered DIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	C1h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	6	36h	
77	 Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	6	36h	
80	 Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	5	35h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	FDh	6
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.
 6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.

M374S6453AT0 SDRAM DIMM

64Mx72 SDRAM DIMM with ECC based on 32Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S6453AT0 is a 64M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S6453AT0 consists of eighteen CMOS 32M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S6453AT0 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M374S6453AT0-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
 - Latency (Access from column address)
 - Burst length (1, 2, 4, 8 & Full page)
 - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : Height (1,375mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ 7	Check bit (Data-in/data-out)
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
WP	Write protection
DU	Don't use
NC	No connection

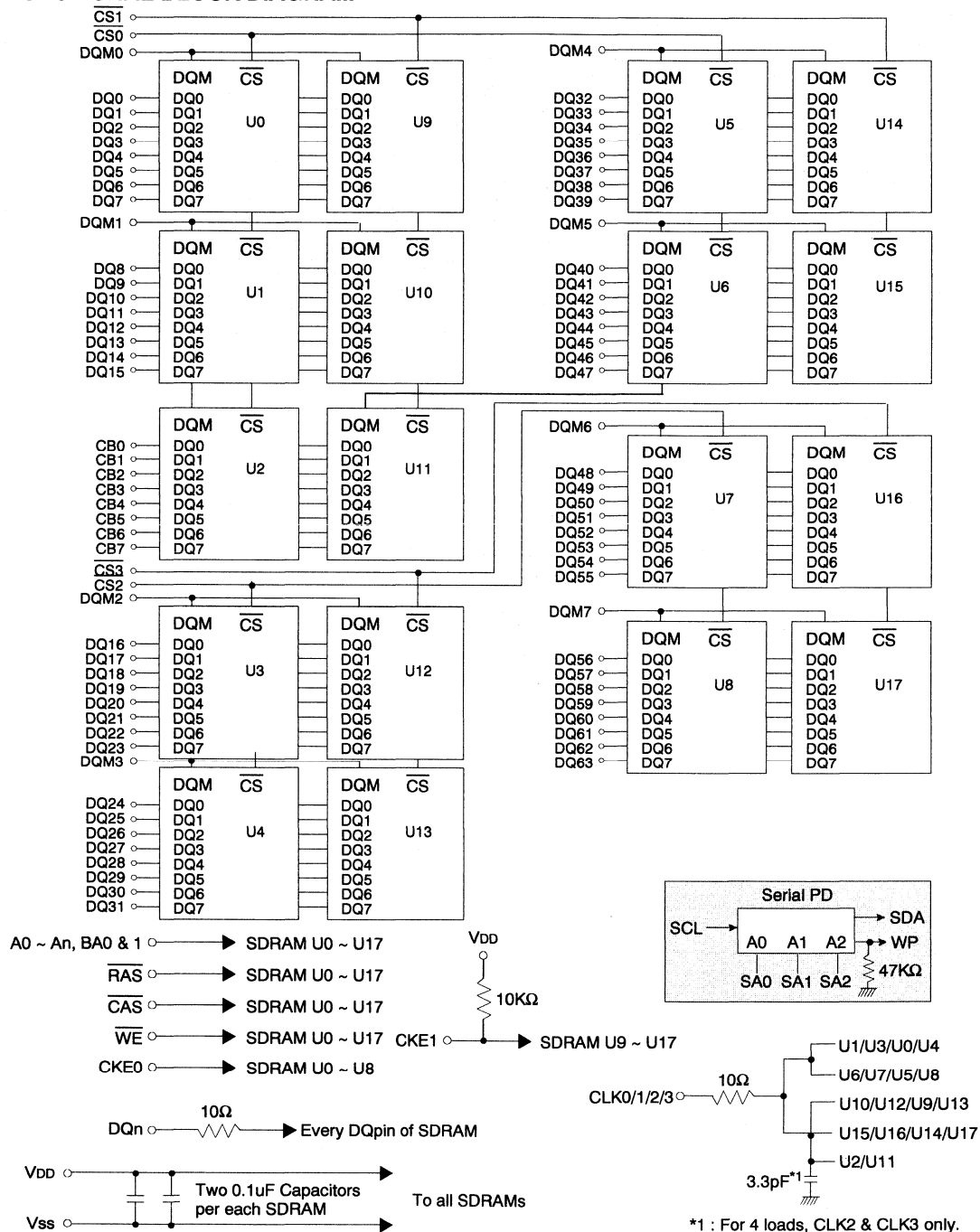
- * These pins are not used in this module.
 ** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
WP	<i>Write protection</i>	WP pin is connected to Vss through 47K Ω Resistor. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	C _{ADD}	85	105	pF
RAS, CAS, WE	C _{IN}	85	105	pF
CKE (CKE0 ~ CKE1)	C _{CKE}	50	65	pF
Clock (CLK0 ~ CLK3)	C _{CLK}	40	45	pF
CS (CS0, CS2)	C _{CS}	30	40	pF
DQM (DQM0 ~ DQM7)	C _{DQM}	25	30	pF
DQ (DQ0 ~ DQ63)	C _{OUT1}	10	15	pF
CB (CB0 ~ CB7)	C _{OUT2}	10	15	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\min)$ $I_O = 0 \text{ mA}$	1,350	mA	1
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	36	mA	
	ICC2PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	36		
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	288	mA	
	ICC2NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	252		
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL}(\max)$, $t_{CC} = 10\text{ns}$	108	mA	
	ICC3PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$	108		
Active standby current in non power-down mode (One bank active)	ICC3N	$CKE \geq V_{IH}(\min)$, $\overline{CS} \geq V_{IH}(\min)$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	540	mA	
	ICC3NS	$CKE \geq V_{IH}(\min)$, $CLK \leq V_{IL}(\max)$, $t_{CC} = \infty$ Input signals are stable	450	mA	
Operating current (Burst mode)	ICC4	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2CLKs$	1,530	mA	1
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\min)$	2,160	mA	2
Self refresh current	ICC6	$CKE \leq 0.2V$	90	mA	

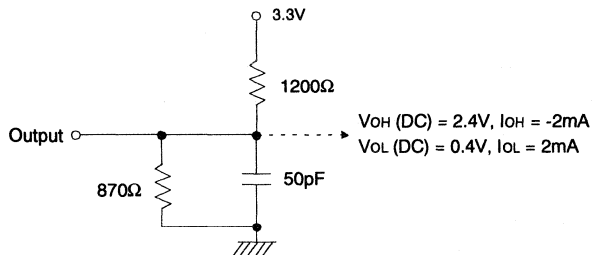
Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

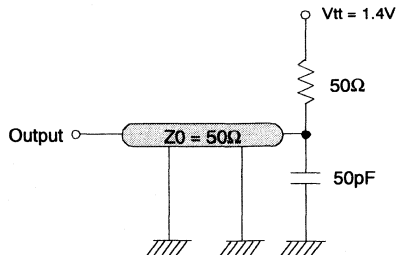
3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

Parameter	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\text{min})$	15	ns	1
RAS to CAS delay	$t_{RCD}(\text{min})$	20	ns	1
Row precharge time	$t_{RP}(\text{min})$	20	ns	1
Row active time	$t_{RAS}(\text{min})$	45	ns	1
	$t_{RAS}(\text{max})$	100	us	
Row cycle time	$t_{RC}(\text{min})$	65	ns	1
Last data in to row precharge	$t_{RDL}(\text{min})$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\text{min})$	2 CLK + 20 ns		
Last data in to new col. address delay	$t_{CDL}(\text{min})$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\text{min})$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\text{min})$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter	Symbol	-75		Unit	Note
		Min	Max		
CLK cycle time	tCC	7.5	1000	ns	1
CLK to valid	tSAC		5.4	ns	1,2
Output data	tOH	2.7		ns	2
CLK high pulse width	tCH	2.5		ns	3
CLK low pulse width	tCL	2.5		ns	3
Input setup time	tSS	1.5		ns	3
Input hold time	tSH	0.8		ns	3
CLK to output in Low-Z	tSLZ	1		ns	2
CLK to output	tSHZ		5.4	ns	

Notes : 1. Parameters depend on programmed CAS latency.2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.3. Assumed input rise and fall time (t_r & t_f) = 1ns.If t_r & t_f is longer than 1ns, transient time compensation should be considered,
i.e., $[(t_r + t_f)/2-1]$ ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A12,A11 A9 ~ A0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X		7	
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

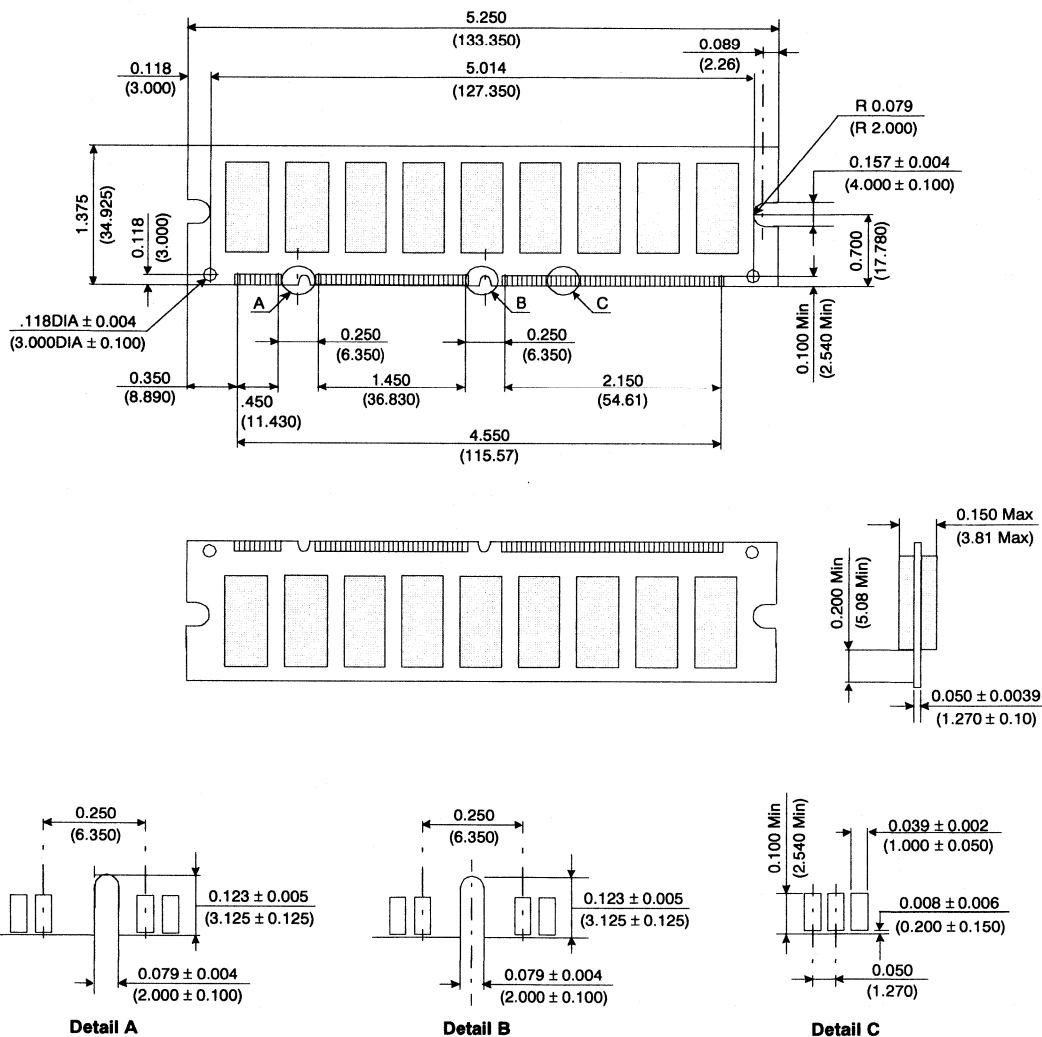
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PC133 Unbuffered DIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
SDRAM Part No. : K4S560832A-TC75

M374S6453AT0-C75

- Organization : 64Mx72
- Composition : 32Mx8 *18
- Used component part # : K4S560832A-TC75
- # of rows in module : 2 Row
- # of banks in component : 4 banks
- Feature : 1,375mil height & double sided component
- Refresh : 8K/64ms
- Contents ;

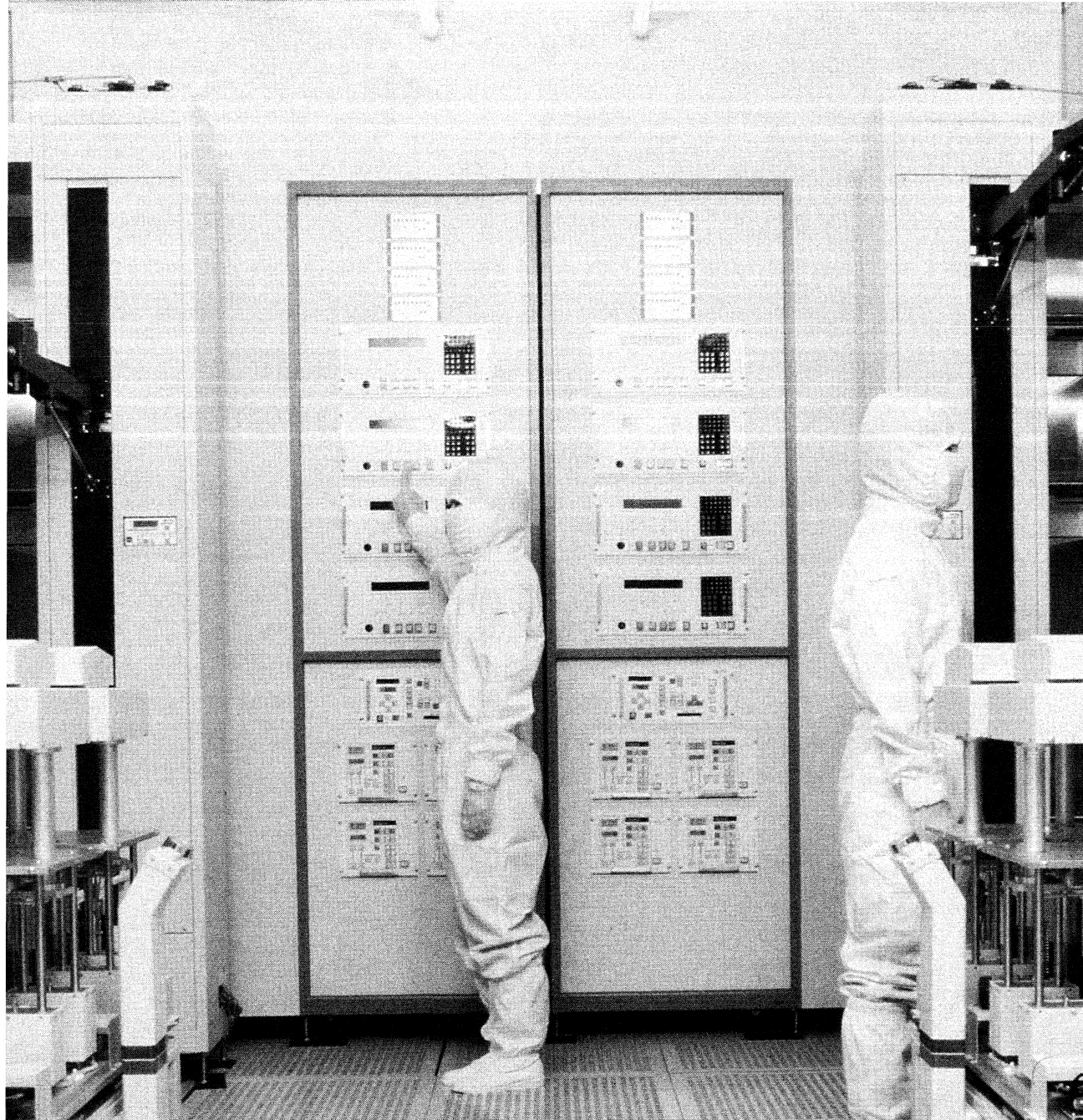
Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	2row	02h	
6	Data width of this assembly	72 bits	48h	
7	 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuraion type	ECC	02h	
12	Refresh rate & type	7.8us, support self refresh	82h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	x8	08h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	16ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 rows of 256MB	40h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT

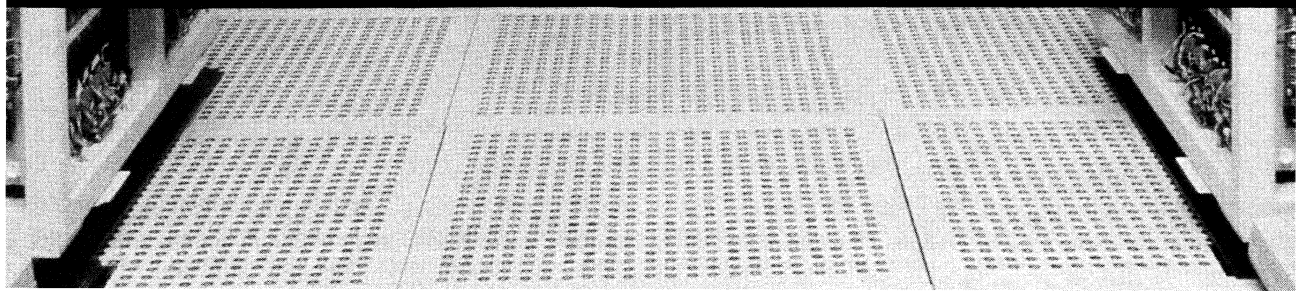
PC133 Unbuffered DIMM

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	D3h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	 Manufacturer part # (Data bits)	7	37h	
77	 Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	6	36h	
80	 Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	5	35h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	 Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	FDh	6
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
 5. These bytes are Undefined and can be used for Samsung's own purpose.
 6. These values apply to PC100 application only, per Intel PC66/100 SPD standards.



Serial Presence Detect User's Manual 4



**SDRAM DIMM(168pin)
SPD Specifications for 100MHz / 133MHz**

SERIAL PRESENCE DETECT

Part I : General Information

General Description

This appendix describes the Presence Detects for Synchronous DRAM modules. These PD are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced ; that is, after the identification of the Fundamental memory type and before identification of whether there is any Super-srt Features presented.

Address Map

The following is the SPD address map for Synchronous DRAM. It describes where the individual LUT-Entries will be held in the serial EEPROM ;

Byte #	Function Described	Function Supported	Note
0	# of Bytes written into serial memory at module manufacturer	128 Bytes	1
1	Total # of Bytes of SPD memory device	256 Bytes (2K bit)	2
2	Fundamental memory type	SDRAM	
3	# of Row address on this assembly	*	3
4	# of Column address on this assembly	*	3
5	# of Module Rows on this assembly	*	3
6	Data width of this assembly	*	3
7	... Data width of this assembly (Continued)	*	3
8	Voltage interface standard of this assembly	LVTTL	
9	SRAM cycle time from clock @CAS latency of 3	*	3
10	SRAM access time from clock @CAS latency of 3	*	3
11	DIMM configuration type	*	3
12	Refresh rate & type	*	3
13	Primary SDRAM width	*	3
14	Error checking SDRAM width	*	3
15	Minimum clock delay for back-to-back random column address	tCCD = 1 CLK	
16	SDRAM device attributes : Burst lengths supported	*	3
17	SDRAM device attributes : # of banks on SDRAM device	*	3
18	SDRAM device attributes : CAS latency	*	3
19	SDRAM device attributes : CS latency	0 CLK	
20	SDRAM device attributes : Write latency	0 CLK	
21	SDRAM module attributes	*	3
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all & auto precharge	
23	SDRAM cycle time @CAS latency of 2	*	3
24	SDRAM access time @CAS latency of 2	*	3
25	SDRAM cycle time @CAS latency of 1	*	3
26	SDRAM access time @CAS latency of 1	*	3

SERIAL PRESENCE DETECT

Byte #	Function Described	Function Supported	Note
27	Minimum row precharge time (=tRP)	*	3
28	Minimum row active to row active delay (=tRRD)	*	3
29	Minimum RAS to CAS delay (=RCD)	*	3
30	Minimum activate to precharge time (=tRAS)	*	3
31	Module Row density	*	3
32	Command and address signal input setup time	*	3
33	Command and address signal input hold time	*	3
34	Data signal input setup time	*	3
35	Data signal input hold time	*	3
32 ~ 61	Superset information (may be used in future)	-	4
62	SPD data revision code	Current release Intel spd 1.2A	
63	Checksum for Bytes 0 ~ 62	*	3
64 ~ 71	Manufacturer JEDEC ID code	Samsung	
72	Manufacturing location	Onyang Korea	
73 ~ 90	Manufacturer part #	*	3
91 ~ 92	Manufacturer revision code	*	3
93	Manufacturing date (Week)	-	5
94	Manufacturing date (Year)	-	5
95 ~ 98	Assembly serial #	-	4
99 ~ 125	Manufacturing Specific data (may be used in future)	-	6
126	System frequency for 100MHz	100MHz	
127	Intel Specification details for 100MHz Support	*	3
128 +	Unused storage locations	-	6

<Note>

1. This will be 128 Bytes for Synchronous DRAM.
2. This will be typically 256 Bytes.
3. This field is different, module by module. So, if more detail information is needed Individual SPD Datasheets.
4. These Bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These Bytes are programmed by code of Date Week & Date Year with BCD format .
6. These bytes are Undefined and can be used for Samsung 's own purpose.

SERIAL PRESENCE DETECT

Part II : Detail Byte Assignments

Byte 0 : # of Bytes written into serial memory at module manufacturer

This field describes the total number of Bytes used by the module manufacturer for the SPD data and any(optional) specific supplier information. The byte count includes the fields for all required and optional data ;

Number of Bytes	Byte 0
Undefined	00h
1 Bytes	01h
2 Bytes	02h
:	:
128 Bytes	80h
.	.
.	.
256 Bytes	FFh

Byte 1 : Total # of Bytes of SPD memory device

This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes serial memory densities(in Bytes) along with the corresponding descriptor ;

SPD memory size	Byte 1
RFU	00h
2 Bytes	01h
4 Bytes	02h
8 Bytes	03h
:	:
128 Bytes	07h
256 Bytes	08h
.	.
8192 Bytes	0Dh

Byte 2 : Fundamental memory type

This field describes the fundamental memory type (or technology) implemented on the module ;

fundamental memory type	Byte 2
Reserved	00h
Standard FPM DRAM	01h
EDO DRAM	02h
.	.
.	.
SDRAM	04h
.	.
.	.

SERIAL PRESENCE DETECT

Byte 3 : # of row address on this assembly

This field describes the number of row address bits in the SDRAM array. That is, the number of row address bits does not include the bank selects(BA0, BA1). If the module has only one bank or if the module has two banks of the same size and organization, then bits 3:0 describe the number of row address bits and bits 7:4 are 0. If the module has two banks with different size/organization, then bits 3:0 describe the row addressing for bank1 and bits 7:4 describe the row addressing for bank2 ;

# of row address	Bits 3:0	Bits 7:4
Undefined	0h	0h
:	:	:
10	Ah	Ah
11	Bh	Bh
12	Ch	Ch
13	Dh	Dh
14	Eh	Eh
15	Fh	Fh

Byte 4 : # of column address on this assembly

This field describes the number of column address bits in the SDRAM array. That is, the number of column address bits does not include the bank selects(BA0, BA1). If the module has only one bank or if the module has two banks of the same size and organization, then bits 3:0 describe the number of column address bits and bits 7:4 are 0. If the module has two banks with different size/organization, then bits 3:0 describe the column addressing for bank1 and bits 7:4 describe the column addressing for bank2 ;

# of column address	Bits 3:0	Bits 7:4
Undefined	0h	0h
:	:	:
7	7h	7h
8	8h	8h
9	9h	9h
10	Ah	Ah
11	Bh	Bh
:	:	:
15	Fh	Fh

Byte 5 : # of module Rows on this assembly

This field describes the number of module banks on the SDRAM module ;

# of module bank	Byte 5
Undefined	00h
1	01h
2	02h
:	:
254	FEh
255	FFh

SERIAL PRESENCE DETECT

Byte 6 & 7 : Data width of this assembly

Byte 6 & 7 are used to designate the data width of the module. The data width is presented as a 16bit word ; bit 0 of byte 6 becomes the LSB of the 16bit width identifier and bit 7 of byte 7 becomes MSB. Consequently, if the module has a data width less than 255 bits wide, byte 7 will be "00h". If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width ;

# of row address	Byte 6	Byte 7
Undefined	00h	00h
:	:	:
32	20h	00h
36	24h	00h
:	:	:
64	40h	00h
72	48h	00h
80	50h	00h
:	:	:
256	00h	00h

Byte 8 : Voltage interface standard of this assembly

This field describes the SDRAM module voltage & interface ;

Voltage & interface	Byte 8
5.0V/TTL	00h
LVTTL	01h
HSTL 1.5V	02h
SSTL 3.3V	03h
SSTL 2.5V	04h
TBD	05h
TBD	06h
:	:
New table	FFh

Byte 9 : SDRAM cycle time from clock @CAS latency of 3

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1(as indicated in byte 18), this byte defines tCC for CAS latency of 3. The byte is broken into two nibbles : the higher order nibble(bit4 ~7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 3, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 10 : SDRAM access time from clock @CAS latency of 3

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 3. The byte is broken into two nibbles : the higher order nibble(bit4 ~7) designates the access time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different access time @CAS latency of 3, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

SERIAL PRESENCE DETECT

Byte 11 : DIMM configuration type

This field describes the module error detection and correction scheme ;

Error detect & correct	Byte 11
None	00h
Parity	01h
ECC	02h
TBD	03h
.	.
.	.
TBD	FFh

Byte 12 : Refresh rate & type

This field describes the module's refresh rate and type. The bit 7 is especially used for self refresh flag ; if SDRAM supports self refresh, bit 7 is "1" and if not, bit 7 is "0" ;

Refresh rate/type	Byte 12
Normal(15.625us)	00h
Reduced (.5x) 7.8us	02h
:	:
Self refresh	
Normal(15.625us)	80h
Reduced (.5x) 7.8us	82h
:	:
TBD	FFh

Byte 13 : Primary SDRAM width

This field describes the data width of the primary SDRAM components used on the module. The primary SDRAM is that which is used for data ;

SDRAM data width	Byte 13
Undefined	00h
.	.
x4	04h
.	.
x8	08h
.	.
x16	10h
.	.
x32	20h
.	.
x127	7Fh

SERIAL PRESENCE DETECT

Byte 14 : Error checking SDRAM width

If the module incorporates error checking and if the primary data SDRAM does not include these bits ; i.e. there are separate error checking SDRAMs, then the error checking SDRAM width is expressed in this byte ;

ECC SDRAM data width	Byte 14
Undefined	00h
.	.
x4	04h
.	.
x8	08h
.	.
x16	10h
.	.
x32	20h
.	.
x127	7Fh

Byte 15 : Minimum clock delay for back-to-back random column addresses

Number of clocks	Byte 15
Undefined	00h
1 CLK	01h
2 CLK	02h
.	.
.	.
256 CLK	FFh

Byte 16 : SDRAM device attributes : Burst lengths supported

This field describes various burst lengths supported. If the burst length is supported, then the corresponding bit is "1". Samsung value for this field is "8Fh" because the burst lengths of 1, 2, 4, 8 and full page are supported ;

Burst length supported	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	Full page	TBD	TBD	TBD	8	4	2	1

Byte 17 : SDRAM device attributes : Number of banks on SDRAM device

This field describes the number of banks internal to the SDRAM devices ;

# of banks in component	Byte 17
Undefined	00h
1 bank	01h
2 banks	02h
.	.
4 banks	04h
.	.
256 banks	FFh

SERIAL PRESENCE DETECT

Byte 18 : SDRAM device attributes : CAS latency

This field describes which CAS latencies are supported for the module. If the bit is "1", then that CAS latency is supported ;

CAS latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	7	6	5	4	3	2	1

Byte 19 : SDRAM device attributes : CS latency

This field describes which CS latencies are acceptable for the module. If the bit is "1", then that CS latency is supported. Samsung value for this field is "01h" because CS latency of 0 is supported ;

CAS latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	6	5	4	3	2	1	0

Byte 20 : SDRAM device attributes : WE latency

This field describes which WE latencies are acceptable for the module. If the bit is "1", then that WE latency is supported. Samsung value for this field is "01h" because WE latency of 0 is supported ;

WE latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	6	5	4	3	2	1	0

Byte 21 : SDRAM module attributes: General

This field describes various aspects of the module. If the aspect is TRUE, then the corresponding bit is "1". Samsung value for this field is "00h" ;

Module attributes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	Redundant addressing	Differential CLK input	Registered DQMB input	Buffered DQMB input	On-card PLL	Registered Add/Cntr input	Buffered Add/Cntr input

Byte 22 : SDRAM device attributes : General

This field describes various aspects of the SDRAMs on the module. If the aspect is TRUE, then the corresponding bit is "1". Samsung value for this field is "0Eh" ;

Device attributes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	TBD	Upper Vdd tolerance 0=10% 1=5%	Lower Vdd tolerance 0=10% 1=5%	Support BRSW	Support precharge all	Support auto precharge	Support early RAS precharge

Byte 23 : SDRAM cycle time from clock @CAS latency of 2

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tCC for CAS latency of 2. The byte is broken into two nibbles : the higher order nibble(bit4 ~ 7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 2, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 24 : SDRAM access time from clock @CAS latency of 2

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 2. The byte is broken into two nibbles : the higher order nibble(bit4 ~ 7) designates the access time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 2, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

SERIAL PRESENCE DETECT

Byte 25 : SDRAM cycle time from clock @CAS latency of 1

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tCC for CAS latency of 1. The byte is broken into two pieces : the higher order piece(bit2 ~ 7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order piece has a granularity of 1/4ns and is added to the value of the higher piece. Samsung SDRAM has the different cycle time @CAS latency of 1, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 26 : SDRAM access time from clock @CAS latency of 1

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 1. The byte is broken into two pieces : the higher order piece(bit2 ~ 7) designates the access time to a granularity of 1ns ; the value presented by the lower order piece has a granularity of 1/4ns and is added to the value of the higher piece. Samsung SDRAM has the different access time @CAS latency of 1, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 27 : Minimum row precharge time (=tRP)

Bit 0 ~ 5 of this byte describe the precharge to active minimum(=tRP) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 28 : Minimum row active to row active delay (=tRRD)

Bit 0 ~ 5 of this byte describe the minimum row activate to row activate delay(=tRRD) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 29 : Minimum RAS to CAS delay (=tRCD)

Bit 0 ~ 5 of this byte describe the minimum RAS to CAS delay(=tRCD) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 30 : Minimum activate to precharge time (=tRAS)

Bit 0 ~ 5 of this byte describe the minimum activate to precharge time(=tRAS) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 31 : Module Row density

This field describes the density of each physical Row on the SDRAM DIMM. This field will have at least one bit to "1" to represent at least one Row density. If there are more than one Row on the module(as indicated in byte 5) and they have the same density, then only one bit is set in this field. If the module has more than one Row of different sizes, then more than one bit will be set for each density represented ;

Module Row density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If YES, the bit is "1"	512MByte	256MByte	128MByte	64MByte	32MByte	16MByte	8MByte	4MByte

Byte 32~35 : Input setup and hold time for 100MHz system frequency

Definition of these bytes are in JEDEC Ballot process. The proposed data structure is as defined:

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Posiive/ Negaive	Setup	Time	in ns	Setup	Time	in tenth	of a ns
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit 7 = 0 defines a positive setup time w.r.t. the clock

Bit 7 = 1 defines a negative setup time w.r.t. the clock

Bit 6-4 = Defines the setup time in ns.

Bit 3-0 = Defines the setup time in tenth of a ns.

Some encoded values in the table

bit 7	bit 6	bit 5	bit4	bit3	bit2	bit 1	bit 0	comment
0	0	0	0	0	0	0	0	0 ns
0	0	0	0	0	0	0	1	0.1ns
0	0	0	0	0	0	1	0	0.2ns
.	.	.	.	.	.	.	.	.
0	0	0	0	1	0	0	1	0.9ns
0	0	0	1	0	0	0	0	1.0ns
0	0	0	1	0	0	0	1	1.1ns
.	.	.	.	.	.	.	.	.
0	0	0	1	1	0	0	1	1.9ns
0	0	1	0	0	0	0	0	2.0ns
.	.	.	.	.	.	.	.	.
0	1	1	1	0	0	0	0	7.0ns
.	.	.	.	.	.	.	.	.
0	1	1	1	1	0	0	1	7.9ns
1	0	0	0	0	0	0	1	-0.1ns
1	0	0	0	0	0	1	0	-0.2ns
.	.	.	.	.	.	.	.	.
1	0	0	0	1	0	0	1	-0.9ns
1	0	0	1	0	0	0	0	-1.0ns
1	0	0	1	0	0	0	1	-1.1ns
.	.	.	.	.	.	.	.	.
1	0	0	1	1	0	0	1	-1.9ns
1	0	1	0	0	0	0	0	-2.0ns
.	.	.	.	.	.	.	.	.
1	1	1	1	0	0	0	0	-0.7ns
.	.	.	.	.	.	.	.	.
1	1	1	1	1	0	0	1	-7.9ns
x	x	x	x	1	0	1	0	RFU
.	.	.	.	.	.	.	.	RFU
x	x	x	x	1	1	1	1	RUF

SERIAL PRESENCE DETECT

Byte 32 : Command and Address signal input setup time.

This byte describes the input setup time w.r.t the rising edge of the clock input. Both positive and negative setup times are supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Positive/ Negative	Setup Time in ns			Setup Time in tenth of a ns			
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit7= 0 Defines a positive setup time w.r.t the clock.

Bit7= 1 Defines a negative setup time w.r.t the clock.

Bit 6-4= Defines a setup time in ns.

Bit 3-0= Defines a setup time in tenth of a ns.

Byte 33 : Command and Address signal input hold time.

This byte describes the input setup time w.r.t the rising edge of the clock input. Both positive and negative setup times are supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Positive/ Negative	Hold Time in ns			Hold Time in tenth of a ns			
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit7= 0 Defines a positive Hold time w.r.t the clock.

Bit7= 1 Defines a negative Hold time w.r.t the clock.

Bit 6-4= Defines a Hold time in ns.

Bit 3-0= Defines a Hold time in tenth of a ns.

Byte 34 : Data signal input setup time.

This byte describes the input setup time w.r.t the rising edge of the clock input. Both positive and negative setup times are supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Positive/ Negative	Setup Time in ns			Setup Time in tenth of a ns			
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit7= 0 Defines a positive setup time w.r.t the clock.

Bit7= 1 Defines a negative setup time w.r.t the clock.

Bit 6-4= Defines a setup time in ns.

Bit 3-0= Defines a setup time in tenth of a ns.

Byte 35 : Data signal input hold time.

This byte describes the input setup time w.r.t the rising edge of the clock input. Both positive and negative setup times are supported.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Positive/ Negative	Hold Time in ns			Hold Time in tenth of a ns			
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit7= 0 Defines a positive Hold time w.r.t the clock.

Bit7= 1 Defines a negative Hold time w.r.t the clock.

Bit 6-4= Defines a Hold time in ns.

Bit 3-0= Defines a Hold time in tenth of a ns.

SERIAL PRESENCE DETECT

Byte 36 ~ 61 : Superset information (may be used in future)

This field are reserved for superset information. Currently, these fields are programmed by "00h" because the standardization for these fields are not fixed yet.

Byte 62 : SPD data revision code

This field identifies the SDRAM DIMM SPD data revision to which the module conforms. Currently, this field is programmed by "01h"

SPD data revision code	Byte 62
Intel Initial release	00h
.	.
.	.
Intel Current Release Ver1.2A (Nov. 97)	12h
.	.
JEDEC 2.0	20h

Byte 63 : Checksum for Bytes 0 ~ 62

This field is the checksum for Bytes 0 through 62. Currently, this byte contains the value of the low 8bits of arithmetic sum of Bytes 0 through byte 62.

Byte 64 ~ 71 : Manufacturer JEDEC ID code

This field describes the manufacturer JEDEC ID code per EIA/JEP106-E. The unique code for Samsung is "CEh" only for byte64 and another Bytes, Bytes 65 ~ 71 are programmed by "00h" ;

JEDEC ID code	Byte 64	Byte 65	Byte 66	Byte 67	Byte 68	Byte 69	Byte 70	Byte 71
Samsung	CEh	00h	00h	00h	00h	00h	00h	00h

Byte 72 : Manufacturing location

This field identifies the manufacturing location and is programmed by binary code not ASCII ;

Manufacturing location	Byte 72
Kiheung Korea	00h
Onyang Korea	01h
.	.
.	.

Byte 73 ~ 90 : Manufacturer part # (ASCII code)

This fields describe the manufacturer part number and are programmed by ASCII code not binary.

Byte 73 : Samsung memory (ASCII code)

Samsung Korea	Byte 73
M	4Dh
.	.
.	.

SERIAL PRESENCE DETECT

Byte 74 : Memory type (ASCII code)

Memory type	Byte 74
3 (DIMM)	33h
4 (SODIMM)	34h
.	.
.	.

Byte 75 ~ 77 : Data bits (ASCII code)

Data bits	Byte 75	Byte 76	Byte 77
50(x72, 168pin, register & SPD , Intel)	20h	35h	30h
64(x64, 144pin, SODIMM. SPD)	20h	36h	34h
:	:	:	:
66(x64, 144pin/168pin, unbuffered & SPD)	20h	36h	36h
:	:	:	:
74(x72, 168pin, unbuffered & SPD)	20h	37h	34h
75(x72, 168pin, register, PLL & SPD, JEDEC)	20h	37h	35h
:	:	:	:
77(x72, 168pin, register, PLL & SPD , Intel)	20h	37h	37h
:	:	:	:
90 (x72, 168pin, register, PLL & SPD, PC133)	20h	39h	30h

Byte 78 : Mode & operating voltage (ASCII code)

Mode & operating voltage	Byte 78
F (EDO 3.3V)	46h
S (Sync. DRAM)	53h
.	.
.	.

SERIAL PRESENCE DETECT

Byte 79 ~ 80 : Module depth (ASCII code)

Module density	Byte 79	Byte 80
01 (1M)	30h	31h
02 (2M)	30h	32h
04 (4M)	30h	34h
08 (8M)	30h	38h
16 (16M)	31h	36h
32 (32M)	33h	32h
.	.	.
.	.	.
.	.	.

Byte 81 : Refresh. # of banks in Comp. & interface (ASCII code)

Features	Byte 81
0 (4K ref., 2banks, LVTTL)	30h
1 (2K ref., 2banks, LVTTL)	31h
2 (4K ref., 4banks, LVTTL)	32h
.	.
.	.
.	.
5 (8K ref., 4banks, LVTTL)	35h
6 (16K ref., 4banks, LVTTL)	36h
.	.
.	.
.	.

Byte 82 : Composition component (ASCII code)

Composition component	Byte 82
0 (x4)	30h
3 (x8)	33h
4 (x16)	34h
.	.
.	.
.	.

SERIAL PRESENCE DETECT

Byte 83 : Component revision (ASCII code)

Component revision	Byte 83
M (Mother die)	4Dh
A (1st Rev.)	41h
B (2nd Rev.)	42h
C (3rd Rev.)	43h
D (4rd Rev.)	44h
.	.
.	.
.	.

Byte 84 : Package type (ASCII code)

Package type	Byte 84
T (400mil TSOP II - forward)	54h

Byte 85 : PCB revision (ASCII code)

PCB revision	Byte 85
F (PC66 4 Layer)	46h
S(PC100 4 Layer)	53h
0(Modet PCB)	30h
1 (1st Rev.)	31h
1 (2nd Rev.)	32h
2 (3rd Rev.)	33h
.	.
.	.

Byte 86 : Hyphen (ASCII code)

Hyphen	Byte 86
" - "	2Dh

Byte 87 : Power (ASCII code)

Power	Byte 87
C (Auto & self Ref., normal power)	43h
L (Auto & self Ref., low power)	4Ch

SERIAL PRESENCE DETECT

Byte 88 ~ 89 : Minimum cycle time (ASCII code)

Minimum cycle time	Byte 88	Byte 89
70 (7ns =143MHz)	37h	30h
75 (7.5ns =133MHz)	37h	35h
80 (8ns=125MHz)	38h	30h
10 (10ns=100MHz)	31h	30h
1H (10ns=100MHz, PC100 CL=2)	31h	48h
1L (10ns=100MHz, PC100 CL=3)	31h	4Ch
.	.	.
.	.	.
.	.	.

Byte 90 : Manufacturer part # (TBD)

Byte 91 : Manufacturer revision code for PCB (ASCII code)

This field is referred to the module PCB revision and has the same programming code with byte.

Byte 92 : Manufacturer revision code for component (ASCII code)

This field is referred to the component revision and has the same programming code with byte 83.

Byte 93 : Manufacturing date : Week

This field describes manufacturing week and programmed with BCD format.

Byte 94 : Manufacturing date : Year

This field describes manufacturing year and programmed with BCD format.

Byte 95 ~ 98 : Assembly serial number (Binary code)

These fields describe assembly serial number. But, all of the Samsung modules are controlled by another way, not assembly serial #. Currently, this field is programmed by "00h".

Byte 99 ~ 125 : Manufacturer specific data (may be used in future)

These bytes are Undefined and can be used for Samsung's own purpose.

Byte 126 : Intel Specification for frequency

System frequency	Byte 126
66MHz	66h
100MHz	64h

SERIAL PRESENCE DETECT

Byte 127 : Intel Specification details for 100MHz Support

This byte defines the SDRAM component and Clock interconnection details for the DIMMs as defined:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLK0	CLK1	CLK2	CLK3	Juncion temp	CAS Latency = 3	CAS Latency = 2	Intel AP
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

Bit7 = 1: CLK0 is connected on the DIMM
Bit7 = 0: CLK0 is not connected on the DIMM
Bit6 = 1: CLK1 is connected on the DIMM
Bit6 = 0: CLK1 is not connected on the DIMM
Bit5 = 1: CLK2 is connected on the DIMM
Bit5 = 0: CLK2 is not connected on the DIMM
Bit4 = 1: CLK3 is connected on the DIMM
Bit4 = 0: CLK3 is not connected on the DIMM
Bit3 = 1: 100 °C junction temp
Bit3 = 0: 90 °C junction temp
Bit2 and Bit1 = 1: CL3 and CL2 support as shown

Performance Grade	Hex Value (Bits 2-1)
CAS Latency 3	04
CAS Latency 2	06

Bit0 = 1: It supports Intel defined Concurrent Auto-precharge
Bit0 = 0: It does not support Intel defined Concurrent Auto-precharge

Byte 128 ~ 255 : Unused storage locations

These bytes are Undefined and can be used for Samsung 's own purpose.

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